SONY

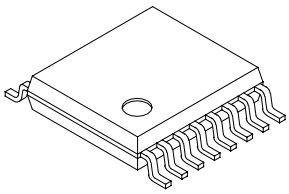
CXA3201AN

RX Gain Control Amplifier

Description

CXA3201AN is an RX gain control amplifier suitable for CDMA cellular/PCS phone.

16 pin SSOP (Plastic)



Features

- Wide gain control range
- Linear gain slope
- Wideband operation (50MHz to 300MHz)
- Very small package (16 Pin SSOP)
- Low voltage operation
- Two input ports
- Power save function included

Absolute Maximum Ratings

• Supply voltage	V_{CC}	6	V
• Operating temperature	Topr	–55 to +125	℃
• Storage temperature	Tstg	–65 to +150	℃
• Allowable Power dissipation	P_D	330	mW
• Supply voltage range		–0.3 to 6	V
• Logic input voltage		–0.3 to V_{CC} + 0.3	V
• Signal input voltage		–0.3 to V_{CC} + 0.3	V
• Differential signal input voltage		0 to 2.5	V

Operating Condition

Supply voltage	V_{CC}	2.7 to 3.8	V

Applications

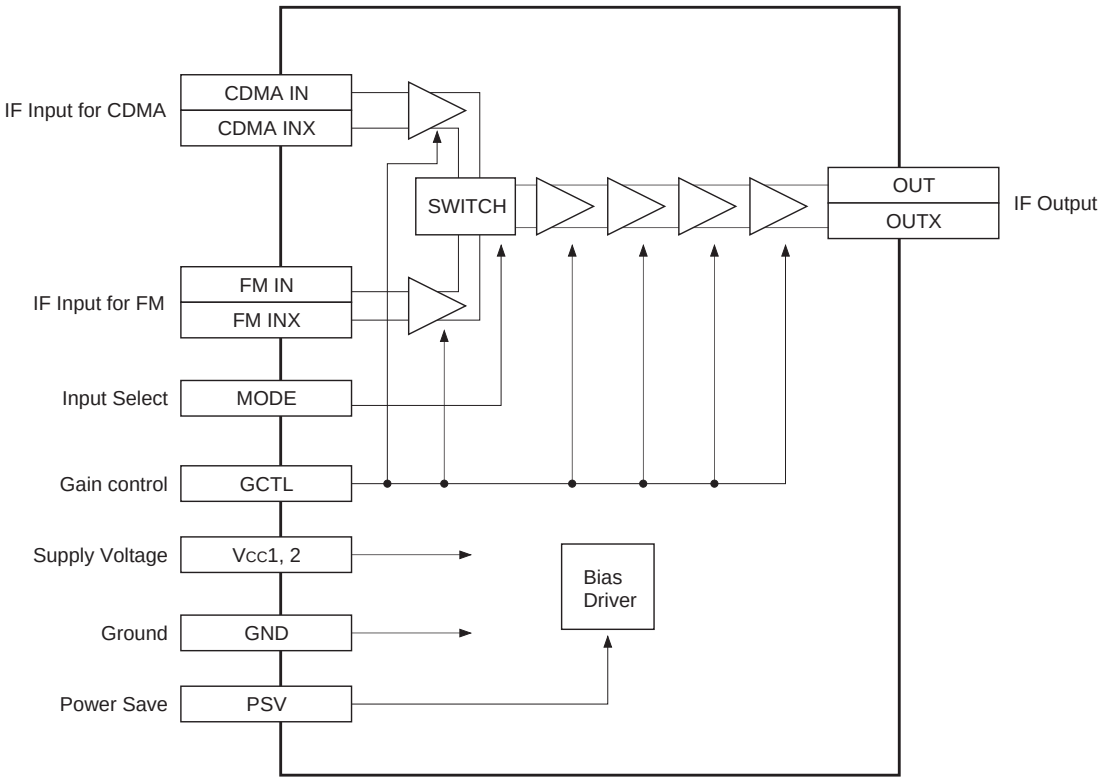
CDMA cellular/PCS phone

Structure

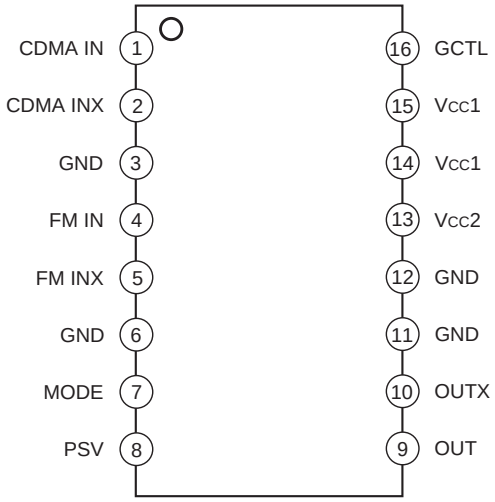
Bipolar silicon monolithic IC

E98909A8Y

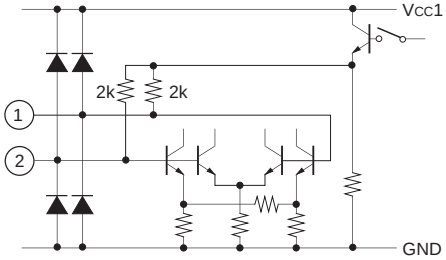
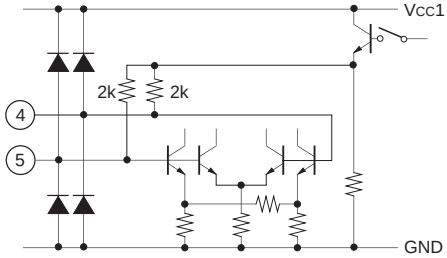
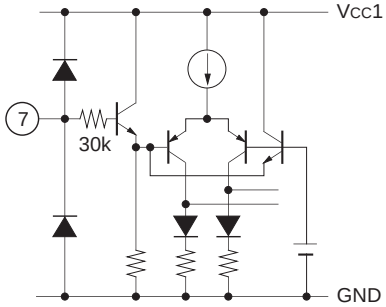
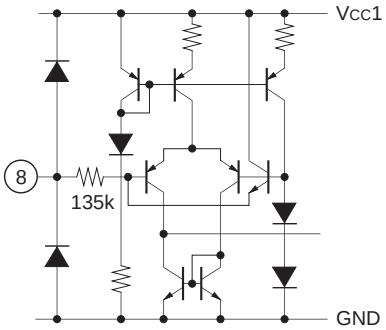
Block Diagram

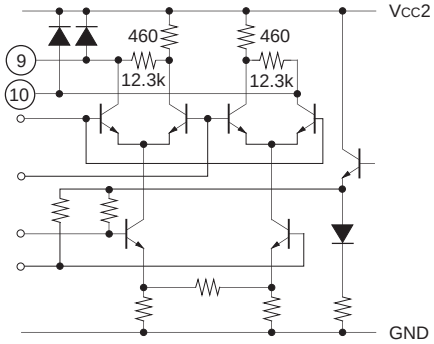
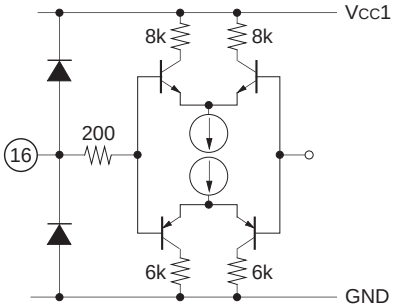


Pin Configuration



Pin Description

Pin No.	Symbol	Pin voltage TYP (V)	Equivalent circuit	Description
1	CDMA IN	1.15		Differential input pins for received CDMA IF signal.
2	CDMA INX	1.15		
3 6 11 12	GND	0		Ground.
4	FM IN	1.15		Differential input pins for received FM IF signal.
5	FM INX	1.15		
7	MODE	—		Input select pin. CDMA IN for High FM IN for Low.
8	PSV	—		Power save function pin. High: Active Low: Power save

Pin No.	Symbol	Pin voltage TYP (V)	Equivalent circuit	Description
9	OUT	—		Differential output pins for received CDMA IF signal. Open collector output.
10	OUTX	—		
13	Vcc2	3.0		Positive power supply for output stage.
14 15	Vcc1	3.0		Positive power supply.
16	GCTL	—		Gain control pin.

Electrical Characteristics

DC Characteristics

(V_{CC} = 3.0V, Ta = 27°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption 1	$I_{CC}1$	Vpsv = 3.0V, Vgctl = 1.5V, Pin 13, 14	7	10.2	15	mA
Current consumption 2	$I_{CC}2$	Vpsv = 0 V, Vgctl = 1.5V, Pin 13, 14	10	27	50	µA
Input current pin 7H	ImodeH	Vmode = 3.0V			1	
Input current pin 7L	ImodeL	Vmode = 0.5V	–1			
Input current pin 8H	IpsvH	Vpsv = 3.0V			1	
Input current pin 8L	IpsvL	Vpsv = 0 V	–15			
Input current pin 16H	IgctlH	Vgctl = 3.0V			1	
Input current pin 16L	IgctlL	Vgctl = 0.5V	–1			
MODE high voltage	VmH	Pin 7	2.5			V
MODE low voltage	VmL	Pin 7			0.5	
PSV high voltage	VpsH	Pin 8	2.5			
PSV low voltage	VpsL	Pin 8			0.5	

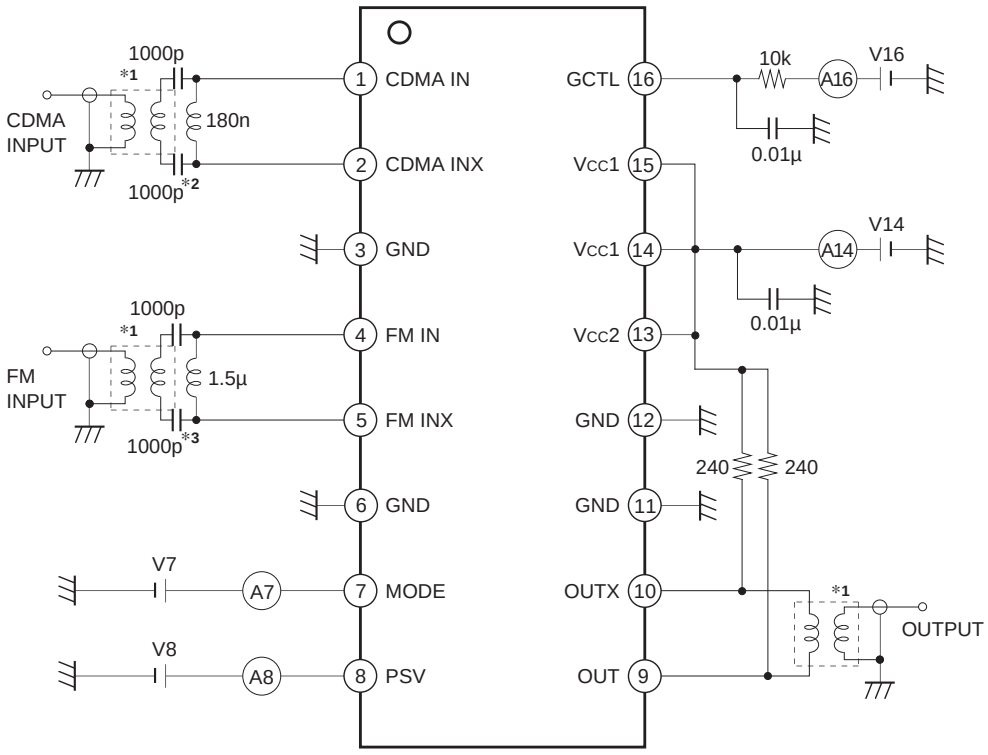
AC Characteristics

(V_{CC} = 3.0V, Ta = 27°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating frequency range	Fr		50		300	MHz
Gain CDMA2.4	$G_{CDMA}2.4$	Vmode = "H", f = 210.38MHz, Vgctl = 2.4V	42	46	50	dB
Gain CDMA1.5	$G_{CDMA}1.5$	Vmode = "H", Vgctl = 1.5V	–7	–3	1	
Gain CDMA0.6	$G_{CDMA}0.6$	Vmode = "H", Vgctl = 0.6V	–59	–55	–51	
CDMA Gain slope	G_{CLIN}	Vmode = "H", Gain CDMA at Vgctl = 2.0V – Gain CDMA at Vgctl = 1.0V	58	61	64	dB/V
Gain FM2.4	$G_{FM}2.4$	Vmode = "L", f = 85.38MHz, Vgctl = 2.4V	42	46	50	dB
Gain FM1.5	$G_{FM}1.5$	Vmode = "L", Vgctl = 1.5V	–7	–3	1	
Gain FM0.6	$G_{FM}0.6$	Vmode = "L", Vgctl = 0.6V	–59	–55	–51	
FM Gain slope	G_{FMLIN}	Vmode = "L", Gain FM at Vgctl = 2.0V – Gain FM at Vgctl = 1.0V	58	61	64	dB/V
Input level 3rd order intercept point	IIP3	Vmode = "H", G_{CDMA} = 40dB*1 f_1 = 209.38MHz, f_2 = 211.38MHz Measure of 210.38MHz	–42	–38		dBm
Noise Figure	NF	Vmode = "H", G_{CDMA} = 40dB*1 Measure of 210.38MHz		5	8	dB

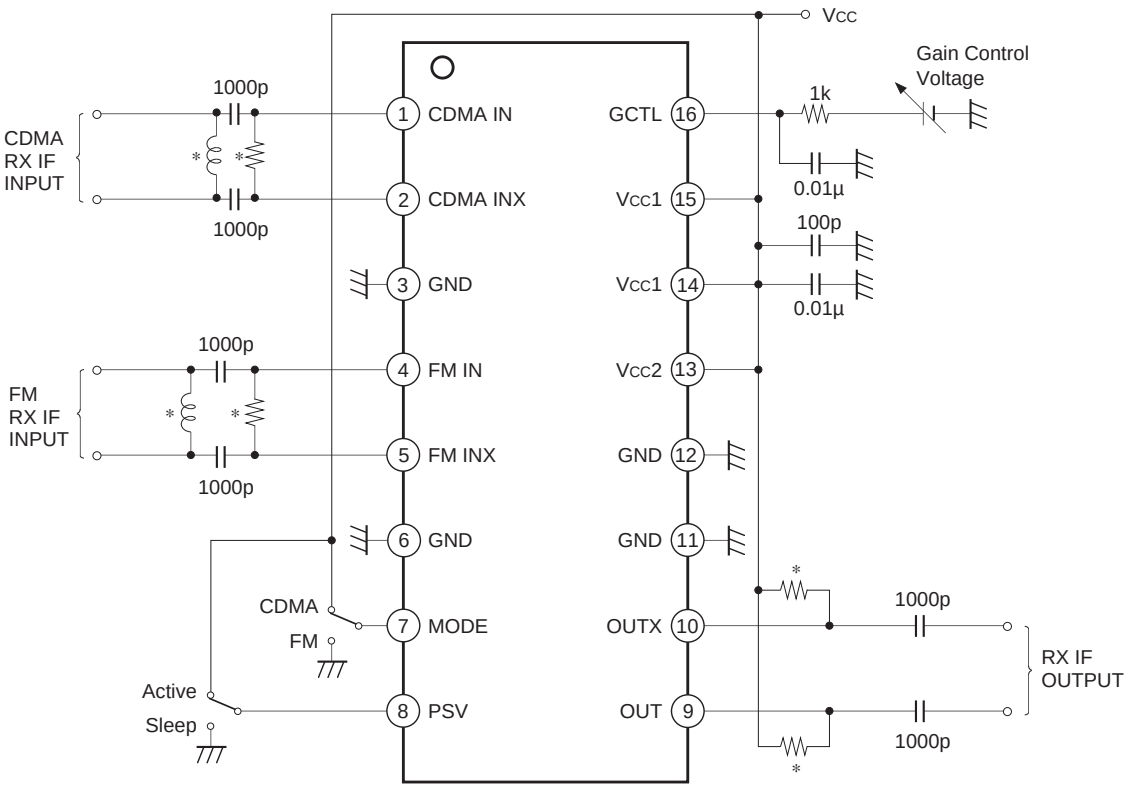
*1 Adjust GCTL voltage, and set the overall gain to 40dB.

Measurement Circuit



*1 TOKO, Inc. B5FL 616DS-1135
*2 Coilcraft, Inc. 0805HS-181TKBC
*3 Coilcraft, Inc. 1008CS-152XKBC

Application Circuit



* Must be adjusting values to result a best impedance matching between BPF filter and this IC.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Design Reference Values

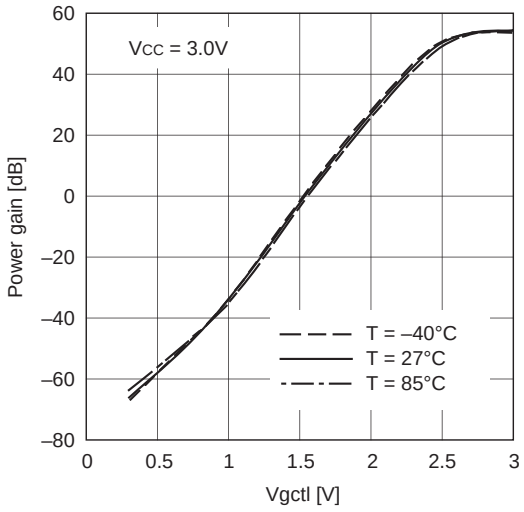
Single ended measurement (Vcc = 3.0V, Ta = 27°C)

Item	Symbol	Conditions	Typ.	Unit
Input resistance	Rin	f = 210.38MHz, Vgctl = 1.5V	1.6	kΩ
Input capacitance	Cin		1.4	pF
Output resistance	Rout		5.9	kΩ
Output capacitance	Cout		0.85	pF

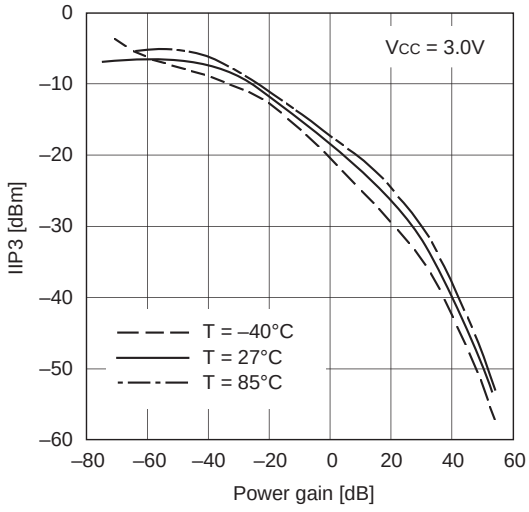
Notes on Operation

1) This IC is a wideband amplifier with wide gain control range. The decouping capacitors between GND Pin and Vcc Pin should be as close to the IC as possible.
2) The resistors connected to Pins 9 and 10 should be as close to the IC as possible.
3) This IC assumes the excellent characteristics when the differential input impedance between Pins 1 and 2, Pins 4 and 5 is 500Ω. Refer to the Measurement Circuit for the external element settings, etc.
4) Pay attention to handling this IC because its electrostatic discharge strength is weak.

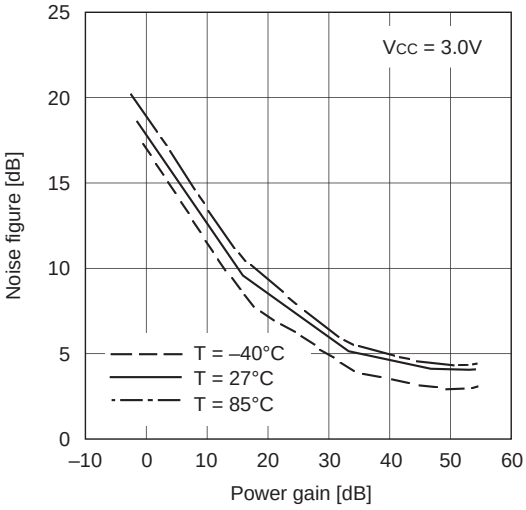
Sensitivity



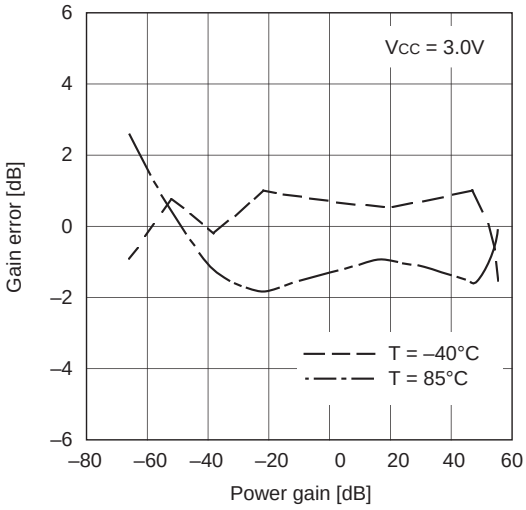
IIP3



Noise Figure

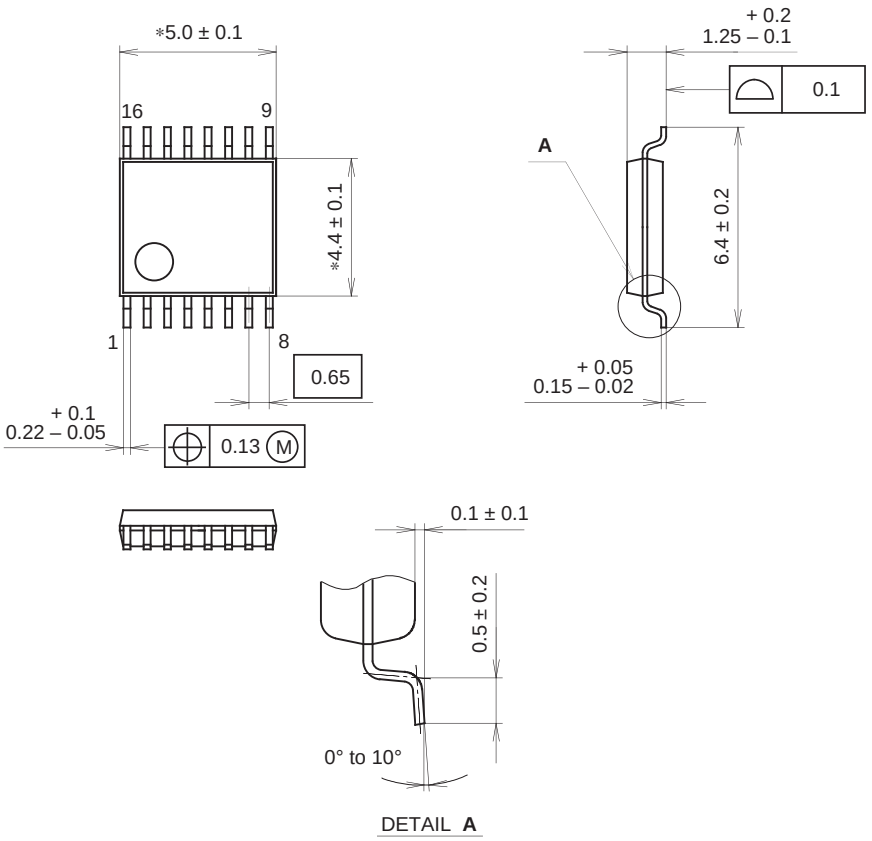


Gain Error from Room Temp



Package Outline Unit: mm

16PIN SSOP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	SSOP-16P-L01
EIAJ CODE	SSOP016-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).