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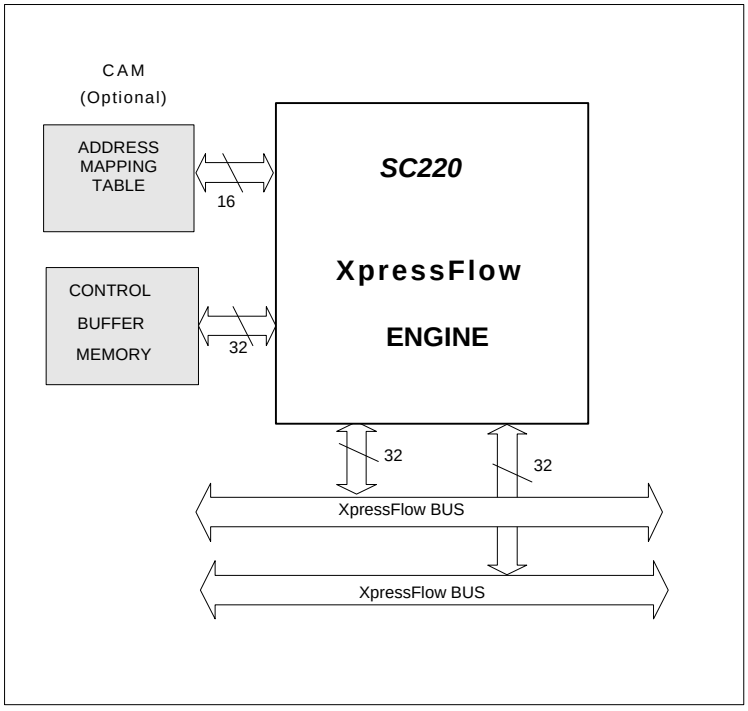
Distinctive Characteristics

- Highly integrated central switch controller
- State of the art 0.35 micron 3.3 Volt CMOS process
- 256-PIN PQFP package
- Operating frequency
  - ◊ -40 40 MHz maximum
  - ◊ -50 50 MHz maximum
  - ◊ -66 66 MHz maximum
- 16-bit external CAM interface
  - ◊ Supports ½ to 16k MAC addresses
- 32-bit Control Buffer Memory interface
  - ◊ Supports 128k to 1M bytes
  - ◊ Utilize high performance 32-bit Synchronous Burst SRAM
- Hardware assisted Buffer and Queue Management to minimize CPU overhead
- 32-bit Management Bus I/O interface
  - ◊ Allows host to access CAM and Control Buffer Memory
  - ◊ Supports Big and Little Endian CPUs
  - ◊ Direct interface with various different standard microprocessors including 386, 486 families and Motorola MPC series embedded processors
- 32-bit *XpressFlow Bus* Interface
  - ◊ Switching bandwidth
  - –1.28 Gbps @ 40 MHz system clock
  - –1.60 Gbps @ 50 MHz system clock
  - –2.10 Gbps @ 66.67 MHz system clock
  - ◊ Supports up to 8 Multi-port Network Access Controllers
  - ◊ *XpressFlow* Bus access arbitration
  - ◊ *XpressFlow* Bus data transfer load regulation
- Full IP Switching
  - ◊ Addresses resolved by SC220
- MAC Address Mapping Table
  - ◊ Supports either CAM based or SRAM based Switching data base

SC220 – XpressFlow Engine

XpressFlow 2020 Ethernet Routing Switch Chipset



SC220 - XpressFlow Engine

General Description

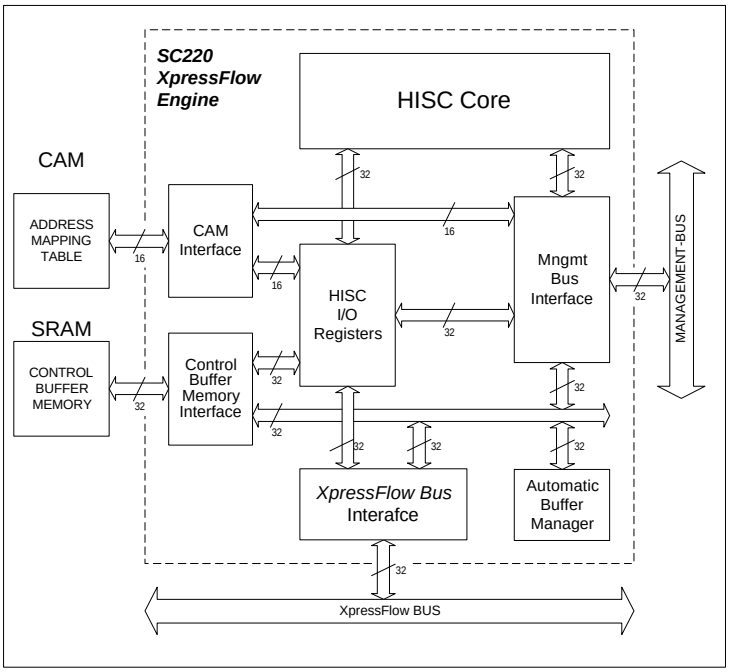
The *XpressFlow* Engine contains the switching data base interface and buffer management logic in order to do the switching decision making for unicast, multicast, and broadcast frames. Hardware assisted queue manager is incorporated to facilitate buffer management. It also provides a generic Management Bus interface to allow external processor to do initialization, learning, VLAN, and RMON support, etc. In addition, a *XpressFlow Bus* interface block is responsible for communicating with the Network Access Controllers through the *XpressFlow* message passing protocol.

Related Components:

- *EA218E* – 8-port 10Mbps Ethernet Access Controller
- *EA218* – 6-port 10 + 2-port 10/100 Ethernet Access Controller
- *EA234* – 4-port 10/100 Fast Ethernet

Characteristics Continue

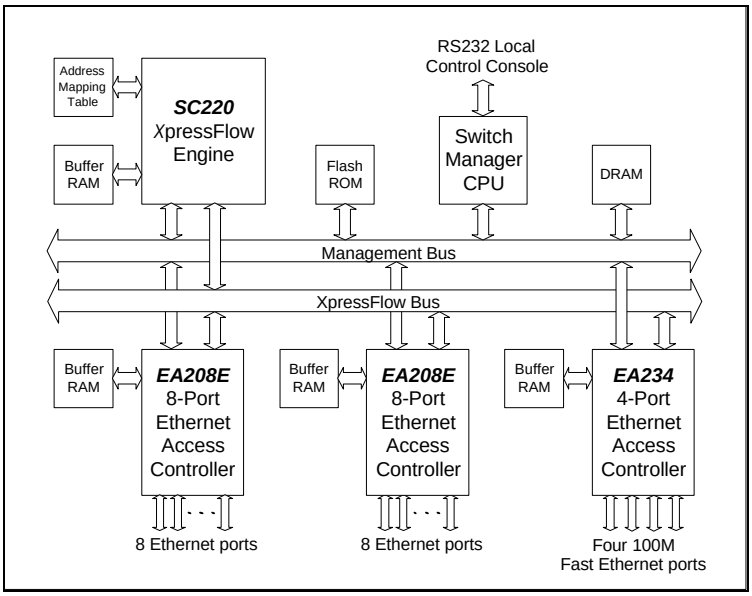
- Built-in address to port resolution
  - ◊ Embedded 32-bit HISC™ (High density Instruction Set Core) Processor
  - ◊ Optimized architecture for switch applications
  - ◊ Loadable firmware for easy upgrade
- Supports unicast, multicast, and broadcast frames
- Address Filtering
  - ◊ Destination & Source MAC address matching & filtering
- VLAN classification & verification
  - ◊ Up to 62 groups
  - ◊ Level 1 and 2 mapping
  - ◊ VLAN ID tagging & stripping
  - ◊ Auto padding if necessary after stripping
- Supports Store-&-Forward Frame Forwarding Mode
- Collects statistics for RMON



Block Diagram –
SC220 XpressFlow Engine

Typical Application:

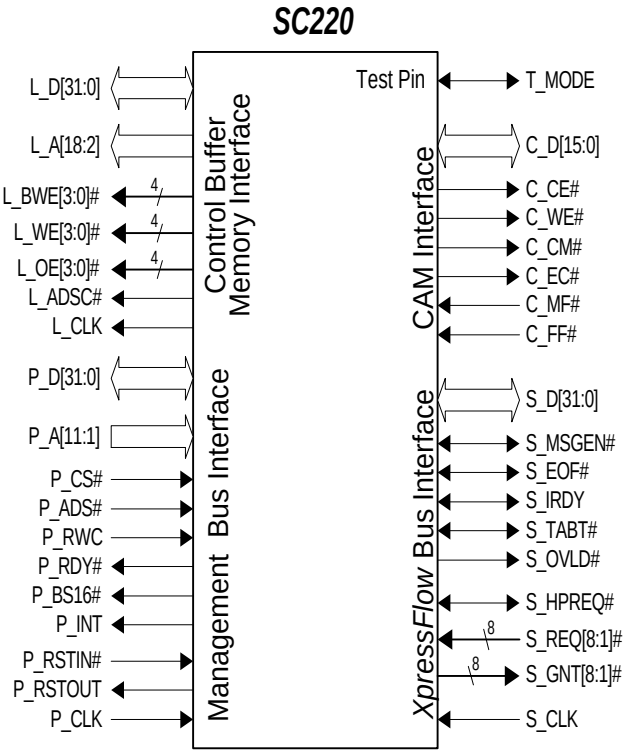
◊ A 16-port Ethernet Switch with 4-Fast Ethernet



System Block Diagram --
16-Port Ethernet Switch with 4 Fast Ethernet Up-Links

1. PIN ASSIGNMENT

1.1 Logic Symbol



Note: The SC220 is pin compatible to the SC201 with only one exception:

The RSTOUT pin of SC201 is defined as a synchronous RESET output pin which follows the RSTIN input and re-synchronous with P_CLK for meeting the 80386 timing requirement.

The RSTOUT pin for SC220 has a totally different function. It is no longer related with the RSTIN input. The RSTOUT is a watch-dog output from SC220 to keep track of the active state of the host processor. Host processor needs to access the Keep Alive register periodically to prevent the setting of the RSTOUT output. The RSTOUT output can be use as Reset input to the host processor.

1.2 *Pin Assignment* (Preliminary)

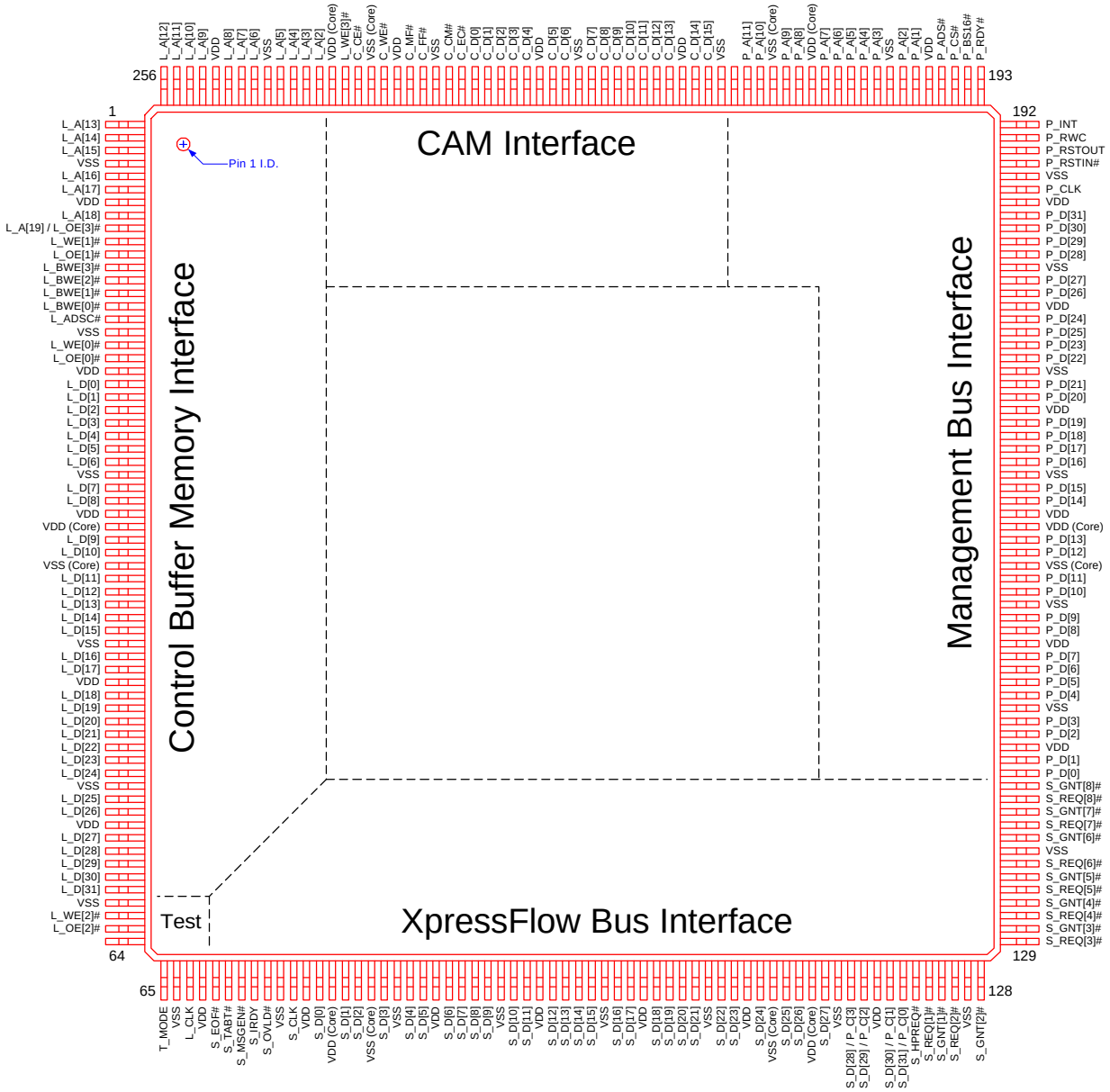
Note: # Active low signal
Input Input signal
I-ST Input signal with Schmitt-Trigger
Output Output signal (Tri-State driver)
Out-OD Output signal with Open-Drain driver
I/O-TS Input & Output signal with Tri-State driver
I/O-OD Input & Output signal with Open-Drain driver
5VT Input with 5V Tolerance

Pin No(s).	Symbol	Type	Name & Functions
XpressFlow Bus Interface			
122,121,119,118, 116	S_D[31:27] / P_C[0:4]	CMOS I/O-TS	*XpressFlow* Bus – Data Bit [31:28] *or Processor Interface Configuration Bit [0:4]*
114,113,111,109,108, 106,105,104,103,101, 100,98,97,96,95,93,92, 90,89,88,87,85,84,82, 80,79,77	S_D[26:0]	CMOS I/O-TS	*XpressFlow* Bus – Data Bit [27:0]
71	S_MSGEN#	CMOS I/O-TS	*XpressFlow* Bus – Message Envelope
69	S_EOF#	CMOS I/O-TS	*XpressFlow* Bus – End of Frame
72	S_IRDY	CMOS I/O-TS	*XpressFlow* Bus – Initiator Ready
70	S_TABT#	CMOS I/O-OD	*XpressFlow* Bus – Target Abort
123	S_HPREQ#	CMOS I/O-OD	*XpressFlow* Bus – High Priority Request
140,138,135,133,131, 129,126,124	S_REQ[8:1]#	CMOS Input **	*XpressFlow* Bus – Bus Request [8:1]
141,139,137,134,132, 130,128,125	S_GNT[8:1]#	CMOS Output	*XpressFlow* Bus – Bus Grant [8:1]
73	S_OVLD#	CMOS Output	*XpressFlow* Bus – Bus Overload
75	S_CLK	CMOS Input	*XpressFlow* Bus – Clock

Pin No(s).	Symbol	Type	Name & Functions
XpressFlow Bus Interface			
185,184,183,182,180, 179,177,176,175,174, 172,171,169,168,167, 166,164,163,160,159, 157,156,154,153,151, 150,149,148,146,145, 143,142	P_D[31:0]	TTL I/O-TS (5VT)	Management Bus – Data Bit [31:0]
211,210,208,207,205, 204,203,202,201,199, 198	P_A[11:1]	TTL Input (5VT)	Management Bus – Address Bit [11:1]
196	P_ADS#	TTL Input (5VT)	Management Bus – Address Strobe
191	P_RWC	TTL Input (5VT)	Management Bus – Read/Write Control
183	P_RDY#	CMOS Out-OD	Management Bus – Data Ready
184	P_BS16#	CMOS Out-OD	Management Bus – 16 bit Data Bus
185	P_CS#	TTL Input (5VT)	Management Bus – Chip Select
189	P_RSTIN#	TTL In-ST (5VT)	System RESET Input
190	P_RSTOUT	CMOS Output	CPU RESET Output
192	P_INT	CMOS Output	Management Bus – Interrupt Request
187	P_CLK	TTL Input (5VT)	CPU Clock
Control Buffer Memory Interface			
60,59,58,57,56,54,53,51, 50,49,48,47,46,45,43,42, 40,39,38,37,36,34,33,30, 29,27,26,25,24,23,22,21,	L_D[31:0]	TTL I/O-TS	Local Memory Bus – Data Bit [31:0]
8,6,5,3,2,1,256,255,254, 253,251,250,248,247, 246,245,244	L_A[18:2]	CMOS Output	Local Memory Bus – Address Bit [17:2]
9	L_A[19] / L_OE[3]#	CMOS Output	Local Memory Bus – Address Bit [19:18] or Memory Read Chip Select [3]
63, 11, 19	L_OE[2:0]#	CMOS Output	Local Memory Bus- Read Chip Select [2:0]
242, 62, 10, 18	L_WE[3:0]#,	CMOS Output	Local Memory Bus – Write Chip Select [3:0]
12,13,14,15	L_BWE[3:0]#	CMOS Output	Local Memory Bus – Byte Write Enable [3:0]
16	L_ADSC#	CMOS Output	Local Memory Bus – Controller Address Status
66	L_CLK	CMOS Output	Local Memory Bus – Synchronous Clock

Pin No(s).	Symbol	Type	Name & Functions
CAM Interface			
214,215,217,218,219, 220,221,222,223,225, 226,228,229,220.221,	C_D[15:0]	TTL I/O-TS (5VT)	CAM Interface – Data Bus bit [15:0]
239	C_WE#	CMOS Output	CAM Interface – Write Enable
241	C_CE#	CMOS Output	CAM Interface – Chip Enable
233	C_EC#	CMOS Output	CAM Interface – Enable Comparison
234	C_CM#	CMOS Output	CAM Interface – Data/Command Select
236	C_FF#	TTL Input (5VT)	CAM Interface – Full Flag
237	C_MF#	TTL Input (5VT)	CAM Interface – Match Flag
Test & Reserved Pins			
65	TEST	CMOS I/O-TS	Test Pin – Set Test Mode upon Reset, and provides test status output during test mode
62,63,64,67,242	n/c	---	Reserved Pins (5 pins)
Power Pins			
32,78,115,161,206,243	VDD (Core)	Input	+3.3 Volt DC Supply for Core Logic (6 pins)
7,20,31,44,55,68,76,86, 94,102,110,120,144, 152,162,170,178,186, 197,216,227,238,252	VDD	Input	+3.3 Volt DC Supply for I/O Pads (23 pins)
35,81,112,158,209,240	VSS (Core)	Input	Ground for Core Logic (6 pins)
4,17,28,41,52,61,66,74, 83,91,99,197,117,127, 136,147,155,165,173, 181,188,200,213,224, 235,249	VSS	Input	Ground for I/O Pads (26 pins)

1.3 Connection Diagram – 256-PQFP Package (Top View)



1.4 Connection Diagram – 256-BGA Package (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	L_A [13]	L_A [12]	L_A [10]		L_A[5] / P_C[3]	L_A[2] / P_C[0]		C_ MF#	C_ EC#	C_D [2]	C_D [3]	C_D [6]	C_D [10]	C_D [13]	P_A [11]	P_A [8]	P_A [6]	P_A [3]	P_ BS16#	P_ RDY#
B	L_A [14]		L_A [11]	L_A [8]	L_A [6]	L_A[3] / P_C[1]	C_ CE#		C_ CM#	C_D [1]	C_D [4]	C_D [7]	C_D [11]	C_D [14]	P_A [10]	P_A [7]	P_A [4]	P_ ADS#	P_A [2]	P_ INT
C	L_A [18]	L_A [16]	L_A [15]	L_A [9]	L_A [7]	L_A[4] / P_C[2]	L_WE [3]	C_ WE#	C_ FF#	C_D [0]	C_D [5]	C_D [9]	C_D [12]	C_D [15]	P_A [9]	P_A [5]	P_A [1]	P_ CS#	P_ RWC	P_RST OUT
D	L_OE [1]#	L_OE [3]#	L_A [17]	VDD (Core)	VSS	VDD	VSS	VDD	VSS	VSS	C_D [8]	VDD	VSS	VDD	VDD (Core)	VSS	VDD	P_RST IN#		P_ CLK
E	L_BWE [2]#	L_BWE [3]#	L_WE [1]#	VSS													VSS		P_D [31]	P_D [30]
F	L_ ADSC#	L_BWE [0]#	L_BWE [1]#	VDD													VDD	P_D [29]	P_D [28]	P_D [27]
G	L_D [0]	L_OE [0]#		VSS													VDD (Core)	P_D [26]	P_D [25]	P_D [24]
H	L_D [3]	L_D [2]	L_D [1]	L_WE [0]#													VSS	P_D [23]	P_D [22]	P_D [21]
J	L_D [7]	L_D [6]	L_D [4]	L_D [5]													VDD	P_D [20]	P_D [19]	P_D [18]
K	L_D [9]		L_D [8]	VDD													VSS	P_D [17]	P_D [16]	P_D [15]
L	L_D [10]	L_D [11]	L_D [12]	VSS													P_D [12]	P_D [13]		P_D [14]
M	L_D [13]	L_D [14]	L_D [15]	VDD (Core)													VSS	P_D [9]	P_D [10]	P_D [11]
N	L_D [16]	L_D [17]	L_D [18]	VSS													P_D [3]	P_D [6]	P_D [7]	P_D [8]
P	L_D [19]	L_D [20]	L_D [21]	VDD													VDD (Core)	P_D [2]	P_D [4]	P_D [5]
R	L_D [22]	L_D [23]	L_D [24]	L_D [26]													VDD	P_D [0]	P_D [1]	
T	L_D [25]	L_D [27]	L_D [28]	VSS													VSS	S_REQ [7]#	S_REQ [8]#	S_GNT [8]#
U	L_D [29]	L_D [30]	L_D [31]		VDD	VSS	S_D [4]	VSS	VDD	VDD (Core)	VSS	VDD	VSS	S_D [25]	S_D [29]	S_REQ [1]#	S_GNT [4]#	S_GNT [5]#	S_GNT [6]#	S_GNT [7]#
V		L_WE [2]#	L_ CLK	S_ TABT#		S_D [0]	S_D [3]	S_D [7]	S_D [10]	S_D [13]	VDD	S_D [20]	S_D [23]	S_D [26]	VDD	S_D [30]	VDD	S_REQ [4]#	S_REQ [5]#	
W	L_OE [2]#	S_MSG EN#	S_ EOF#	S_ OVLD#		S_D [1]	S_D [5]	S_D [8]	S_D [11]	S_D [14]	S_D [17]	S_D [19]	S_D [22]	VSS	S_D [27]		S_HP REQ#	S_GNT [1]#	S_REQ [6]#	S_GNT [3]#
Y	T_ MODE		S_ IRDY	S_ CLK		S_D [2]	S_D [6]	S_D [9]	S_D [12]	S_D [15]	S_D [16]	S_D [18]	S_D [21]	S_D [24]		S_D [28]	S_D [31]	S_REQ [2]#	S_GNT [2]#	S_REQ [3]#

1.5 Pin Reference Table: (256 Pin PQFP& 256-BGA)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	L_A[13]	65	TEST	129	S_REQ[3]#	193	P_RDY#
2	L_A[14]	66	VSS	130	S_GNT[3]#	194	P_BS16#
3	L_A[15]	67	L_CLK	131	S_REQ[4]#	195	P_CS#
4	VSS	68	VDD	132	S_GNT[4]#	196	P_ADS#
5	L_A[16]	69	S_EOF#	133	S_REQ[5]#	197	VDD
6	L_A[17]	70	S_TABT#	134	S_GNT[5]#	198	P_A[1]
7	VDD	71	S_MSGEN#	135	S_REQ[6]#	199	P_A[2]
8	L_A[18]	72	S_IRDY	136	VSS	200	VSS
9	L_A[19] / L_OE[3]#	73	S_OVLD#	137	S_GNT[6]#	201	P_A[3]
10	L_WE[1]#	74	VSS	138	S_REQ[7]#	202	P_A[4]
11	L_OE[1]#	75	S_CLK	139	S_GNT[7]#	203	P_A[5]
12	L_BWE[3]#	76	VDD	140	S_REQ[8]#	204	P_A[6]
13	L_BWE[2]#	77	S_D[0]	141	S_GNT[8]#	205	P_A[7]
14	L_BWE[1]#	78	VDD (Core)	142	P_D[0]	206	VDD (Core)
15	L_BWE[0]#	79	S_D[1]	143	P_D[1]	207	P_A[8]
16	L_ADSC#	80	S_D[2]	144	VDD	208	P_A[9]
17	VSS	81	VSS (Core)	145	P_D[2]	209	VSS (Core)
18	L_WE[0]#	82	S_D[3]	146	P_D[3]	210	P_A[10]
19	L_OE[0]#	83	VSS	147	VSS	211	P_A[11]
20	VDD	84	S_D[4]	148	P_D[4]	212	
21	L_D[0]	85	S_D[5]	149	P_D[5]	213	VSS
22	L_D[1]	86	VDD	150	P_D[6]	214	C_D[15]
23	L_D[2]	87	S_D[6]	151	P_D[7]	215	C_D[14]
24	L_D[3]	88	S_D[7]	152	VDD	216	VDD
25	L_D[4]	89	S_D[8]	153	P_D[8]	217	C_D[13]
26	L_D[5]	90	S_D[9]	154	P_D[9]	218	C_D[12]
27	L_D[6]	91	VSS	155	VSS	219	C_D[11]
28	VSS	92	S_D[10]	156	P _D[10]	220	C_D[10]
29	L_D[7]	93	S_D[11]	157	P_D[11]	221	C_D[9]
30	L_D[8]	94	VDD	158	VSS (Core)	222	C_D[8]
31	VDD	95	S_D[12]	159	P_D[12]	223	C_D[7]
32	VDD (Core)	96	S_D[13]	160	P_D[13]	224	VSS
33	L_D[9]	97	S_D[14]	161	VDD (Core)	225	C_D[6]
34	L_D[10]	98	S_D[15]	162	VDD	226	C_D[5]
35	VSS (Core)	99	VSS	163	P_D[14]	227	VDD
36	L_D[11]	100	S_D[16]	164	P_D[15]	228	C_D[4]
37	L_D[12]	101	S_D[17]	165	VSS	229	C_D[3]
38	L_D[13]	102	VDD	166	P_D[16]	230	C_D[2]
39	L_D[14]	103	S_D[18]	167	P_D[17]	231	C_D[1]
40	L_D[15]	104	S_D[19]	168	P_D[18]	232	C_D[0]
41	VSS	105	S_D[20]	169	P_D[19]	233	C_EC#
42	L_D[16]	106	S_D[21]	170	VDD	234	C_CM#
43	L_D[17]	107	VSS	171	P_D[20]	235	VSS
44	VDD	108	S_D[22]	172	P_D[21]	236	C_FF#
45	L_D[18]	109	S_D[23]	173	VSS	237	C_MF#
46	L_D[19]	110	VDD	174	P_D[22]	238	VDD
47	L_D[20]	111	S_D[24]	175	P_D[23]	239	C_WE#
48	L_D[21]	112	VSS (Core)	176	P_D[24]	240	VSS (Core)
49	L_D[22]	113	S_D[25]	177	P_D[25]	241	C_CE#
50	L_D[23]	114	S_D[26]	178	VDD	242	L_WE[3]
51	L_D[24]	115	VDD (Core)	179	P_D[26]	243	VDD (Core)
52	VSS	116	S_D[27]	180	P_D[27]	244	L_A[2] / P_C[0]
53	L_D[25]	117	VSS	181	VSS	245	L_A[3] / P_C[1]
54	L_D[26]	118	S_D[28]	182	P_D[28]	246	L_A[4] / P_C[2]
55	VDD	119	S_D[29]	183	P_D[29]	247	L_A[5] / P_C[3]
56	L_D[27]	120	VDD	184	P_D[30]	248	L_A[6]
57	L_D[28]	121	S_D[30]	185	P_D[31]	249	VSS
58	L_D[29]	122	S_D[31]	186	VDD	250	L_A[7]
59	L_D[30]	123	S_HPREQ#	187	P_CLK	251	L_A[8]
60	L_D[31]	124	S_REQ[1]#	188	VSS	252	VDD
61	VSS	125	S_GNT[1]#	189	P_RSTIN#	253	L_A[9]
62	L_WE[2]#	126	S_REQ[2]#	190	P_RSTOUT	254	L_A[10]
63	L_OE[2]#	127	VSS	191	P_RWC	255	L_A[11]
64		128	S_GNT[2]#	192	P_INT	256	L_A[12]

Note: ① For 256-BGA package: F4, K4, P4, U5, U9, U12, V11, V15, V17, R17, J17, F17, D17, D14, D12, D8 and D6 are VDD.

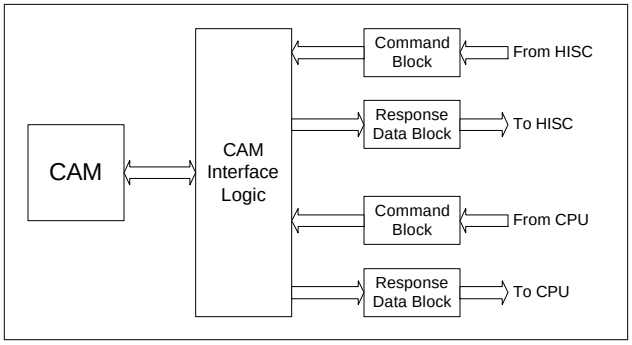
② For 256-BGA package: D4, M4, U10, P17, G17 and D15 are VDD(Core).

③ For 256-BGA package: E4, G4, L4, N4, T4, U6, U8, U11, U13, W14, T17, M17, K17, H17, E17, D16, D13, D10, D9, D7, and D5 are VSS.

2 FUNCTIONAL DESCRIPTION

2.1 CAM Interface

- Direct interface with MUSIC MU9C1480 1k x 64 bit Content Addressable Memory (CAM)
  - ◊ Expandable to support 8k MAC Addresses
- Two access masters: HISC in *XpressFlow* Engine, and Switch Manager CPU
- Master interface with CAM Interface logic via two dedicated CAM Command Blocks
  - ◊ One for HISC
  - ◊ One for Switch Manager CPU



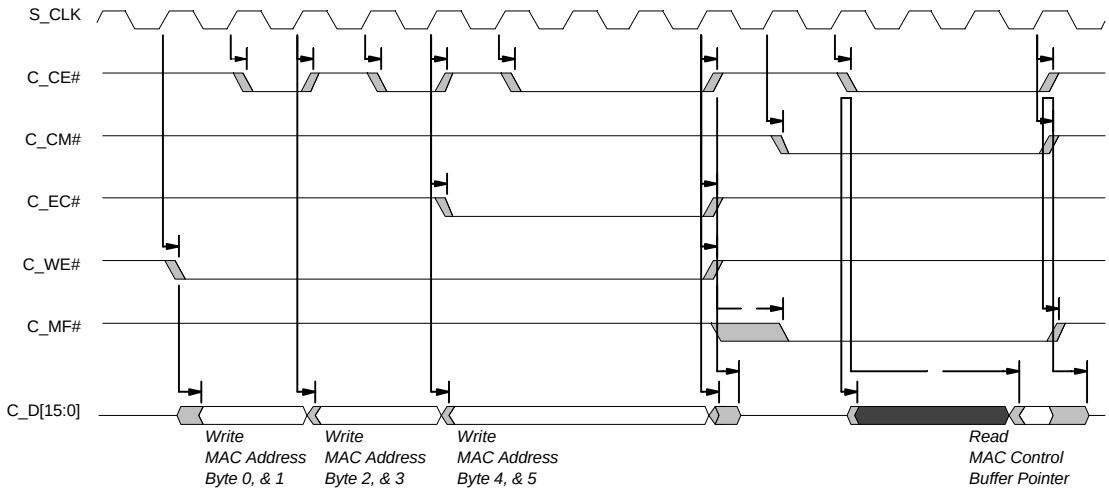
Block Diagram – CAM Interface

- Both HISC and Switch Manager CPU can access the CAM by setting up their corresponding CAM Command Blocks, and read the return information from their own Response Data Block

2.1.1 Pin Description

Symbol	Type	Name & Functions
C_D[15:0]	TTL I/O-TS	*CAM Data Bus bit [15:0]* – a 16-bit data bus for Data/Command input/output.
C_CE#	CMOS Output	*CAM Chip Enable* – Enables the CAM by registers the control signals on its falling edge and release them on its rising edge. Also used for locking and unlocking the cascaded daisy chain.
C_WE#	CMOS Output	*CAM Write Enable* – allows to write data or command to CAM
C_CM#	CMOS Output	*CAM Data/Command Select* – defines data or command operations
C_EC#	CMOS Output	*CAM Enable Comparison* – latches and enables the MF and FF outputs during a comparison cycle.
C_MF#	TTL Input	*CAM Match Flag* – indicates a valid match during a comparison cycle.
C_FF#	TTL Input	*CAM Full Flag* – indicates there is no empty location in the CAM.

2.1.2 Bus Cycle Waveforms



Typical MAC Address Compare Operation

Note: Refer to MUSIC MU9C1480 CAM data sheet for detailed timing parameters.

2.2 Local Memory (Control Buffer Memory) Interface

- Uses industry standard Synchronous Burst SRAM (Pipe-lined Mode)
  - Supports 64k x 32, 128k x 32, or 256k x 32 chips up to maximum 2M bytes
- Provides 4 individual *Byte Write Enable* controls
- Supports back to back Read or Write operations

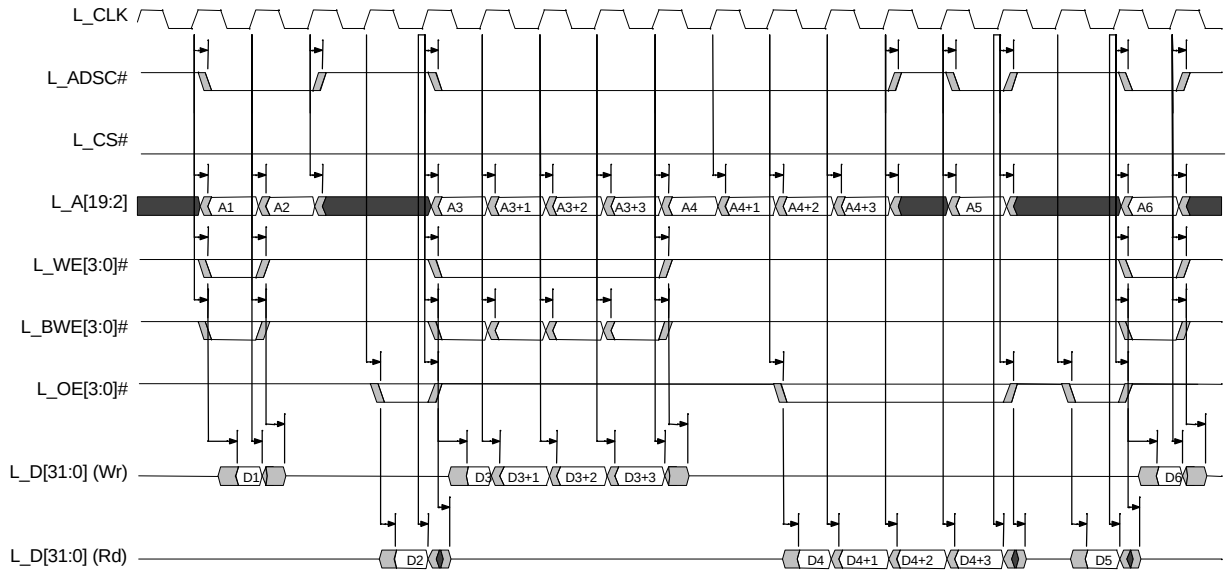
2.2.1 Pin Description

Symbol	Type	Name & Functions
L_D[31:0]	TTL I/O-TS	*Local Memory Data Bus Bit [31:0]* – a 32-bit synchronous data bus.
L_A[18:2]	CMOS Output	*Local Memory Address Bus Bit [18:2]* – Bit [17:2] of a synchronous address bus. The memory address is sampled when L_CS# is enabled and L_ADSC# is asserted.
L_A[19] / L_WE[3]#	CMOS Output	*Local Memory Address Bus Bit [19] or Local Memory Write Chip Select [3]* – Depends on memory configuration, this pin can be used as the Local Memory Address Bit [19] or as the Local Memory Write Chip Select [3].
L_WE[2:0]#	CMOS Output	*Local Memory Write Chip Select [2:0]* – allows up to write one of the 4 banks of memory.
L_OE[3:0]#	CMOS Output	*Local Memory Read Chip Select [3:0]* – allows up to read one of the 4 banks of memory.
L_BWE[3:0]#	CMOS Output	*Local Memory Byte Write Enable [3:0]* – use to write individual bytes.
L_ADSC#	CMOS Output	*Local Memory Controller Address Status* – to load a new address.
L_CLK	CMOS Output	*Local Memory Clock* – a synchronous clock to memory devices.

Supported Memory Configurations

RAM Chip Size	# of RAM Chips	Total Buffer Memory Size	Read/Write Chip Select and High Address Bits							
			Chip #3		Chip #2		Chip #1		Chip #0	
			L_A[19] / L_WE[3]#	L_OE[3]#	L_WE[2]#	L_OE[2]#	L_WE[1]#	L_OE[1]#	L_WE[0]#	L_OE[0]#
64k x 32	1	256k bytes	----	----	----	----	----	----	L_WE[0]#	L_OE[0]#
	2	512k bytes	----	----	----	----	L_WE[1]#	L_OE[1]#	L_WE[0]#	L_OE[0]#
	4	1M bytes	L_WE[3]#	L_OE[3]#	L_WE[2]#	L_OE[2]#	L_WE[1]#	L_OE[1]#	L_WE[0]#	L_OE[0]#
128k x 32	1	256k bytes	----	----	----	----	----	----	L_WE[0]#	L_OE[0]#
	2	1M bytes	----	----	----	----	L_WE[1]#	L_OE[1]#	L_WE[0]#	L_OE[0]#
	4	2M bytes	L_WE[3]#	L_OE[3]#	L_WE[2]#	L_OE[2]#	L_WE[1]#	L_OE[1]#	L_WE[0]#	L_OE[0]#
256k x32	1	1M bytes	L_A[19]	----	----	----	----	----	L_WE[0]#	L_OE[0]#
	2	2M bytes	L_A[19]	----	----	----	L_WE[1]#	L_OE[1]#	L_WE[0]#	L_OE[0]#

2.2.2 Bus Cycle Waveforms



Typical Local Memory Access Operations

Note: Refer to manufacturer's data sheet for detailed timing parameters.

2.3 Management Bus Interface

- Supports various industry standard micro-processors including:
  - Intel 186/486 family or equivalent
  - Motorola MPC series embedded processors
- Easily adapts to other industry standard CPUs
- Provides separate Address and Data bus
- Supports Big & Little Endian byte ordering
- Supports 16- or 32-bit Data Bus
- Provides a single interrupt signal to Switch Manager CPU

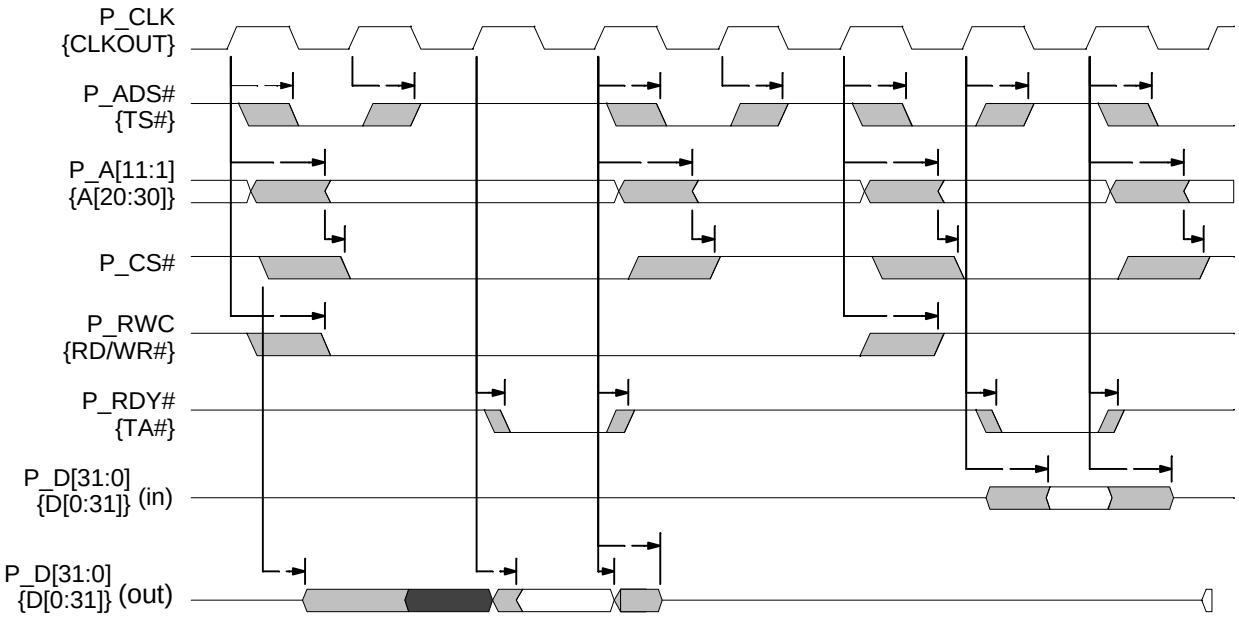
2.3.1 Pin Description

Symbol	Type	Name & Functions
P_C[4:0]	CMOS Input	*Processor Configuration bit [4:0]*: – During the Reset Cycle, the P_C[4:0] pins provides the processor configuration. By using external weak pull-up or -down resistors, they define the External Management Bus Interface Configuration. These inputs are sampled at the trailing edge of the Reset cycle. C[0] – Defines the CPU Clock input is 1X or 2X clock C[1] – Selects either Big or Little Endian byte ordering C[2] – Defines the polarity of the P_RWC (Rd/Wr Control) input C[3] – Defines the CPU Data Bus width – 16-bit or 32-bit C[4] – Defines the timing relationship between P_RDY and P_D[15:0] valid. If C[4] is High, the P_D[15:0] are valid along in the same clock period as P_RDY is asserted. If C[4] is Low, the P_RDY is asserted one clock period early ahead of the P_D[15:0] are valid. After RESET, these pins are used as *XpressFlow* Bus Data bit [31:27].
P_A[11:1]	TTL In (5VT)	*Address Bus Bit [11:1]* – I/O port address
P_D[15:0]	TTL I/O-TS (5VT)	*Data Bus Bit [15:0]* – a 16-bit synchronous data bus.
P_ADS#	TTL In (5VT)	*Address Strobe* – indicates valid address is on the bus
P_RWC	TTL In-put (5VT)	*Read/Write Control* – indicates the current bus cycle is a read or write cycle. C[1] defines the polarity of this signal during the Reset cycle. C[1]=Low P_R/W# is used for PowerPC or other similar processors. C[1]=High P_W/R# is used for 386, 486 or other similar processors
P_RDY#	TTL Out-OD	*Data Ready* – timing indicates for bus data valid
P_BS16#	TTL Out-OD	*Bus Size 16* – response to bus master that the SC-201 only supports 16-bit data bus width.
P_CS#	TTL In (5VT)	*Chip Select* – indicates the *XpressFlow* Engine is the target for the current bus operation.
P_INT ①	TTL Out-put	*Interrupt Request* to Switch Manager CPU *The polarity of this signal output is programmable via chip configuration register*.
P_RSTIN#	TTL In-ST (5VT)	*Power Up Reset Input* – Asynchronous Reset Input from either Power-Up Reset circuit or from Switch Manager CPU (except 386)
P_RSTOUT	CMOS Output	*Synchronous Reset Output* – Synchronous Reset Output for i386 family as the Switch Manager CPU
P_CLK	TTL In (5VT)	*CPU Clock* – 1X Clock for the others

	C[0]	C[1]	C[2]	C[3]	C[4]
	CPU Clock	Byte Order	RWC	Bus Width	RDY Timing
Lo	1X Clock	Little Endian	P_R/W#	16-bit	Normal
Hi	2x Clock	Big Endian	P_W/R#	32-bit	Early

Note: ① Output signal with programmable polarity.

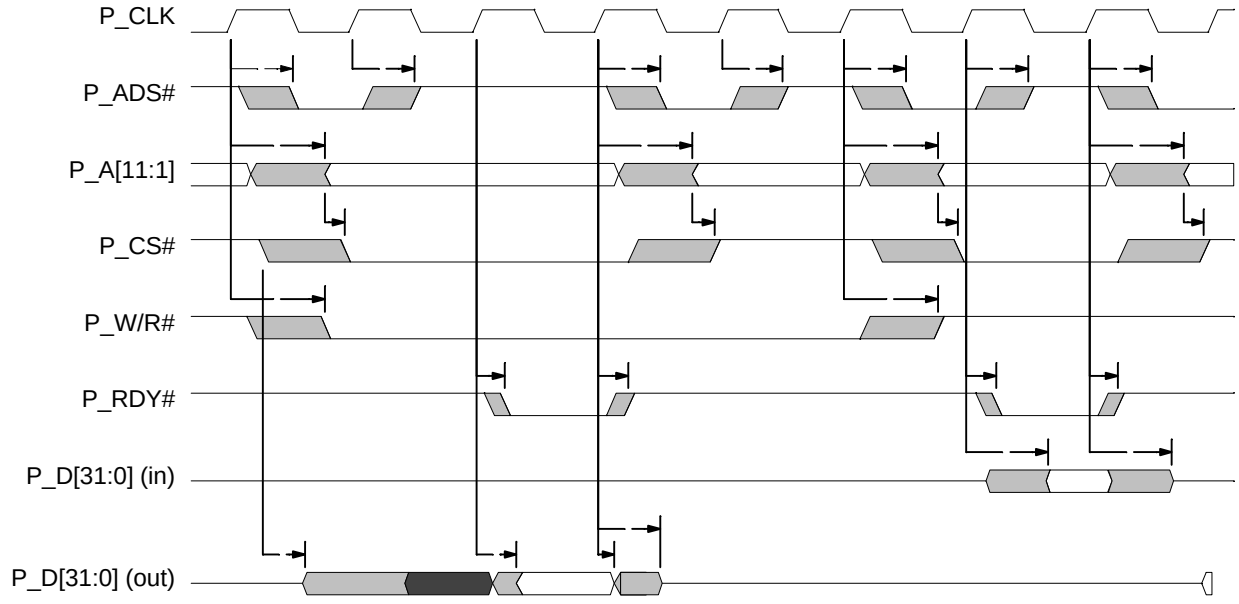
2.3.2 Motorola MPC801 Processor Interface



Note: Mnemonics within {} are the equivalent signals defined by MPC801

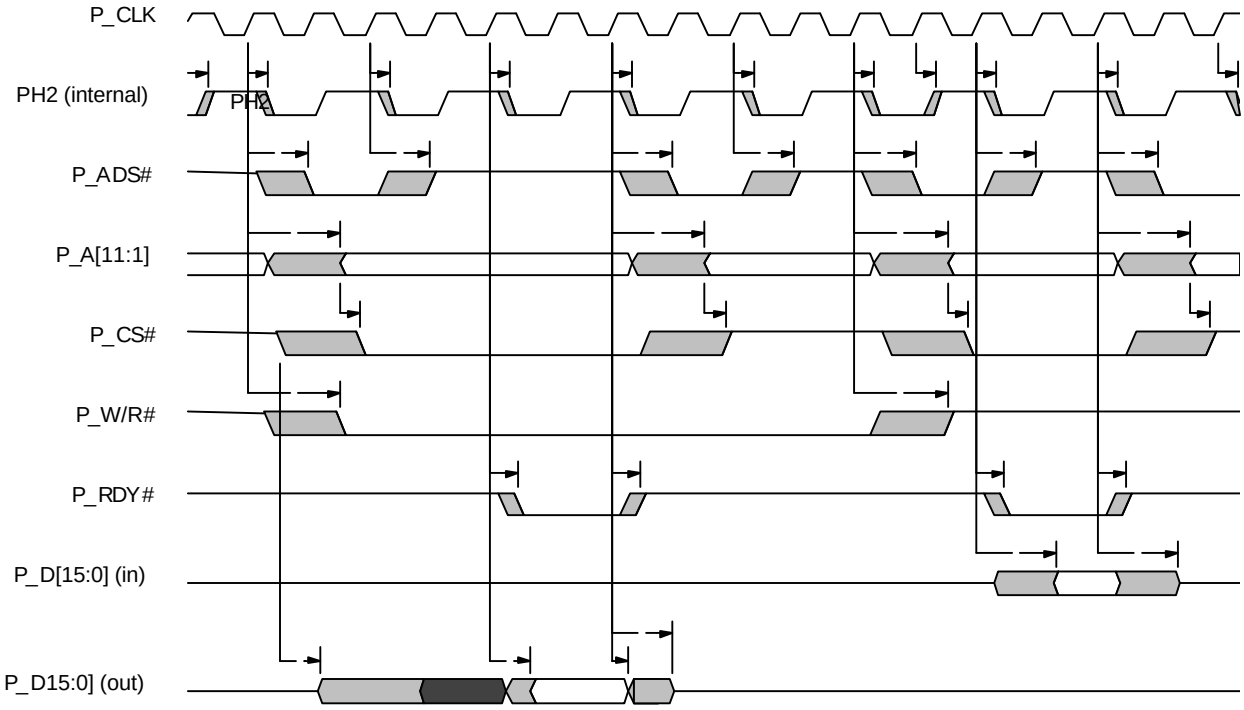
Typical Motorola MPC801 CPU I/O Access Operations

2.3.3 Intel 486 Processor Interface

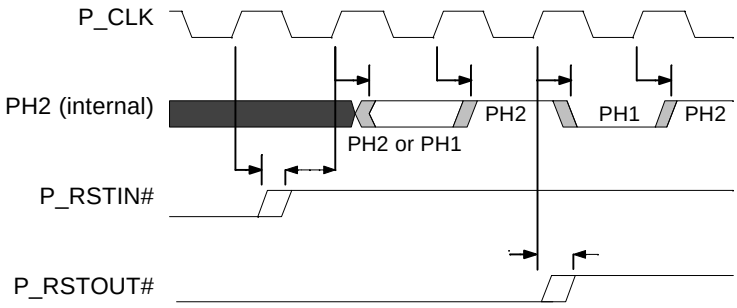


Typical 486 CPU I/O Access Operations

2.3.4 Intel 386 Processor Interface



Typical 386 CPU I/O Access Operations



Internal PH2 Clock Synchronization

Note: See Intel 386 Processor Data Book for more details

2.3.5 Register Map

Note: All 32-bit registers are D-word aligned.

All 16-bit registers are also D-word aligned and right justified.

For the Little Endian CPUs, register offset bit [1,0] are always set to be 00.

For the Big Endian CPUs, register offset bit [1,0] are always set to be 10.

This is a Global Register. CPU is allowed to write the Global Register of all devices by a single operation.

These registers are reserved for system diagnostic usage only.

Register	Description	I/O Offset		Reg. Size	W/R	Note:
		Little Endian	Big Endian			
Device Configuration Registers (DCR)						
GCR	Global Control Register	hF00	hF02	16-bit	W/--	
DCR0	Device Status Register	hF00	hF02	16-bit	--/R	
DCR1	Signature & Revision Register	hF10	hF12	16-bit	--/R	
DCR2	ID Register	hF20	hF22	16-bit	W/R	
DCR3	Local Control Register	hF30	hF32	16-bit	W/R	
DCR4	Interface Status Register	hF40	hF42	16-bit	--/R	
DCR5	Bus Credit Register	hF50	hF52	16-bit	W/R	
Interrupt Controls						
ISR	Interrupt Status Register – Unmasked	hF80	hF82	16-bit	--/R	
ISRM	Interrupt Status Register – Masked	hF90	hF92	16-bit	--/R	
IMSK	Interrupt Mask Register	hFA0	hFA2	16-bit	W/R	
IAR	Interrupt Acknowledgment Register	hFB0	hFB2	16-bit	W/--	
Buffer Memory Interface						
MWAR	Memory Write Address Register – Single Cycle	hE08	hE08	32-bit	W/R	
MRAR	Memory Read Address Register – Single Cycle	hE18	hE18	32-bit	W/R	
MBAR	Memory Address Register – Burst Mode	hE28	hE28	32-bit	W/R	
MWBS	Memory Write Burst Size (in D-words)	hE40	hE42	16-bit	W/R	
MRBS	Memory Read Burst Size (in D-words)	hE50	hE52	16-bit	W/R	
MWDR	Memory Write Data Register	hE68	hE68	32-bit	W/--	
MWDX	Memory Write Data Register – Byte Swapping	hE6C	hE6C	32-bit	W/--	
MRDR	Memory Read Data Register	hE68	hE68	32-bit	--/R	
MRDX	Memory Read Data Register – Byte Swapping	hE6C	hE6C	32-bit	--/R	
Buffers & Stacks Management						
Frame Control Buffers						
FCBBA	Frame Control Buffer – Base Address	hD00	hD02	16-bit	W/R	
FCBA	Frame Control Buffer – Buffer Allocation	hD20	hD22	16-bit	--/R	
FCBR	Frame Control Buffer – Buffer Release	hD20	hD22	16-bit	W/--	
FCBAG	Frame Control Buffer – Buffer Aging Status	hD30	hD32	16-bit	--/R	
FCBSA	Frame Ctrl Buffer Stack – Base Address	hD80	hD82	16-bit	W/R	
FCBSL	Frame Ctrl Buffer Stack – Size Limit	hD90	hD92	16-bit	W/R	
FCBST	Frame Ctrl Buffer Stack – Buffer Low Threshold	hDA0	hDA2	16-bit	W/R	
FCBSS	Frame Ctrl Buffer Stack – Allocation Status	hDB0	hDB2	16-bit	--/R	

Register	Description	I/O Offset		Reg. Size	W/R	Note:
		Little Endian	Big Endian			
Buffers & Stacks Management (Continue)						
Switch Control Buffers						
SCBBA	Switch Control Buffer – Base Address	hC00	hC02	16-bit	W/R	
SCBA	Switch Control Buffer – Buffer Allocation	hC20	hC22	16-bit	--/R	
SCBAG	Switch Control Buffer – Buffer Aging Status	hC30	hC32	16-bit	--/R	
SCBSA	Switch Ctrl Buffer Stack – Base Address	hC80	hC82	16-bit	W/R	
SCBSL	Switch Ctrl Buffer Stack – Size Limit	hC90	hC92	16-bit	W/R	
SCBST	Switch Ctrl Buffer Stack – Buffer Low Threshold	hCA0	hCA2	16-bit	W/R	
SCBSS	Switch Ctrl Buffer Stack – Allocation Status	hCB0	hCB2	16-bit	--/R	
MAC Control Tables						
MCTA	MAC Control Table – Table Allocation	hB20	hB22	16-bit	--/R	
MCTR	MAC Control Table – Table Release	hB20	hB22	16-bit	W/-	
MCTSA	MAC Ctrl Table Stack – Base Address	hB80	hB82	16-bit	W/R	
MCTSS	MAC Ctrl Table Stack – Allocation Status	hBB0	hBB2	16-bit	--/R	
Queue Management						
QSBA	Queue Structure – Base Address	hA00	hA02	16-bit	W/R	
MFTA	Multicast Frame Table – Base Address	hA10	hA12	16-bit	W/R	
CINQ	CPU Input Queue	hA88	hA88	32-bit	W/--	
COTQ	CPU Output Queue	hA88	hA88	32-bit	--/R	
CSQ0	CPU Status Queue – 1st D-word	hA98	hA98	32-bit	--/R	
CSQ1	CPU Status Queue – 2nd D-word	hAA8	hAA8	32-bit	--/R	
CSQ2	CPU Status Queue – 3rd D-word	hAB8	hAB8	32-bit	--/R	
CAM Interface						
CCWR	CAM Command/Data Write Register	h908	h908	32-bit	W/--	
CSRL	CAM Status/Data Read Register Low	h928	h928	32-bit	--/R	
CSRH	CAM Status/Data Read Register High	h938	h938	32-bit	--/R	
HISC Control						
HPCR	HISC Processor Control Register	h980	h982	16-bit	W/R	
HMCL	HISC Micro-Code Loading Port	h998	h998	32-bit	W/R	
HPRC	HISC Priority Control Register	h9B0	h9B2	16-bit	W/R	

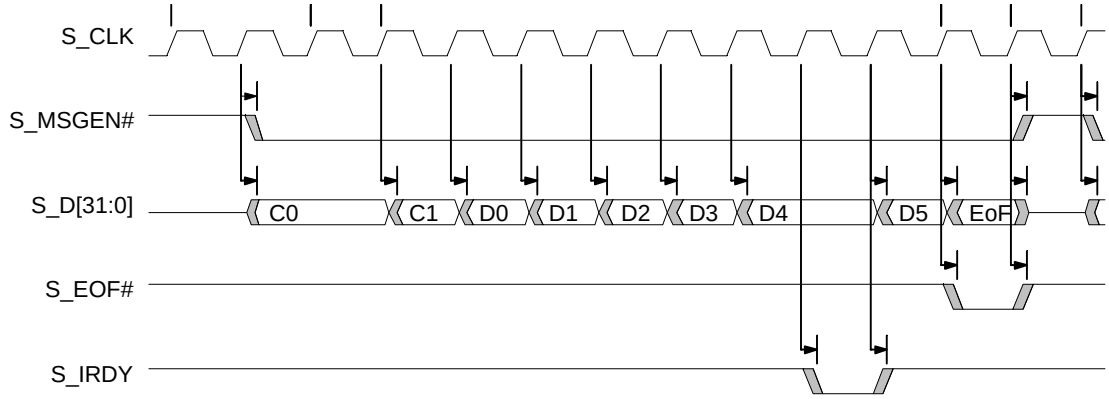
2.4 XpressFlow Bus Interface

- Vertex Networks' optimized *XpressFlow* Bus architecture
- Provides 1G bps switching bandwidth
- Full multi bus master structure
- Allows *XpressFlow* Engine to communicate with Access Controllers via a message passing protocol
  - ◊ Command Messages for passing control information between devices
  - ◊ Data Messages for forwarding an Ethernet frame from receiving port to transmission port
- Built-in intelligent bus load regulator for data traffic balancing
- Provides centralized bus arbitration with two level request priorities
  - ◊ High priority for Data Messages
  - ◊ Low priority for Command Messages

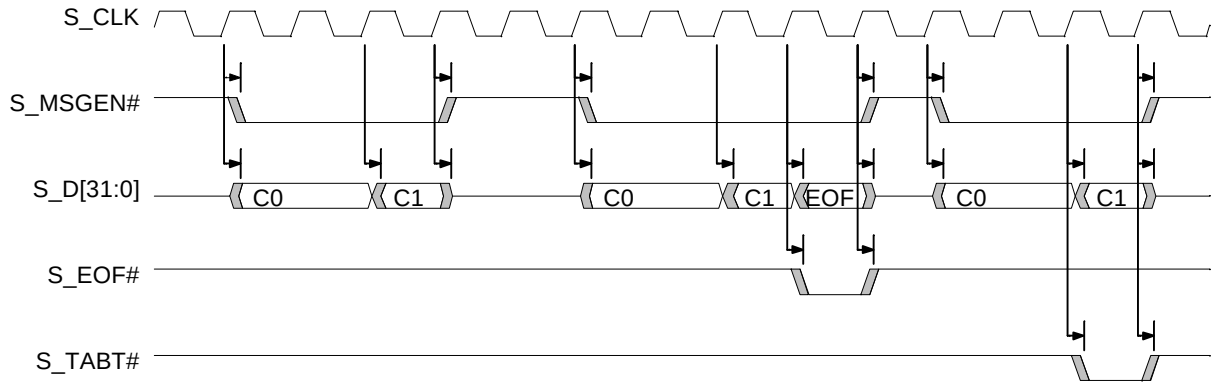
2.4.1 Pin Description

Symbol	Type	Name & Functions
S_D[31:0]	CMOS I/O-TS	***Data Bus Bit*** *[31:0]* – a 32-bit synchronous data bus. **Note:** *During the system RESET period, Data Bit [31:28] are used as Processor Interface Configuration bit [0:3]*
S_MSGEN#	CMOS I/O-TS	***Message Envelope*** – encompasses the entire period of a message transfer. Targets use the leading edge of this signal to detect the beginning of a message transfer, and to decode the message header for the intended target(s).
S_EOF#	CMOS I/O-TS	***End of Frame –*** only used by frame data transfer messages to identify the end of frame condition. This signal is synchronous with the Rx Frame Status word appended to the end of the message.
S_IRDY	CMOS I/O-TS	***Initiator Ready*** – a normal true signal. When negated, it indicates the initiator had asserted wait state(s) in between command words. Target should use this signal as enable signal for latching the data from the bus.
S_TABT#	CMOS I/O-OD	***Target Abort*** – when asserted, the target had aborted the reception of current message on the bus.
S_HPREQ#	CMOS I/O-OD	***High Priority Request*** – indicates one or more Bus Requester is requesting for high priority message transfer.
S_REQ[8:1]#	CMOS Input	***Bus Request [8:1]*** – Bus Request signals from Access Controllers to Bus Access Arbitrator in *XpressFlow* Engine
S_GNT[8:1]#	CMOS Output	***Bus Grant [8:1]*** – Bus Grant signals from Bus Arbitrator to Bus Requesters
S_OVLD#	CMOS Output	***Bus Overload*** – when asserted all data forwarding bus bandwidth has been allocated. Cannot support additional load for data forwarding traffic
S_CLK	CMOS Input	***XpressFlow Bus Clock*** – 33MHz system clock

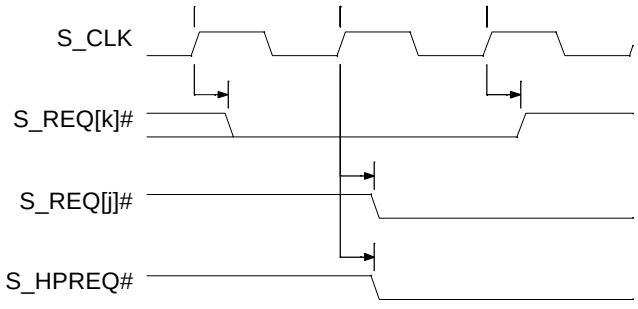
2.4.2 Bus Cycle Waveforms



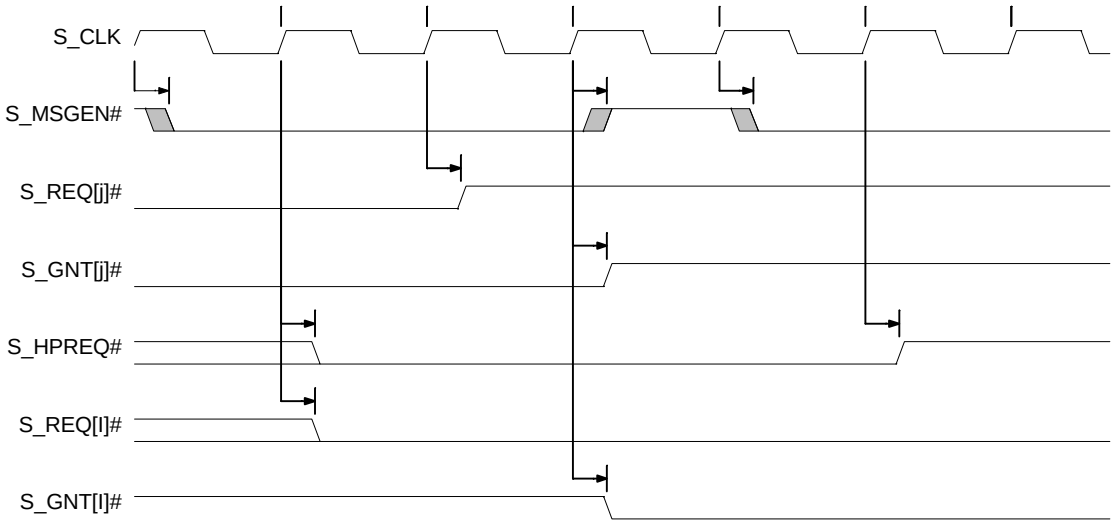
XpressFlow Bus Data Transfer Cycle



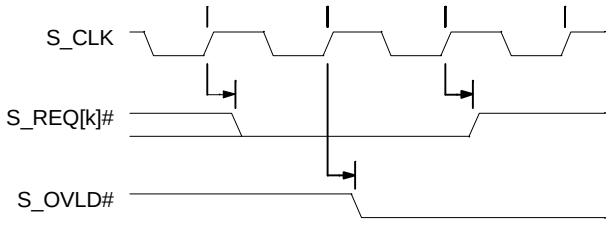
Other XpressFlow Bus Cycles



High Priority Request pre-empts the low priority request



XpressFlow Bus arbitration



Bus Overload pre-empts the data transfer request

2.5 Test Pins

Symbol	Type	Name & Functions
TEST	CMOS I/O	***Test Mode Selection & Test Output*** – Set Test Mode upon Reset, and provides test status output during test mode

3 DC SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 C to +150 C
Operating Temperature	0 C to +70 C
Supply Voltage V_{DD} with Respect to V_{SS}	+3.0 V to +3.6 V
Voltage on 5V Tolerant Input Pins	-0.5 V to (V_{DD} + 2.5 V)
Voltage on Other Pins	-0.5 V to (V_{DD} + 0.3 V)

Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

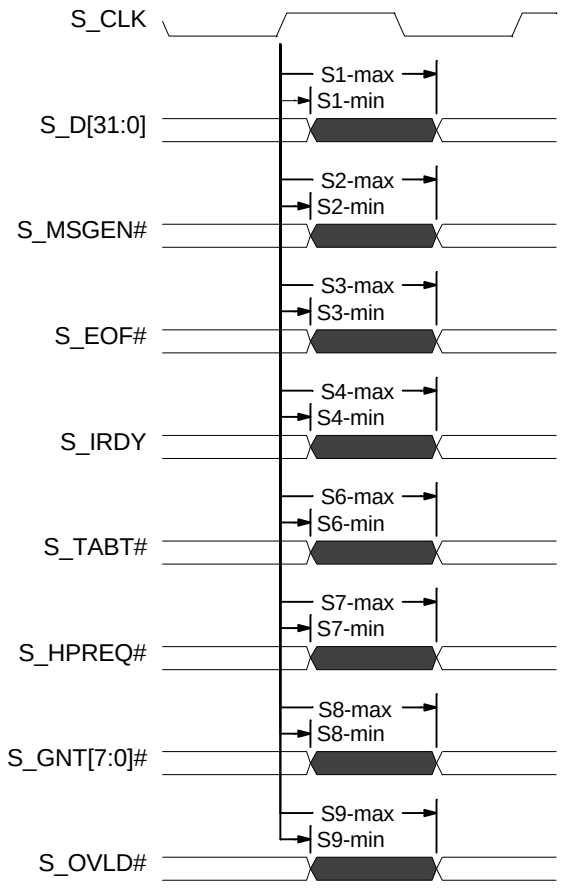
3.2 DC CHARACTERISTICS

V_{DD} = 3.0 V to 3.6 V; $T_{AMBIENT}$ = 0 C to +70 C

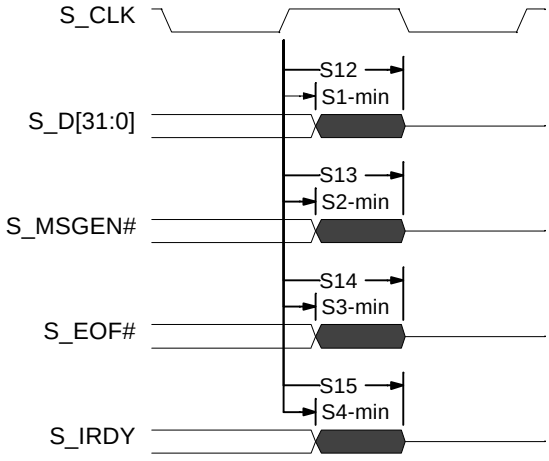
Symbol	Parameter Description	Preliminary			Unit
		Min	Typ	Max	
f_{osc}	Frequency of Operation (-40)	20		40.0000	MHz
	Frequency of Operation (-50)	20		50.0000	MHz
	Frequency of Operation (-66)	20		66.6666	MHz
I_{DD}	Supply Power – @ 33.3333 MHz (V_{DD} =3.3 V)		300	500	mA
	Supply Power – @ 40 MHz (V_{DD} =3.3 V)		300	500	mA
	Supply Power – @ 50 MHz (V_{DD} =3.3 V)		300	500	mA
$V_{OH-CMOS}$	Output High Voltage (CMOS) I_{OH} = -1.0 mA	V_{DD} - 0.5			V
$V_{OL-CMOS}$	Output Low Voltage (CMOS) I_{OL} = 1.0 mA			0.45	V
V_{OH-TTL}	Output High Voltage (TTL) I_{OH} = -1.0 mA	2.4			V
V_{OL-TTL}	Output Low Voltage (TTL) I_{OL} = 1.0 mA			0.45	V
$V_{IH-CMOS}$	Input High Voltage (CMOS)	VDD x 70%		V_{DD} + 0.3	V
$V_{IL-CMOS}$	Input Low Voltage (CMOS)	-0.5		VDD x 30%	V
V_{IH-TTL}	Input High Voltage (TTL)	2.0		V_{DD} + 0.3	V
V_{IL-TTL}	Input Low Voltage (TTL)	-0.3		+0.8	V
V_{IH-5VT}	Input High Voltage (TTL 5V tolerant)	2.0		V_{DD} + 2.5	V
V_{IL-5VT}	Input Low Voltage (TTL 5V tolerant)	-0.3		+0.8	V
I_{LI}	Input Leakage Current (0.1 V V_{IN} V_{DD}) (all pins except those with internal pull-up/pull-down resistors)			10	A
I_{LO}	Output Leakage Current (0.1 V V_{OUT} V_{DD})			15	A
I_{IH}	Input Leakage Current V_{IH} = V_{DD} - 0.1 V (pins with internal pull-down resistors)			60	A
I_{IL}	Input Leakage Current V_{IL} = 0.1 V (pins with internal pull-up resistors)			-60	A
C_{IN}	Input Capacitance			8	pF
C_{OUT}	Output Capacitance			8	pF
$C_{I/O}$	I/O Capacitance			10	pF

4 AC SPECIFICATION

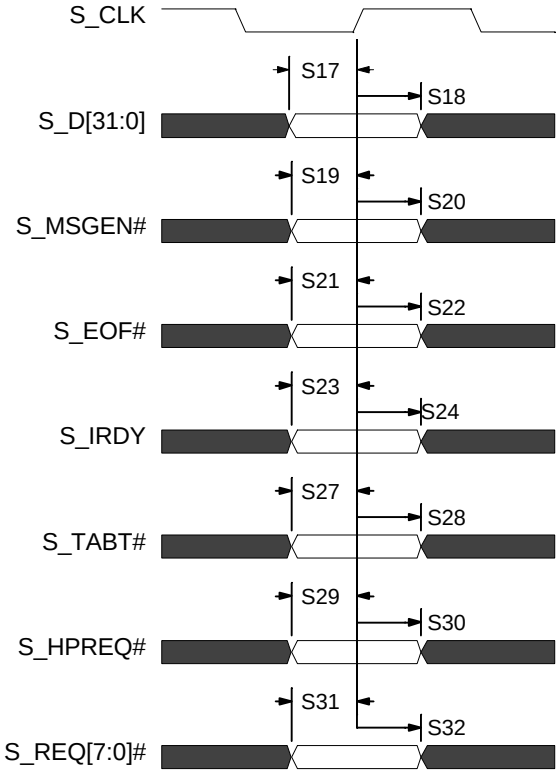
4.1 XpressFlow Bus Interface:



XpressFlow Bus Interface – Output valid delay timing



XpressFlow Bus Interface – Output float delay timing

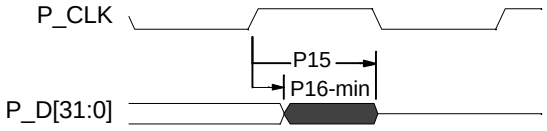


XpressFlow Bus Interface – Input setup and hold timing

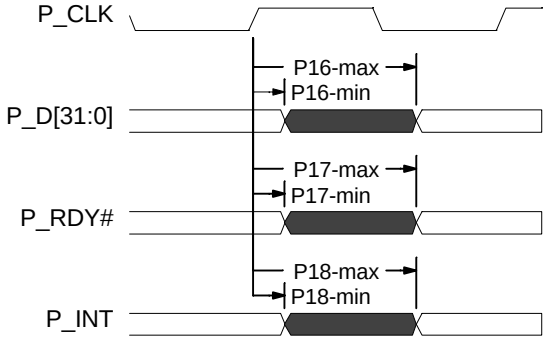
Symbol	Parameter	-40		-50		-66		
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Note:
S1	S_D[31:0] output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S2	S_MSGEN# output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S3	S_EOF# output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S4	S_IRDY output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S6	S_TABT# output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S7	S_HPREQ# output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S8	S_GNT[7:0]# output valid delay	6	14	5	11	4	8.5	C_L = 20pf
S9	S_OVLD# output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S12	S_D[31:0] output float delay		18		15		12	
S13	S_MSGEN# output float delay		18		15		12	
S14	S_EOF# output float delay		18		15		12	
S15	S_IRDY output float delay		18		15		12	
S17	S_D[31:0] input set-up time	2		1.5		1		
S18	S_D[31:0] input hold time	5.5		4.5		3.5		
S19	S_MSGEN# input set-up time	2		1.5		1		
S20	S_MSGEN# input hold time	5.5		4.5		3.5		
S21	S_EOF# input set-up time	2		1.5		1		
S22	S_EOF# input hold time	5.5		4.5		3.5		
S23	S_IRDY input set-up time	2		1.5		1		
S24	S_IRDY input hold time	5.5		4.5		3.5		
S27	S_TABT# input set-up time	5.5		4.5		3.5		
S28	S_TABT# input hold time	5.5		4.5		3.5		
S29	S_HPREQ# input set-up time	4.5		3.5		2.5		
S30	S_HPREQ# input hold time	5.5		4.5		3.5		
S31	S_REQ[7:0]# input set-up time	6		5		4		
S32	S_REQ[7:0]# input hold time	5.5		4.5		3.5		

AC Characteristics -- XpressFlow Bus Interface

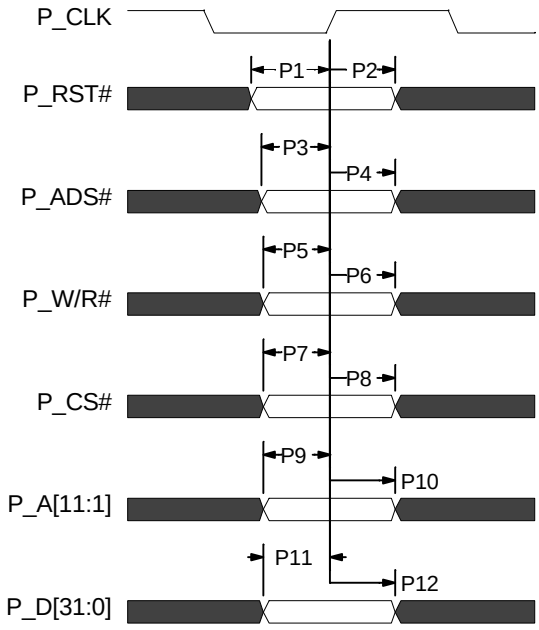
4.2 CPU Bus Interface:



CPU Bus Interface – Output float delay timing



CPU Bus Interface – Output valid delay timing



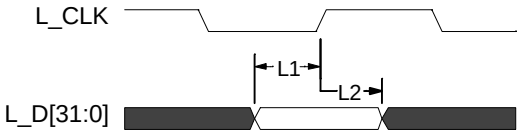
CPU Bus Interface – Input setup and hold timing

Symbol	Parameter	-40		-50		-66		Note:
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	
P1	P_RST# input setup time	13		10		8		
P2	P_RST# input hold time	3.5		2.5		2		
P3	P_ADS# input set-up time	13		10		8		
P4	P_ADS# input hold time	3.5		2.5		2		
P5	P_W/R# input set-up time	13		10		8		
P6	P_W/R# input hold time	3.5		2.5		2		
P7	P_CS# input set-up time	13		10		8		
P8	P_CS# input hold time	3.5		2.5		2		
P9	P_A[11:1] input set-up time	13		10		8		
P10	P_A[11:1] input hold time	3.5		2.5		2		
P11	P_D[31:0]# input set-up time	13		10		8		
P12	P_D[31:0]# input hold time	3.5		2.5		2		
P15	P_D[31:0]# output float delay		17		13		10	
P16	P_D[31:0]# # output valid delay		17		13		10	C_L = 60pf
P17	P_RDY# output valid delay		13		10		8	C_L = 60pf
P18	P_INT# output valid delay		8.5		6.5		5	C_L = 20pf

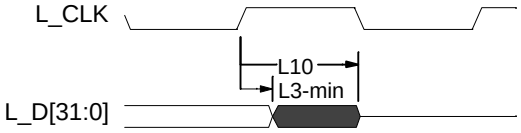
AC Characteristics -- CPU Bus Interface

4.3 Local Memory Interface:

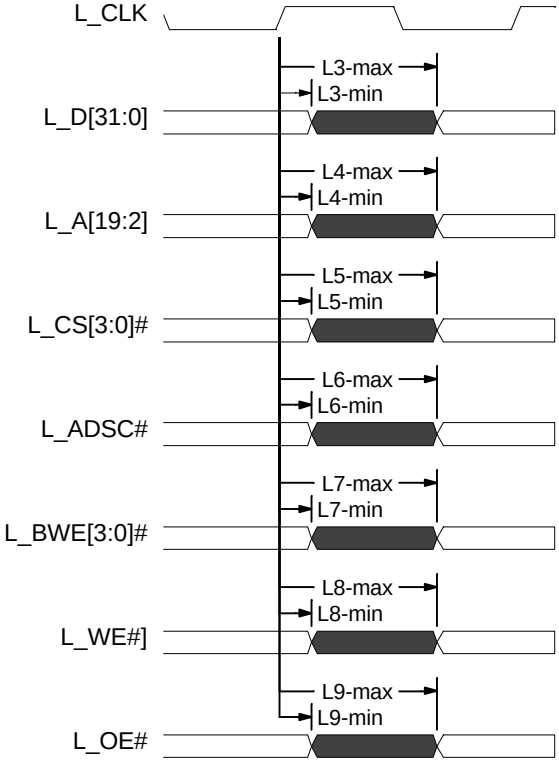
Local Memory Interface:



Local Memory Interface – Input setup and hold timing



Local Memory Interface – Output float delay timing

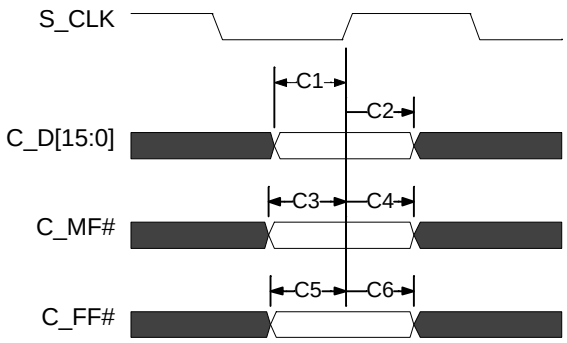


Local Memory Interface – Output valid delay timing

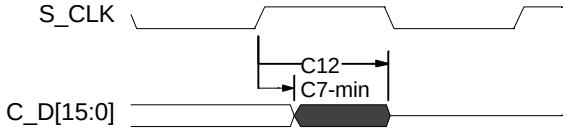
Symbol	Parameter	-40		-50		-66		Note:
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	
L1	L_D[31:0]# input set-up time	6.5		5.5		4		
L2	L_D[31:0]# input hold time	3		2.5		2		
L3	L_D[31:0]# output valid delay	5	17	4	13	3	10	C_L = 30pf
L4	L_A[19:2] output valid delay	5	17	4	13	3	10	C_L = 30pf
L6	L_ADSC# output valid delay	5	17	4	13	3	10	C_L = 30pf
L7	L_BWE[3:0]# output valid delay	5	17	4	13	3	10	C_L = 30pf
L8	L_WE# output valid delay	5	17	4	13	3	10	C_L = 10pf
L9	L_OE# output valid delay	5	17	4	13	3	10	C_L = 10pf
L10	L_D[31:0]# output float delay		22		18		14	

AC Characteristics – Local Memory Interface

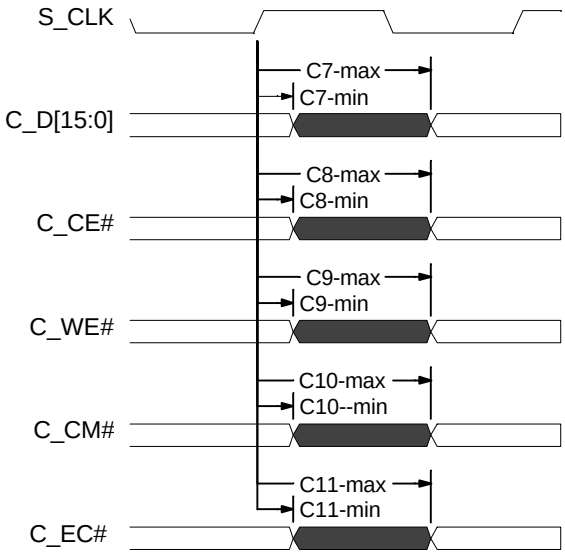
4.4 CAM Memory Interface:



CAM Memory Interface –
Input setup and hold timing



CAM Memory Interface –
Output float delay timing



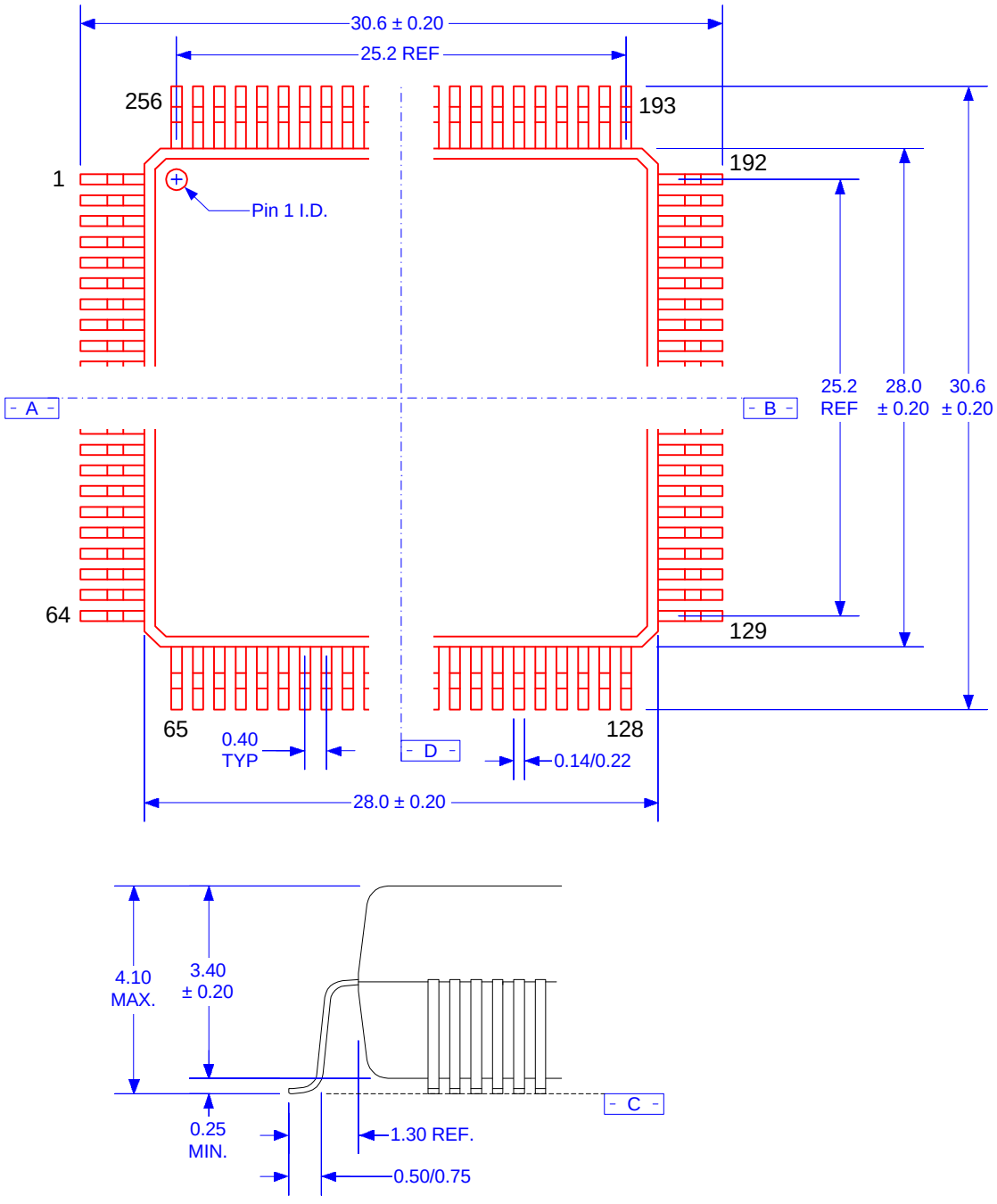
CAM Memory Interface –
Output valid delay timing

Symbol	Parameter	-40		-50		-66		Note:
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	
C1	C_D[15:0]# input set-up time	4.5		4		5		
C2	C_D[15:0]# input hold time	1.5		1.5		2		
C3	C_MF# input set-up time	4.5		4		5		
C4	C_MF# input hold time	1.5		1.5		2		
C5	C_FF# input set-up time	4.5		4		5		
C6	C_FF# input hold time	1.5		1.5		2		
C7	C_D[15:0]# output valid delay	5	18	4	15	6	20	
C8	C_CE# output valid delay	5	18	4	15	6	20	
C9	C_WE# output valid delay	5	18	4	15	6	20	
C10	C_CM# output valid delay	5	18	4	15	6	20	
C11	C_CE# output valid delay	5	18	4	15	6	20	
C12	C_D[16:0]# output float delay		13		10		15	

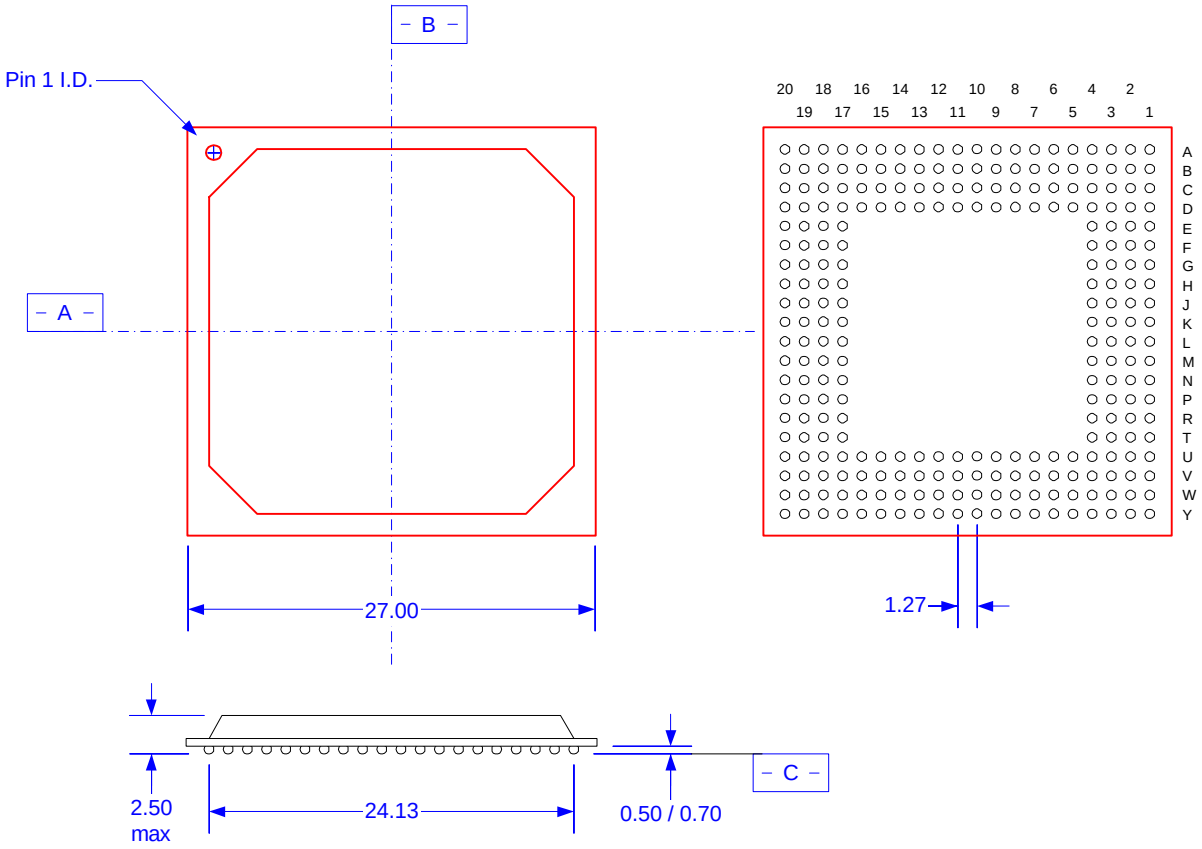
AC Characteristics – CAM Memory Interface

5 PACKAGING INFORMATION

5.1 256-PIN PQFP



5.2 256- Pin BGA



Ordering Information

Part Number	Description	Identification	Vertex Networks Use	Revision
SC220	XpressFlow Switch Engine	**C 0 B**	**TAV**	**rrr**

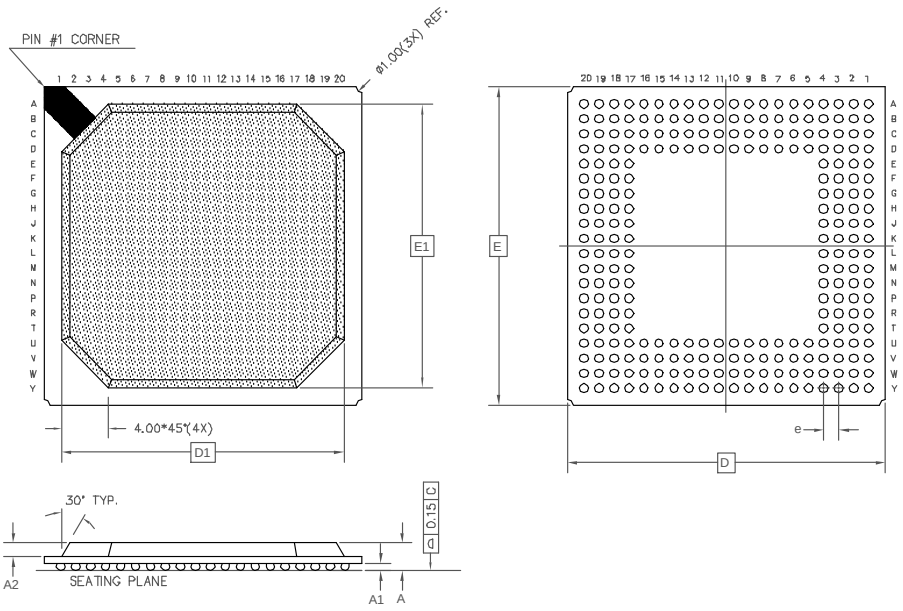
Environmental – *C = Commercial*
I = Industrial

Speed grade - *0 = 40 MHz*
5 = 50 MHz
6 = 66 MHz

Package - *B = BGA*
P= PQFP

Revision - *001 = Rev.1*
For latest revision, leave blank

VERTEX NETWORKS
16842 Von Karman Ave, Suite 250
Irvine, CA 92606-4950
Tel. 1-714-252-8880, FAX: 1-714-252-8868
Web Site: www.vertex-networks.com



DIMENSION	MIN	MAX
A	2.20	2.46
A1	0.50	0.70
A2	1.17 REF	
D	26.80	27.20
D1	24.00 REF	
E	26.80	27.20
E1	24.00 REF	
b	0.60	0.90
e	1.27	
N	256	
Conforms to JEDEC MS - 034		

1. CONTROLLING DIMENSIONS ARE IN MM
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER
3. PRIMARY DATUM -C- AND SEATING PLANE
   ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. N IS THE NUMBER OF SOLDER BALLS
5. NOT TO SCALE.
6. SUBSTRATE THICKNESS IS 0.56 MM

ISSUE	1			
ACN	213983			
DATE	3Feb03			
APPRD.				

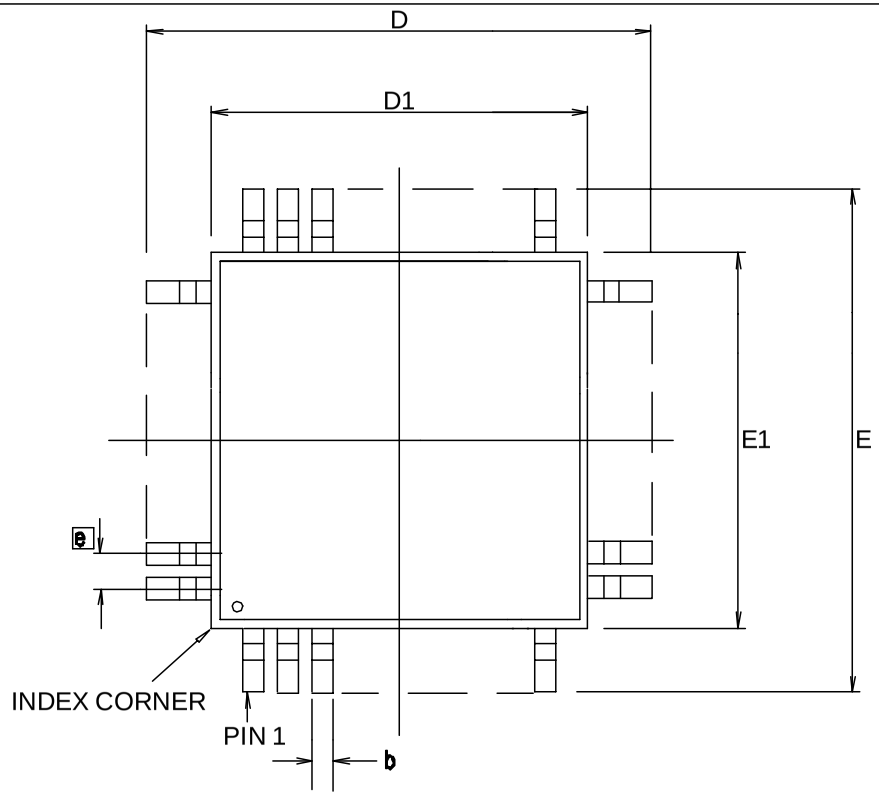
ZARLINK SEMICONDUCTOR

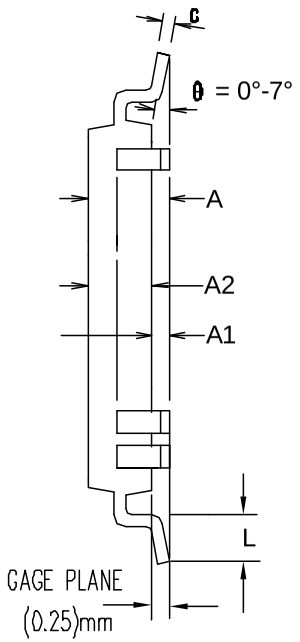
Previous package codes: BP / G

Package Code GA

Package Outline for 256 Ball PBGA (27x27x2.33mm)

GPD00827





Symbol	Control Dimensions in millimetres		
	MIN	Nominal	MAX
A	–	–	4.10
A1	0.25	–	–
A2	3.20	3.32	3.60
D	30.60 BSC		
D1	28.00 BSC		
E	30.60 BSC		
E1	28.00 BSC		
L	0.45	0.60	0.75
e	0.40 BSC		
b	0.13	0.16	0.23
c	0.09	0.15	0.20
θ	0°	–	7°
ccc	–	0.08	–
N	256		
ND	64		
NE	64		

Conforms to JEDEC MO-143

Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.

ISSUE	1			
ACN	213985			
DATE	3Feb03			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes: GP / L

Package Code QB

Package Outline for 256 Lead MQFP (28x28x3.32mm) + 2.6 mm (footprint)

GPD00829

For more information about all Zarlink products visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE