HYUNDAI SEMICONDUCTOR

HY62C256

32K×8-Bit CMOS SRAM

M231202B-MAY92

T-46-23-13

DESCRIPTION

The HY62C256 is a high speed low power, 32,768 words by 8-bit CMOS static RAM fabricated using HYUNDAI's high performance twin tub CMOS process. This high reliability process coupled with innovative circuit design techniques. yields maximum access time of 85ns.

The HY62C256 has a data retention mode that guarantees data will remain valid at a minimum power supply voltage of 2.0 volt.

Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY62C256 family.

FEATURES

- High speed — 85/100/120/150 ns (max.)
- Low power consumption
  - 175mW typical operating
  - 15 μW typical standby (L-version)
- Battery back up (L-version)
  - 2 volt data retention
- Fully static operation
  - No clock or refresh required
- All inputs and outputs directly TTL compatible
- Tri-state output
- High reliability 28 pin 600 mil P-DIP and 330 mil SOP

		HY62C256-85	HY62C256-10	HY62C256-12	HY62C256-15
Maximum Access Time (ns)		85	100	120	150
Maximum Average Operating Current (mA)		70	70	70	70
Maximum Standby Current (mA)		1.0	1.0	1.0	1.0
	L	0.1	0.1	0.1	0.1

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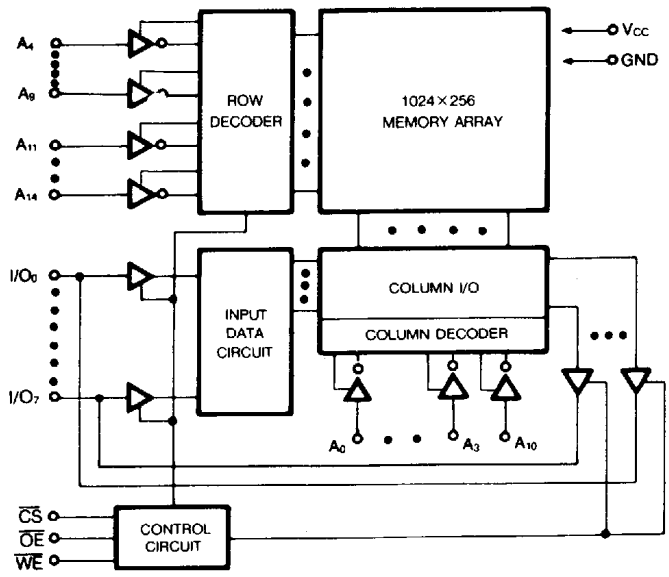
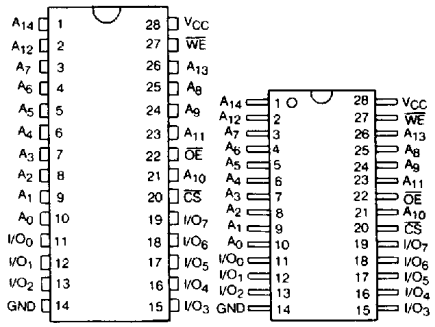
BLOCK DIAGRAM



PIN CONNECTIONS



DIP SOP

PIN NAMES

A_0-A_{14}	ADDRESS INPUT
I/O_0-I/O_7	DATA INPUT / OUTPUT
$\overline{CS}$	CHIP SELECT
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
V_{CC}	POWER
GND	GROUND

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}, V_{IN}, $V_{I/O}$	Power Supply, Input, Input/Output Voltage	−0.5[2] to 7.0	V
T_{BIAS}	Temperature Under Bias	−10 to 125	°C
T_{STG}	Storage Temperature	−65 to 150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA

NOTES :
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended may affect reliability.
2. -3.5V for 20ns pulse.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5[1]	–	0.8	V

NOTE :
1. −3.5V for 20 ns pulse.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION
Standby	H	X	X	High-Z
output Disabled	L	H	H	High-Z
Read	L	L	H	D_{OUT}
Write	L	X	L	D_{IN}

NOTE :
1. X : H or L

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DC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		HY62C56			UNIT
				MIN.	TYP.(1)	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{IN}=GND to V_{CC}		–	–	2	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to V_{CC}		–	–	2	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA		–	40	70	mA
I_{CC1}	Average Operating Current	$\overline{CS}$=V_{IL}, Min. Duty Cycle=100%		–	35	70	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$=V_{IH}		–	–	3	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC}−0.2V,		–	–	1.0	mA
			L	–	3	100	μA
V_{OL}	Output Low Voltage	I_{OL}=4mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−1.0mA		2.4	–	–	V

NOTE :
1. V_{CC}=5V, T_A=25°C

AC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A=0°C to 70°C)

READ CYCLE

SYMBOL	PARAMETER	HY62C256-85		HY62C256-10		HY62C256-12		HY62C256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	120	–	150	–	ns
t_{AA}	Address Access Time	–	85	–	100	–	120	–	150	ns
t_{ACS}	Chip Select Access Time	–	85	–	100	–	120	–	150	ns
t_{CLZ}	Chip Selection to Output in Low-Z	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	45	–	50	–	60	–	70	ns
t_{OLZ}	Output Enable to Output in Low-Z	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Deselection to Output in High-Z	0	30	0	35	0	40	0	50	ns
t_{OHZ}	Output Disable to Output in High-Z	0	30	0	35	0	40	0	50	ns
t_{OH}	Output Hold from Address Change	5	–	10	–	10	–	10	–	ns

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WRITE CYCLE

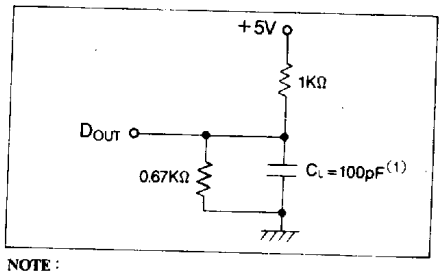
SYMBOL	PARAMETER	HY62C256-85		HY62C256-10		HY62C256-12		HY62C256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	120	–	150	–	ns
t_{CW}	Chip Selection to End of Write	75	–	80	–	85	–	100	–	ns
t_{AW}	Address Valid to End of Write	75	–	80	–	85	–	100	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	70	–	90	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High-Z	0	30	0	35	0	40	0	50	ns
t_{WHZ}	Write to Output in High-Z	0	30	0	35	0	40	0	50	ns
t_{DW}	Data to Write Time Overlap	40	–	40	–	50	–	60	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write	5	–	10	–	10	–	10	–	ns

AC TEST CONDITIONS

(T_A=0°C to 70°C)

Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD



NOTE :
1. Including scope and the Jig.

CAPACITANCE

(T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	10	pF

NOTE :
1. This parameter is sampled and not 100% tested.

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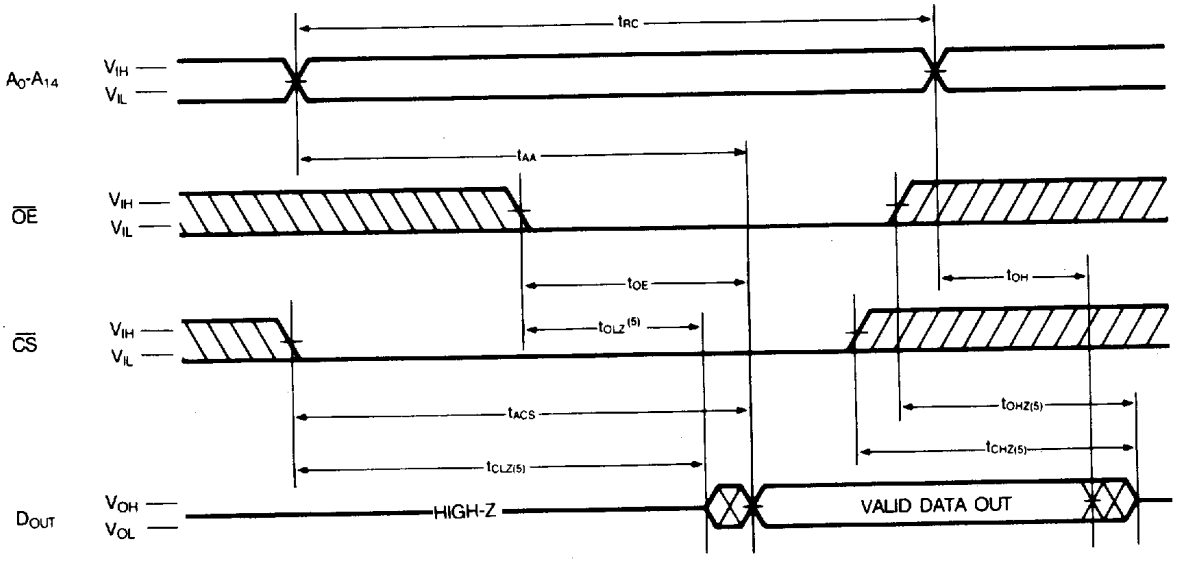
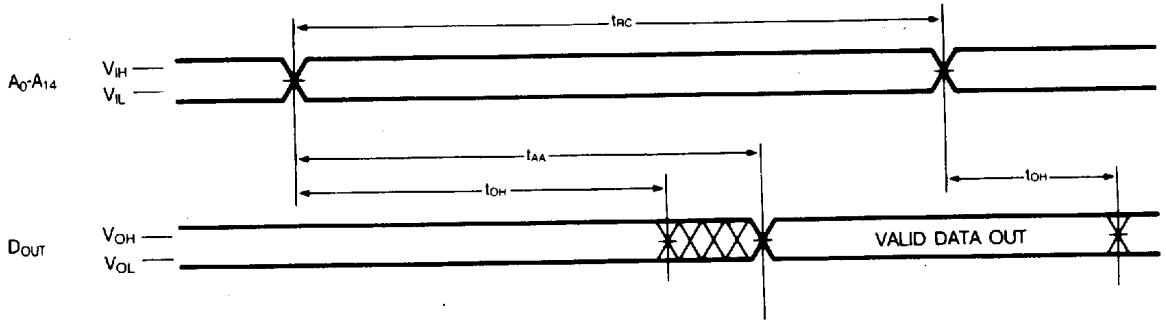
TIMING DIAGRAMS

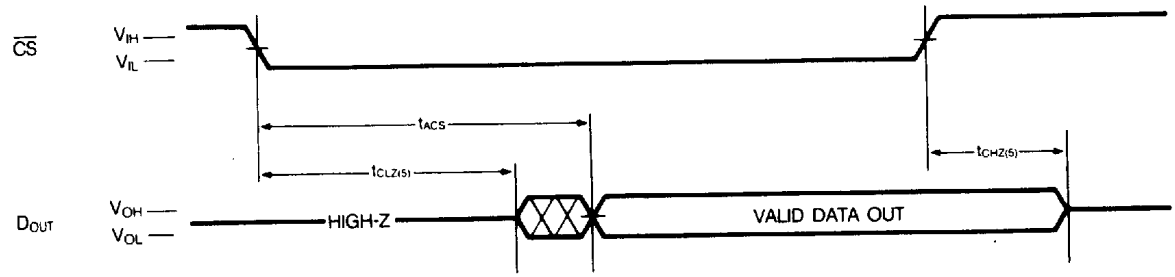
READ CYCLE 1[1]



READ CYCLE 2[1, 2, 4]

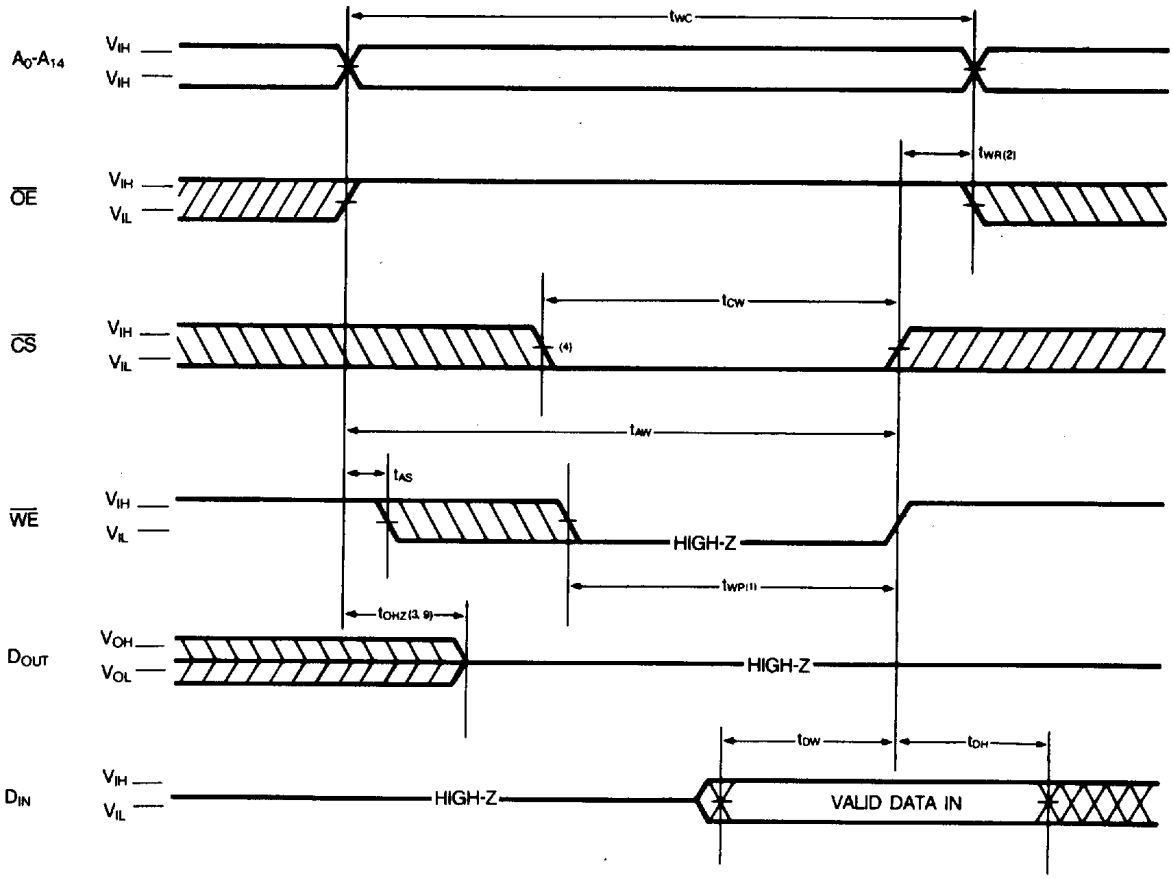


READ CYCLE 3[1, 3, 4]



NOTES :
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Addresses are valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE 1



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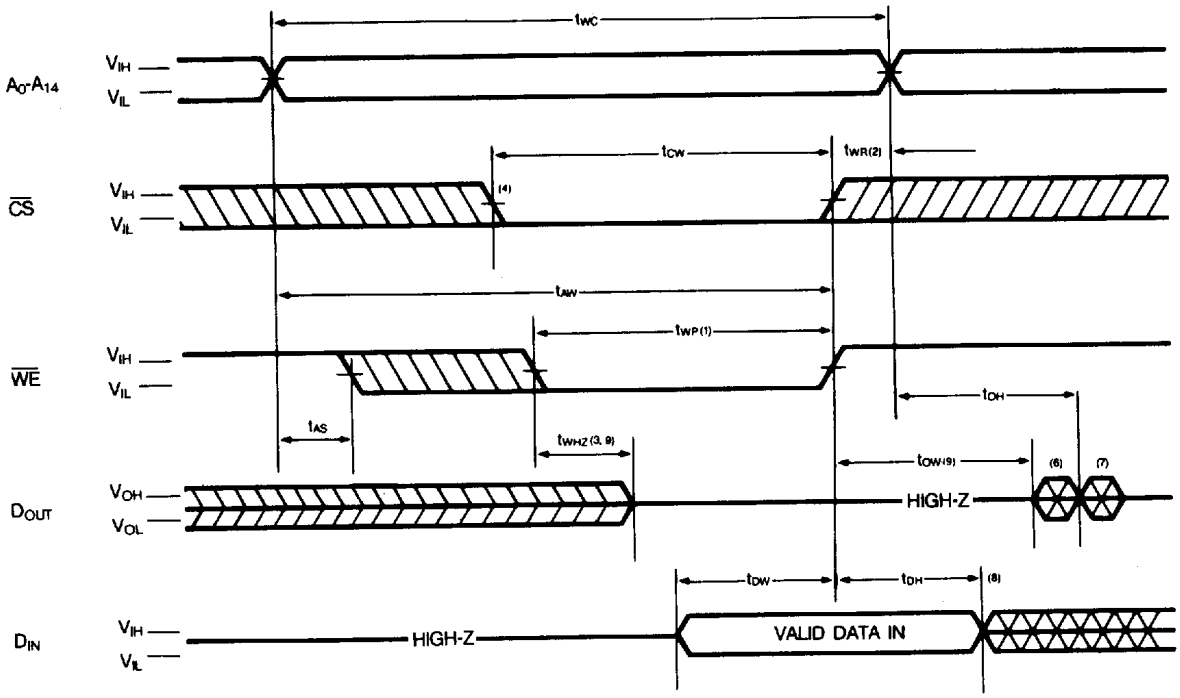
WRITE CYCLE 2(5)



NOTES :
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high at the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE}=V_{IL}$).
6. D_{OUT} is the same phase of write data of this write cycle.
7. D_{OUT} is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

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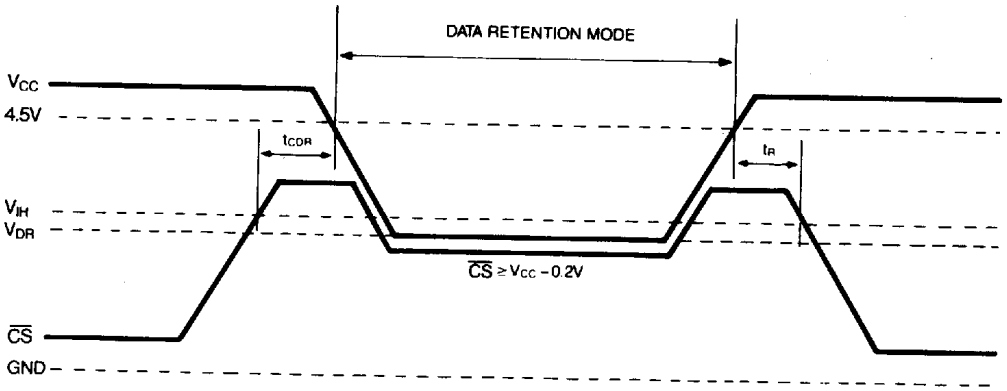
DATA RETENTION CHARACTERISTICS[1]

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DR}	Data Retention Supply Voltage	V_{IN}=0 to V_{CC}, $\overline{CS} \geq V_{CC}-0.2V$	2.0	–	–	V
I_{CCDR}	Data Retention Current	V_{CC}=3.0V, V_{IN}=0 to V_{CC}, $\overline{CS} \geq V_{CC}-0.2V$	–	2	50	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	–	–	ns
t_R	Operating Recovery Time		t_{RC}[2]	–	–	ns

NOTES :
1. These characteristics are guaranteed for L-version.
2. t_{RC}=Read Cycle Time

DATA RETENTION TIMING DIAGRAM



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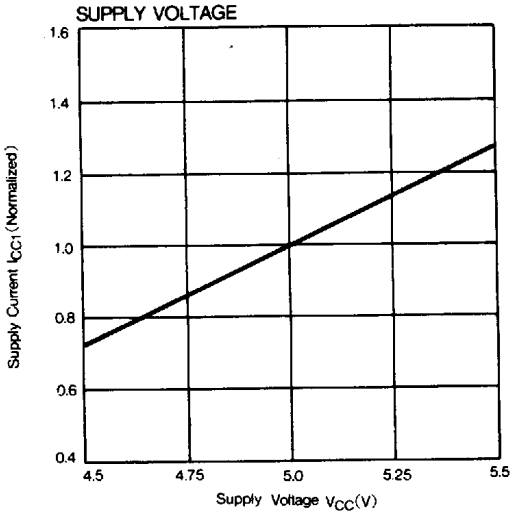
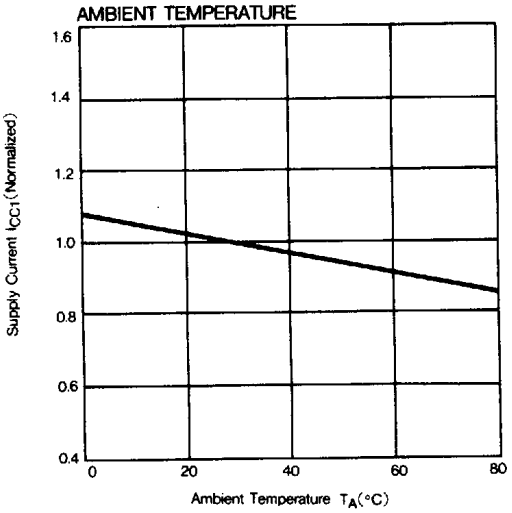
ELECTRICAL CHARACTERISTIC CURVES

(V_{CC}=5V, T_A=25°C , unless otherwise noted)

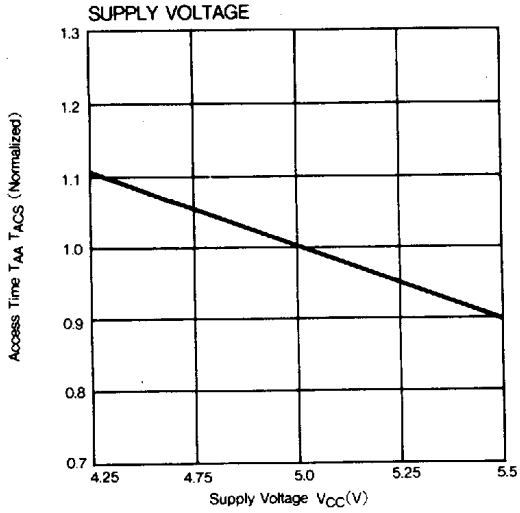
SUPPLY CURRENT vs. SUPPLY VOLTAGE



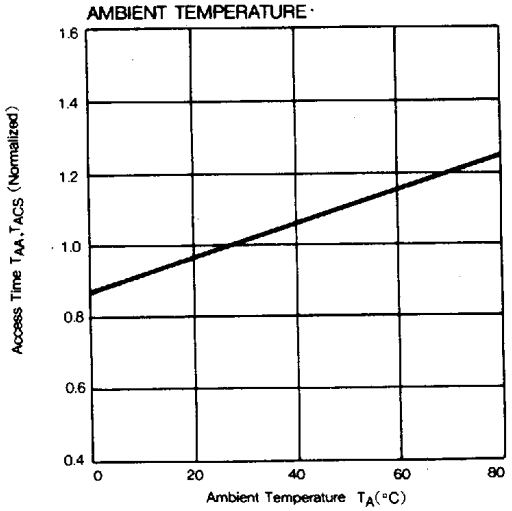
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



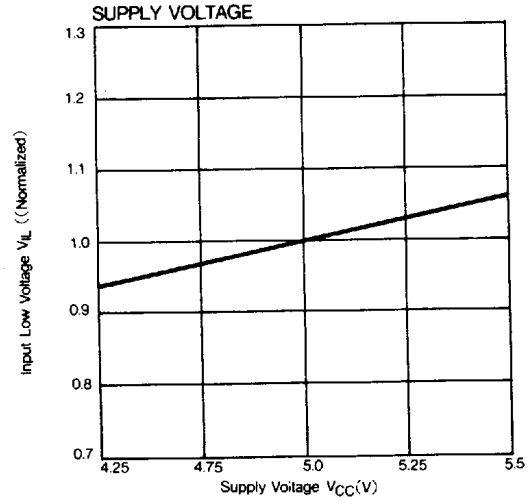
ACCESS TIME vs. SUPPLY VOLTAGE



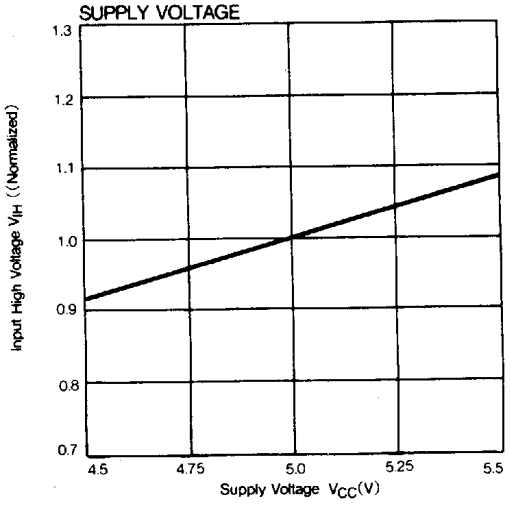
ACCESS TIME vs. AMBIENT TEMPERATURE



INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



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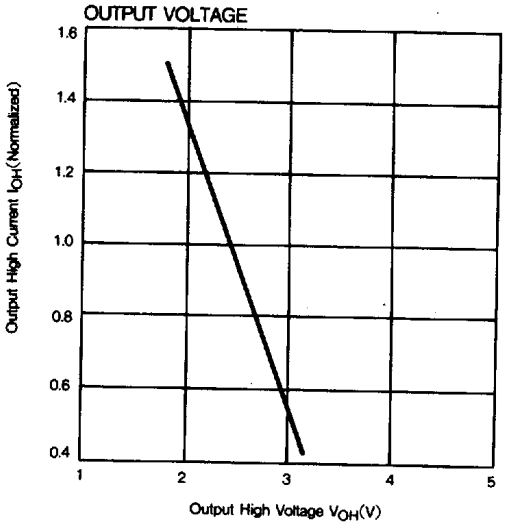
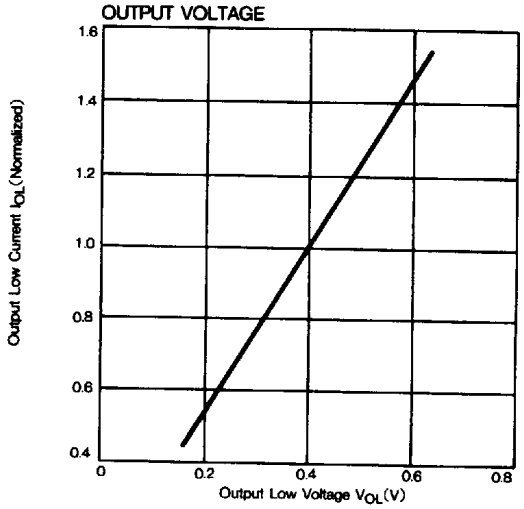
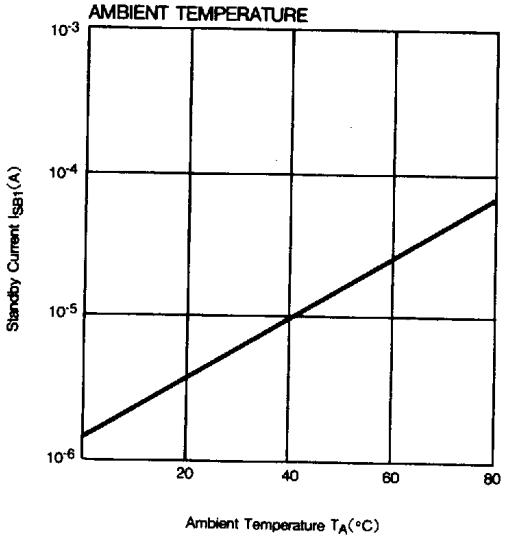
OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE

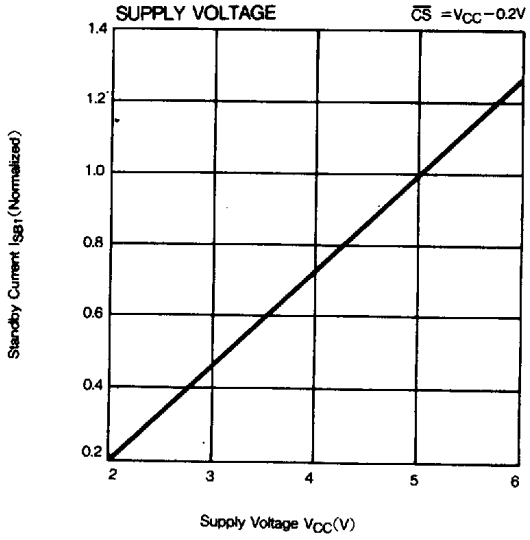


STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE

$\overline{CS}$ = V_{CC} − 0.2V



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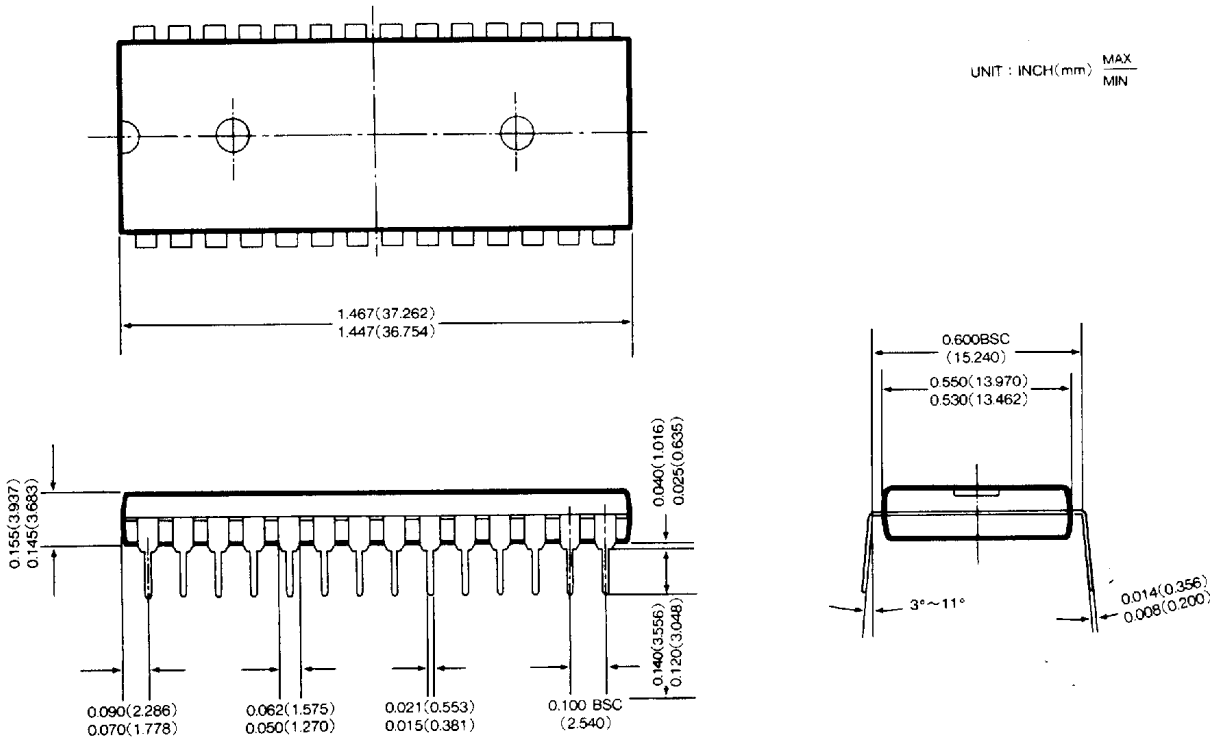
PACKAGE INFORMATION

• 28 PIN PLASTIC DUAL IN LINE PACKAGE−600MIL



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• 28 PIN SMALL OUTLINE PACKAGE−330MIL