THC63LVD104S

112MHz 30Bits Color LVDS Receiver

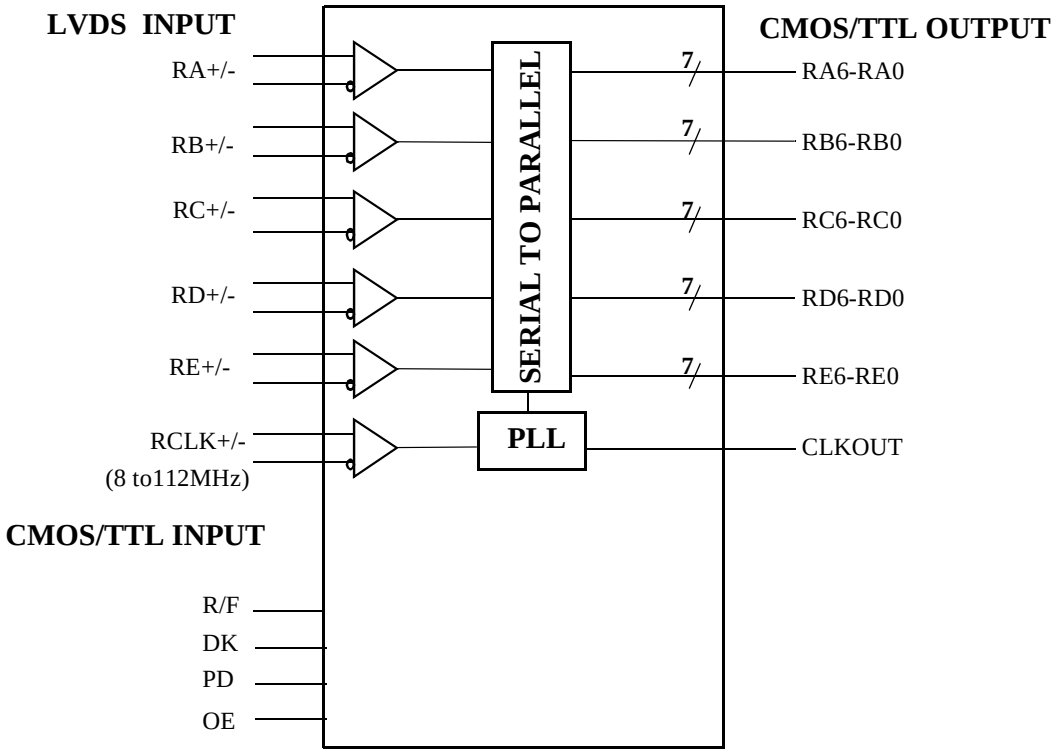
General Description

The THC63LVD104S receiver is designed to support pixel data transmission between Host and Flat Panel Display from NTSC up to SXGA resolutions. The THC63LVD104S converts the LVDS data streams back into 35bits of CMOS/TTL data with rising edge or falling edge clock for convenient with a variety of LCD panel controllers.At a transmit clock frequency of 112MHz, 30bits of RGB data and 5bits of timing and control data (HSYNC,VSYNC,DE,CNTL1,CNTL2) are transmitted at an effective rate of 784Mbps per LVDS channel.Using a 112MHz clock, the data throughput is 490Mbytes per second.

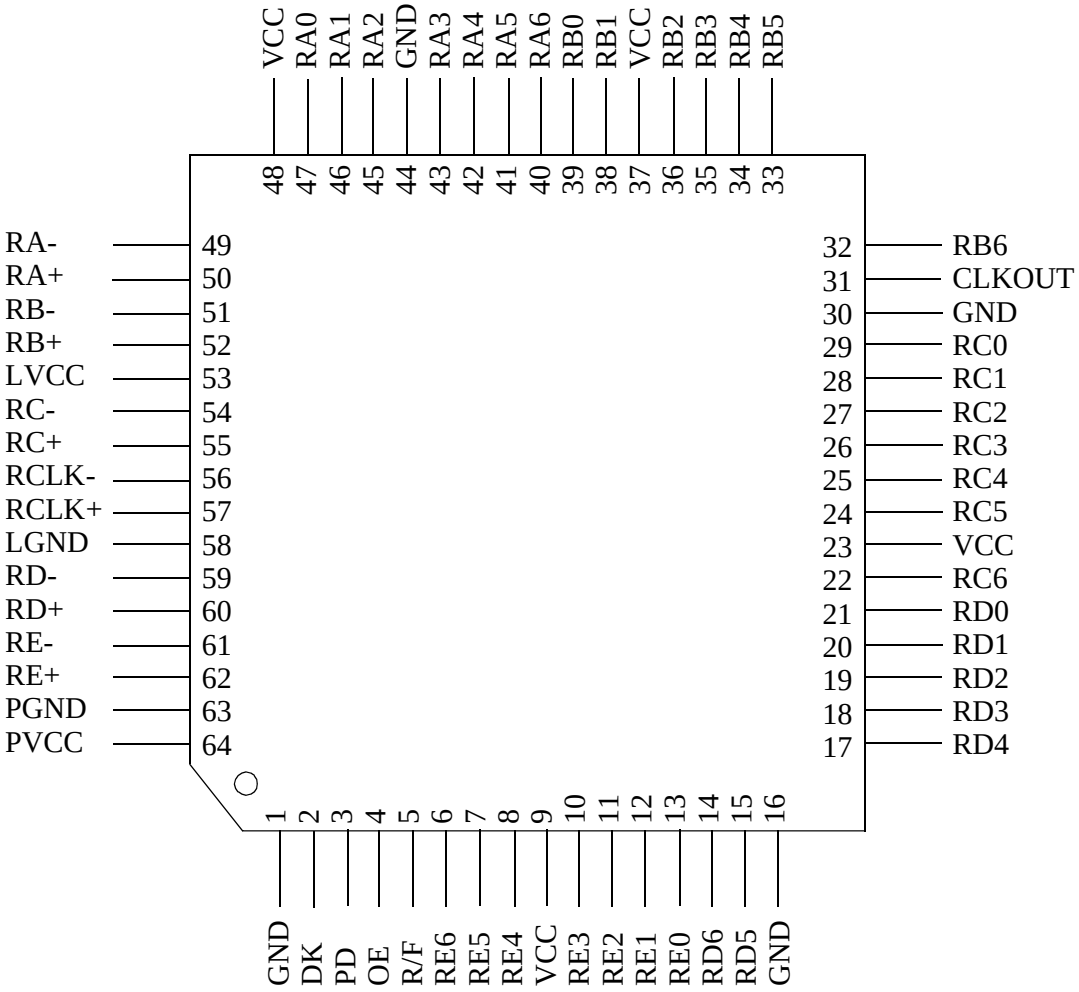
Features

- Wide dot clock range: 8-112MHz suited for NTSC, VGA, SVGA, XGA, and SXGA
- PLL requires no external components
- 50% output clock duty cycle
- TTL clock edge and position programmable(3 step)
- Power down mode
- Low power single 2.5V CMOS design
- TQFP 64pin
- Pin compatible with THC63LVD104A
- Fail-safe for Open CLK Input

Block Diagram



Pin Out



Pin Description

Pin Name	Pin No.	I/O Type	Description
RA+, RA-	50, 49	LVDS IN	LVDS Data In.
RB+, RB-	52, 51	LVDS IN	
RC+, RC-	55, 54	LVDS IN	
RD+, RD-	60, 59	LVDS IN	
RE+,RE-	62, 61	LVDS IN	
RCLK+, RCLK-	57, 56	LVDS IN	LVDS Clock In.
RA6 ~ RA0	40,41,42,43,45,46,47	OUT	CMOS/TTL Data Outputs.
RB6 ~ RB0	32,33,34,35,36,38,39	OUT	
RC6 ~ RC0	22,24,25,26,27,28,29	OUT	
RD6 ~ RD0	14,15,17,18,19,20,21	OUT	
RE6 ~ RE0	6,7,8,10,11,12,13	OUT	
PD	3	IN	Power down and Output Control.(Table1) H: Normal operation L: Power down
OE	4	IN	Output Enable. See Table1. H:Output enable. L:Output disable
DK	2	IN (3-Level)	Output Clock Delay Timing Select.(Fig5) t_{RCP}=Output Clock Cycle L: Offset 0[nsec] M: Offset $-3\frac{t_{RCP}}{14}$ (typ) [nsec] H: Offset $+3\frac{t_{RCP}}{14}$ (typ)[nsec]
R/F	5	IN	Output Clock Triggering Edge Select.(Fig5) H: Rising Edge L: Falling Edge
VCC	9,23,37,48	Power	Power Supply Pins for TTL outputs and digital circuitry.
CLKOUT	31	OUT	Clock out.
GND	1,16,30,44	Ground	Ground Pins for TTL outputs and digital circuitry.
LVCC	53	Power	Power Supply Pin for LVDS inputs.
LGND	58	Ground	Ground Pin for LVDS inputs.
PVCC	64	Power	Power Supply Pin for PLL circuitry.
PGND	63	Ground	Ground Pin for PLL circuitry.

Pin Description (Continued)

Table 1. Output Control

PD	OE	Data Outputs (Rxn)	CLKOUT
L	L	Hi-Z	Hi-Z
L	H	All Low	Fixed Low
H	L	Hi-Z	Hi-Z
H	H	Data Out	CLK Out

** Rxn x = A,B,C,D,E n = 0,1,2,3,4,5,6

Absolute Maximum Ratings

Supply Voltage (V_{CC})	-0.3V ~ +3.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
Output Current	-30mA ~ 30mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +150°C
Resistance to soldering heat	+260°C /10sec
Maximum Power Dissipation @+25°C	1.4W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
All Supply Voltage	2.3	2.5	2.7	V
Operating Ambient Temperature	0		70	°C
Differential CLKIN Frequency	8		112	MHz
Differential CLKIN High Time(t_{RCIH}) (Fig1)	$2\frac{t_{RCIP}}{7}$		$5\frac{t_{RCIP}}{7}$	nsec
Differential CLKIN Low Time(t_{RCIL}) (Fig1)	$2\frac{t_{RCIP}}{7}$		$5\frac{t_{RCIP}}{7}$	nsec

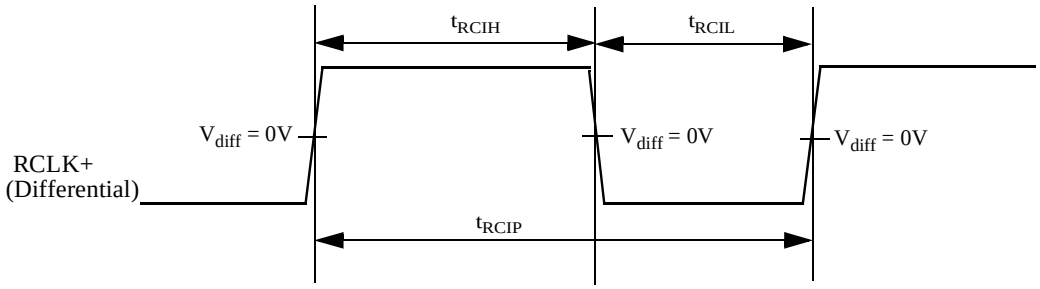


Fig1. Differential CLKIN

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC}=VCC=PVCC=LVCC

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	PD, OE,R/F Pin	1.7		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.7	V
V_{IH3}	High Level Input Voltage	3-Level Inputs(DK Pin)	2.1		V_{CC}	V
V_{IM3}	Middle Level Input Voltage		1.05	1.25	1.45	V
V_{IL3}	Low Level Input Voltage		GND		0.4	V
V_{OH}	High Level Output Voltage	I_{OH}= -2mA	2.1			V
V_{OL}	Low Level Output Voltage	I_{OL}= 2mA			0.4	V
I_{IL}	Input Leakage Current	PD, OE,R/F Pin $0V \le V_{IN} \le V_{CC}$			±10	uA
I_{IL3}	3-Level Input Leakage Current	3-Level Inputs(DK Pin) $0V \le V_{IN} \le V_{CC}$			±10	uA

LVDS Receiver DC Specifications

V_{CC}=VCC=PVCC=LVCC

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{IC}= 1.2V			100	mV
V_{TL}	Differential Input Low Threshold	V_{IC}= 1.2V	-100			mV
I_{ILD}	Differential Input Leakage Current	V_{IN}= 2.4V / 0V			±200	uA

Supply Current

V_{CC}=VCC=PVCC=LVCC

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{RCCW}	Receiver Supply Current Checker Pattern(Worst Case) (Fig 2)	f_{CLKOUT}=65MHz	CL=8pF			125	mA
		f_{CLKOUT}=85MHz				152	mA
		f_{CLKOUT}=112MHz				184	mA
I_{RCCS}	Receiver Power Down Supply Current	PD = L, Ta=RT				10	uA

Electrical Characteristics (Continued)

Checker Pattern

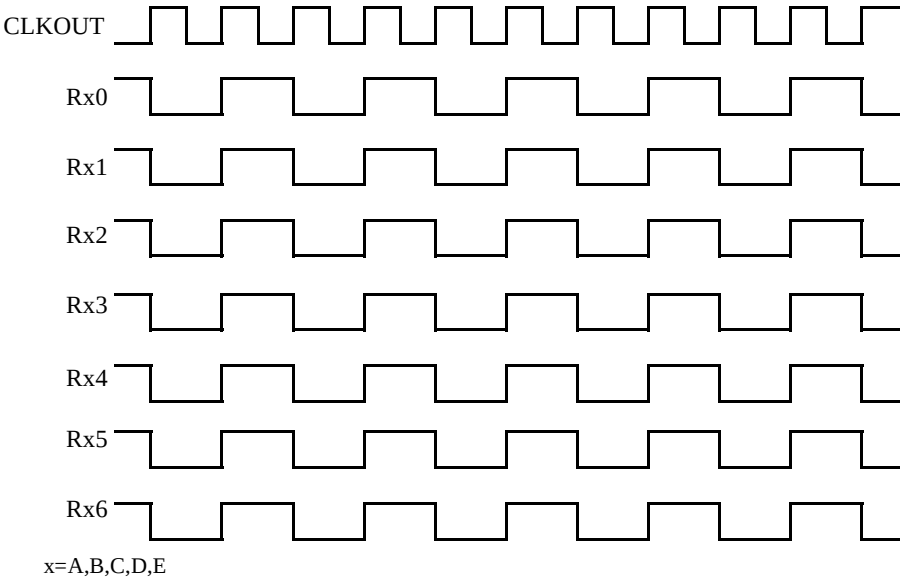


Fig2. Test Pattern

Switching Characteristics

V_{CC}=VCC=PVCC=LVCC

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{RCP}	CLKOUT Period (Fig4)		8.93	T	125.0	ns
t_{RCH}	CLKOUT High Time (Fig4)			$\frac{T}{2}$		ns
t_{RCL}	CLKOUT Low Time (Fig4)			$\frac{T}{2}$		ns
t_{RS}	TTL Data Setup to CLKOUT		$0.50t_{RCP}$-1.5			ns
t_{RH}	TTL Data Hold to CLKOUT		$0.35t_{RCP}$-1.0			ns
t_{TLH}	TTL Low to High Transition Time (Fig 3)			1.3	3.0	ns
t_{THL}	TTL High to Low Transition Time (Fig 3)			1.3	3.0	ns
t_{SK}	Receiver Skew Margin (Fig6)	t_{RCIP}=85MHz	-400	0	400	ps
		t_{RCIP}=112MHz	-350	0	350	ps
t_{RIP1}	Input Data Position0 (Fig6)		$-t_{SK}$	0	$+t_{SK}$	ns
t_{RIP0}	Input Data Position1 (Fig6)		$\frac{t_{RCIP}}{7} - t_{SK}$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP6}	Input Data Position2 (Fig6)		$2\frac{t_{RCIP}}{7} - t_{SK}$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP5}	Input Data Position3 (Fig6)		$3\frac{t_{RCIP}}{7} - t_{SK}$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP4}	Input Data Position4 (Fig6)		$4\frac{t_{RCIP}}{7} - t_{SK}$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP3}	Input Data Position5 (Fig6)		$5\frac{t_{RCIP}}{7} - t_{SK}$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP2}	Input Data Position6 (Fig6)		$6\frac{t_{RCIP}}{7} - t_{SK}$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RPLL}	Phase Lock Loop Set (Fig7)				10.0	ms
t_{RCD}	RCLK +/- to CLK OUT Delay (Fig8)	t_{RCIP}=75MHz	45.5		48.5	ns
t_{RCIP}	CLKIN Period (Fig6)		8.93		125.0	ns

AC Timing Diagrams

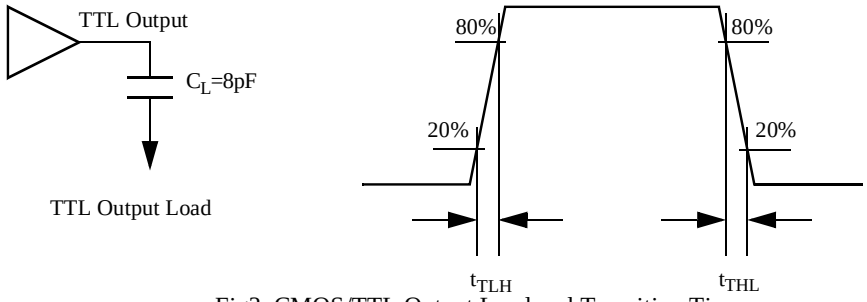


Fig3. CMOS/TTL Output Load and Transition Time

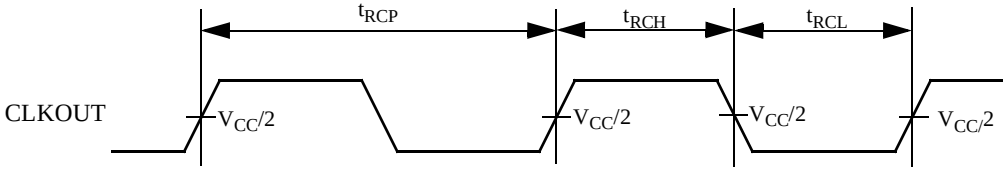


Fig4. CLKOUT Period and High/Low Time

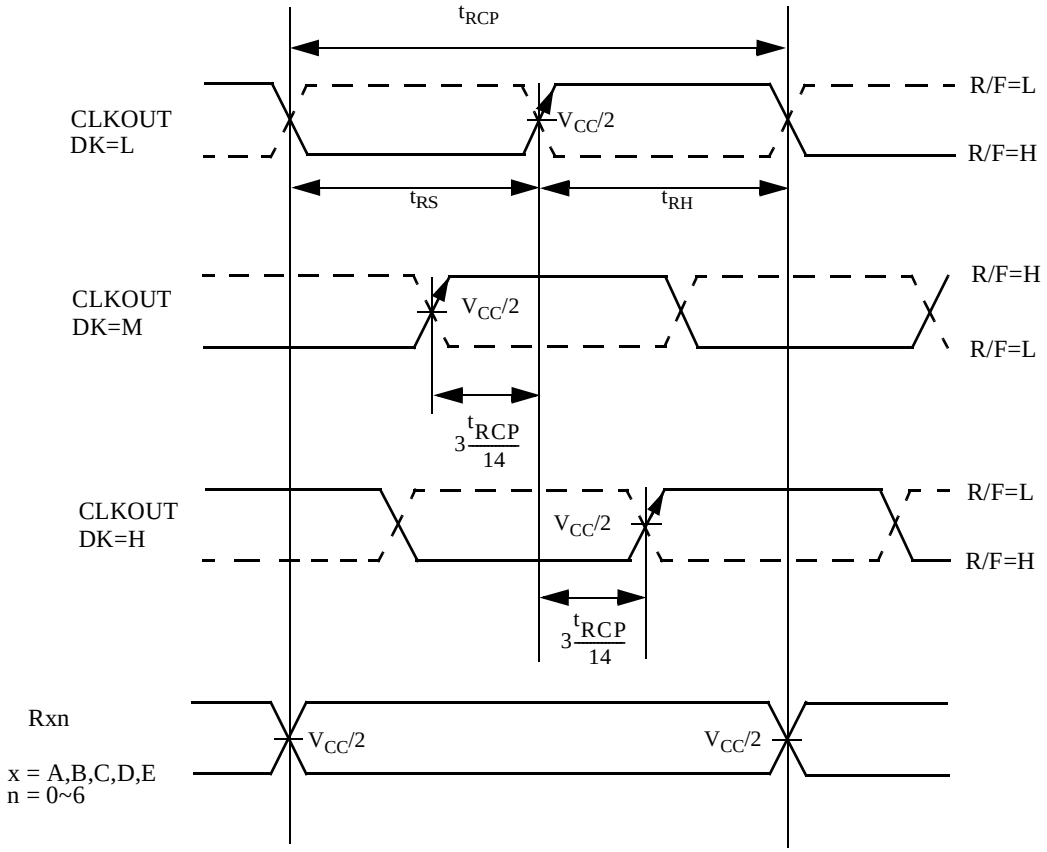


Fig5. CLKOUT Position and Setup/Hold Timing

AC Timing Diagrams (Continued)

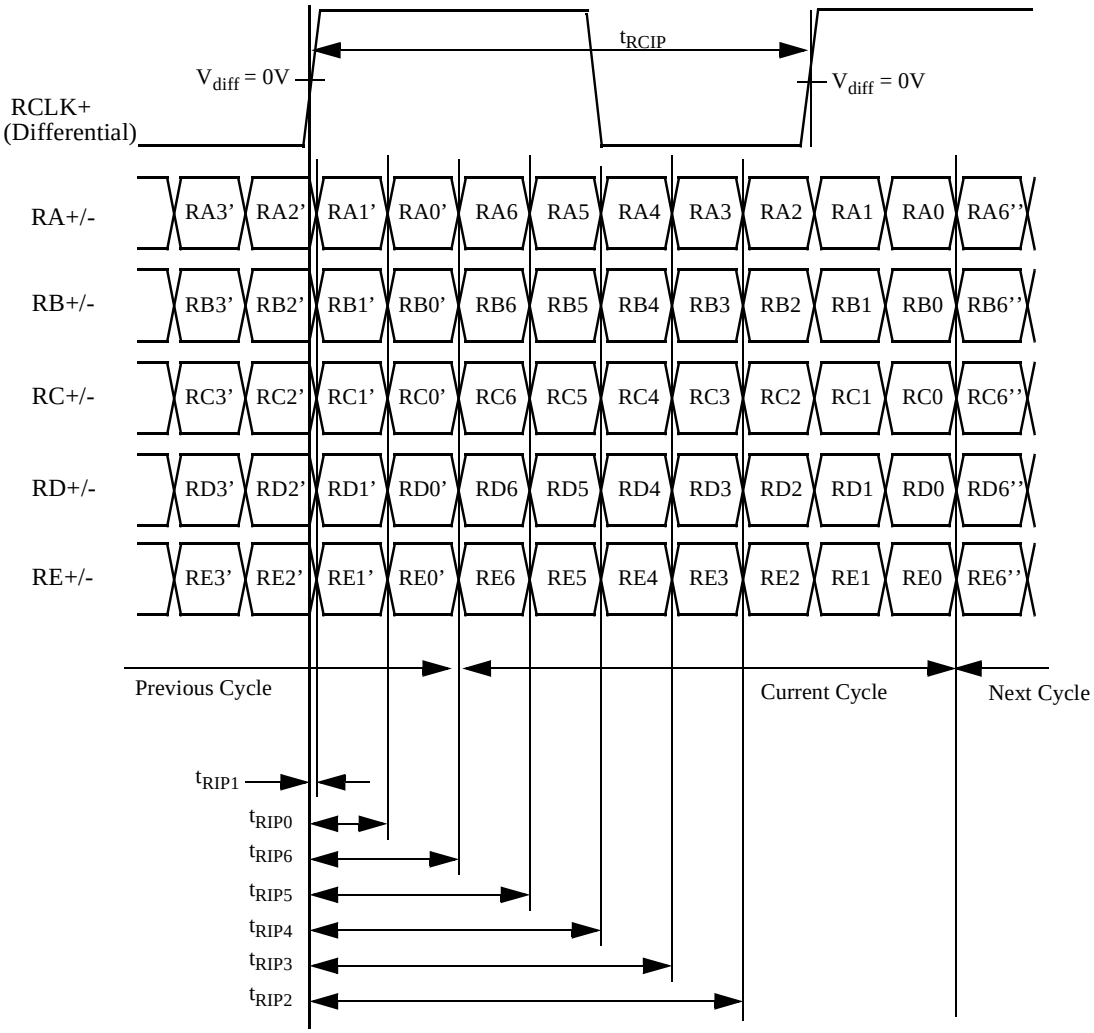


Fig6. LVDS Input Data Position

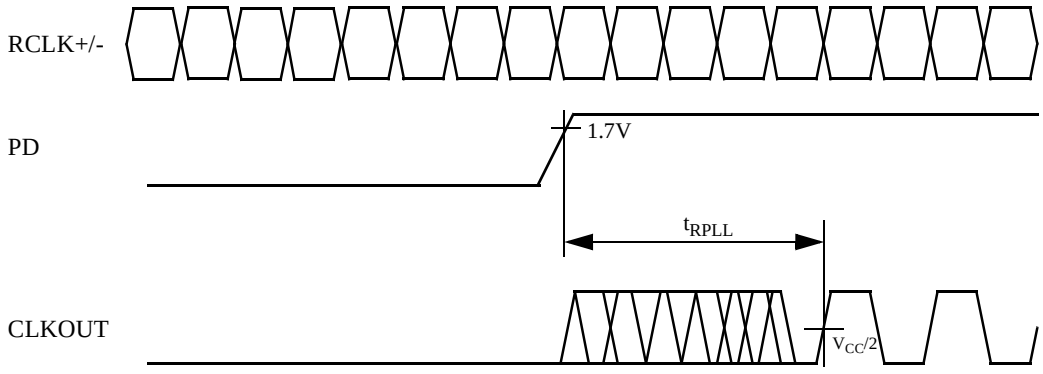
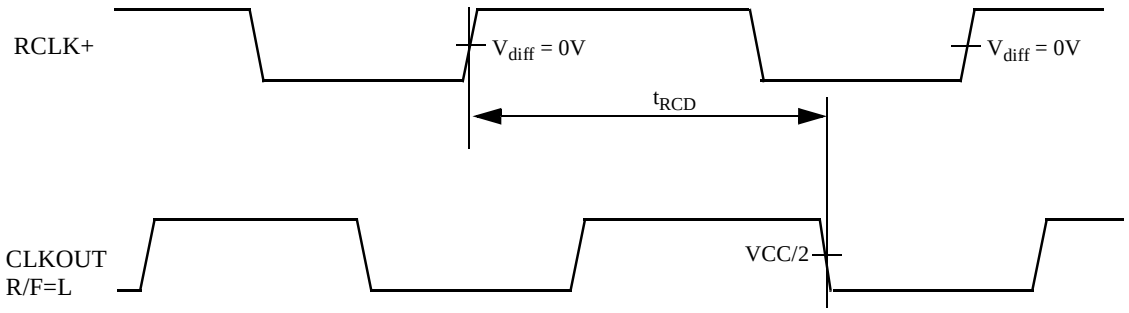


Fig7. PLL Lock Loop Set Time

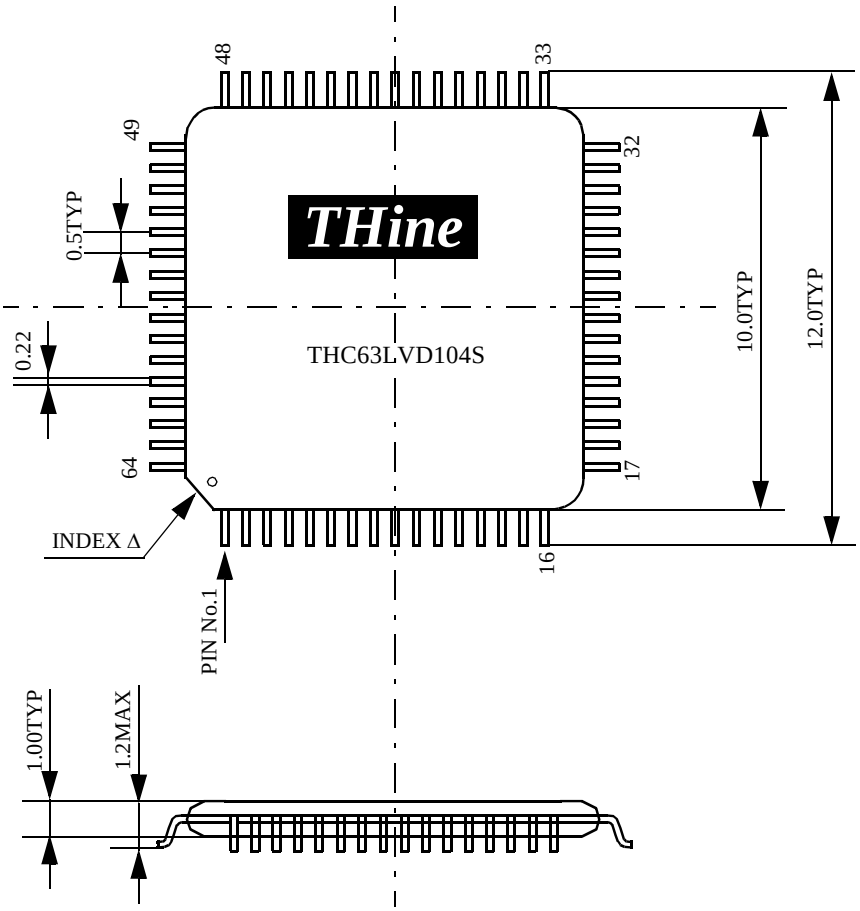
AC Timing Diagrams (Continued)



Note:
1) Vdiff = (RCLK+) - (RCLK-)

Fig8. RCLK +/- to CLK OUT Delay

Package



UNITS: mm

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