Si8220/21

0.5 and 2.5 Amp ISOdrivers with Opto Input (2.5, 3.75, and 5.0 kV_{RMS})

Features

- Functional upgrade for HCPL-0302, HCPL-3120, TLP350, and similar opto-drivers
- 50 ns propagation delay (independent of input drive current)
- 14x tighter part-to-part matching versus opto-drivers
- 2.5, 3.75, and 5.0 kV_{RMS} isolation
- Transient Immunity
  - 30 kV/µs
- Under-voltage lockout protection with hysteresis
- Resistant to temperature and aging effects
- Gate driver supply voltage: 6.5 V to 24 V
- Operating temperature range: –40 to +125 °C
- Cost-effective
- Narrow body SOIC-8 and Wide body SOIC-16 packages
- RoHS Compliant

Applications

- IGBT/ MOSFET gate drives
- Industrial control systems
- Switch mode power supplies
- UPS systems
- Motor control drives
- Inverters

Safety Regulatory Approvals

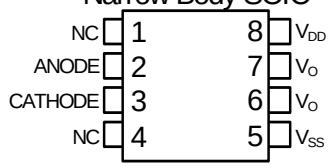
- UL 1577 recognized
  - Up to 5000 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950, 61010, 60601 approved
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)

Description

The Si8220/21 is a high-performance, functional upgrade for opto-coupled drivers, such as the HCPL-3120 and the HPCL-0302 providing 2.5 A of peak output current. It utilizes Silicon Laboratories' proprietary silicon isolation technology, which provides a choice of 2.5, 3.75, or 5.0 kV_{RMS} withstand voltages per UL1577. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and superior common-mode rejection compared to opto-isolated drivers. While the input circuit mimics the characteristics of an LED, less drive current is required, resulting in increased efficiency. Propagation delay time is independent of input drive current, resulting in consistently short propagation time, tighter unit-to-unit variation, and greater input circuit design flexibility.

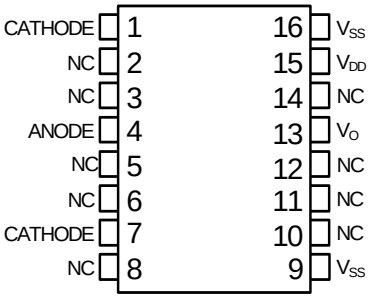
Pin Assignments:
See page 19

Narrow Body SOIC



Top View

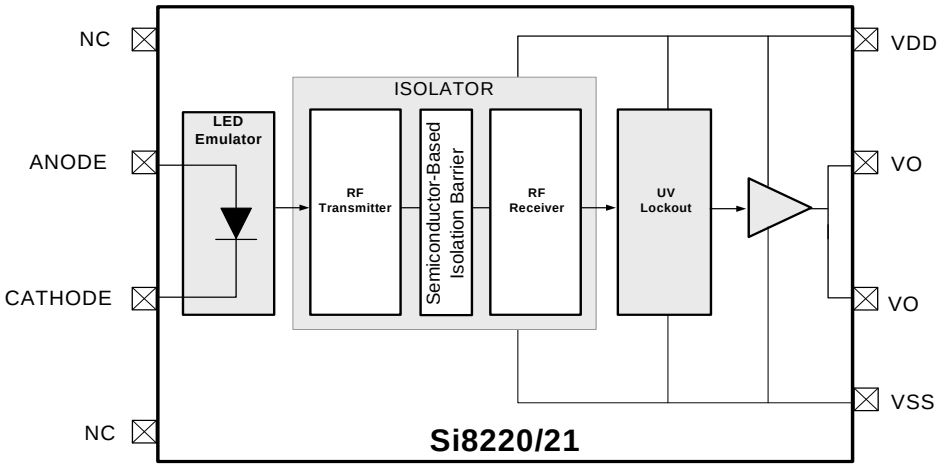
Wide Body SOIC



Top View

Patent pending

Functional Block Diagram



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Section **Page**

1. Electrical Specifications

Table 1. Electrical Characteristics [1]

V_{DD} = 12 V or 15 V, V_{SS} = GND, T_A = –40 to +125 °C; typical specs at 25 °C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DC Specifications						
Power supply voltage	V_{DD}	(V_{DD} – V_{SS})	6.5	—	24	V
Input current (ON)	$I_{F(ON)}$		5.0	—	20	mA
Input current rising edge hysteresis	I_{HYS}		—	1.0	—	mA
Input voltage (OFF)	$V_{F(OFF)}$	Measured at ANODE with respect to CATHODE.	–0.6	—	1.6	V
Input forward voltage	V_F	Measured at ANODE with respect to CATHODE. I_F = 5 mA.	1.7	—	2.5	V
Output resistance high (source)	R_{OH}	0.5 A devices	—	15	—	Ω
		2.5 A devices	—	2.7	—	
Output resistance low (sink)	R_{OL}	0.5 A devices	—	5.0	—	
		2.5 A devices	—	1.0	—	
Output high current (source)	I_{OH}	(0.5 A), I_F = 0 (see Figure 2)	—	0.3	—	A
		(2.5 A), I_F = 0 (see Figure 2)	—	1.5	—	
Output low current (sink)	I_{OL}	(0.5 A), I_F = 10 mA, (see Figure 1)	—	0.5	—	A
		(2.5 A), I_F = 10 mA, (see Figure 1)	—	2.5	—	
High-level output voltage	V_{OH}	(0.5 A), I_{OUT} = –50 mA	—	V_{DD}–0.5	—	V
		(2.5 A), I_{OUT} = –50 mA		V_{DD}–0.1		
Low-level output voltage	V_{OL}	(0.5 A), I_{OUT} = 50 mA	—	200	—	mV
		(2.5 A), I_{OUT} = 50 mA		50		
High level supply current		Output open I_F = 10 mA	—	1.2	—	mA
Low level supply current		Output open V_F = –0.6 to +1.6 V	—	1.4	—	mA
Input reverse voltage	BV_R	I_R = 10 mA. Measured at ANODE with respect to CATHODE.	0.5	—	—	V
Input capacitance	C_{IN}		—	5	—	pF

Notes:
1. VDD = 12 V for 5, 8, and 10 V UVLO devices; VDD = 15 V for 12.5 V UVLO devices.
2. See "9.Ordering Guide" on page 21 for more information.

Table 1. Electrical Characteristics (Continued)[1]

V_{DD} = 12 V or 15 V, V_{SS} = GND, T_A = –40 to +125 °C; typical specs at 25 °C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VDD Undervoltage Threshold[2]	VDD_{UV+}	V_{DD} rising				
5 V threshold		See Figure 8 on page 13.	5.20	5.80	6.30	V
8 V threshold		See Figure 9 on page 13.	7.50	8.60	9.40	V
10 V threshold		See Figure 10 on page 13.	9.60	11.1	12.2	V
12.5 V threshold		See Figure 11 on page 13.	12.4	13.8	14.8	
VDD Undervoltage Threshold[2]	VDD_{UV-}	V_{DD} falling				
5 V threshold		See Figure 8 on page 13.	4.90	5.52	6.0	V
8 V threshold		See Figure 9 on page 13.	7.20	8.10	8.70	V
10 V threshold		See Figure 10 on page 13.	9.40	10.1	10.9	V
12.5 V threshold		See Figure 11 on page 13.	11.6	12.8	13.8	
VDD Lockout hysteresis	VDD_{HYS}	UVLO voltage = 5 V	—	280	—	mV
VDD Lockout hysteresis	VDD_{HYS}	UVLO voltage = 8 V	—	600	—	mV
VDD Lockout hysteresis	VDD_{HYS}	UVLO voltage = 10 V or 12.5 V	—	1000	—	mV
AC Specifications						
Propagation delay time to high output level	t_{PLH}	C_L = 200 pF	—	—	50	ns
Propagation delay time to low output level	t_{PHL}	C_L = 200 pF	—	—	30	ns
UVLO turn-off delay	$t_{UVLO\ OFF}$		—	—	50	ns
Output rise and fall time	t_R, t_F	(0.5 A), C_L = 200 pF	—	—	30	ns
		(2.5 A), C_L = 200 pF	—	—	20	
Device start-up time	t_{START}	Time from V_{DD} = V_{DD_UV+} to V_O	—	—	40	µs
Common Mode Transient Immunity	CMTI	Input ON or OFF	30	50	—	kV/µs

Notes:

1. VDD = 12 V for 5, 8, and 10 V UVLO devices; VDD = 15 V for 12.5 V UVLO devices.
2. See "9.Ordering Guide" on page 21 for more information.

2. Test Circuits

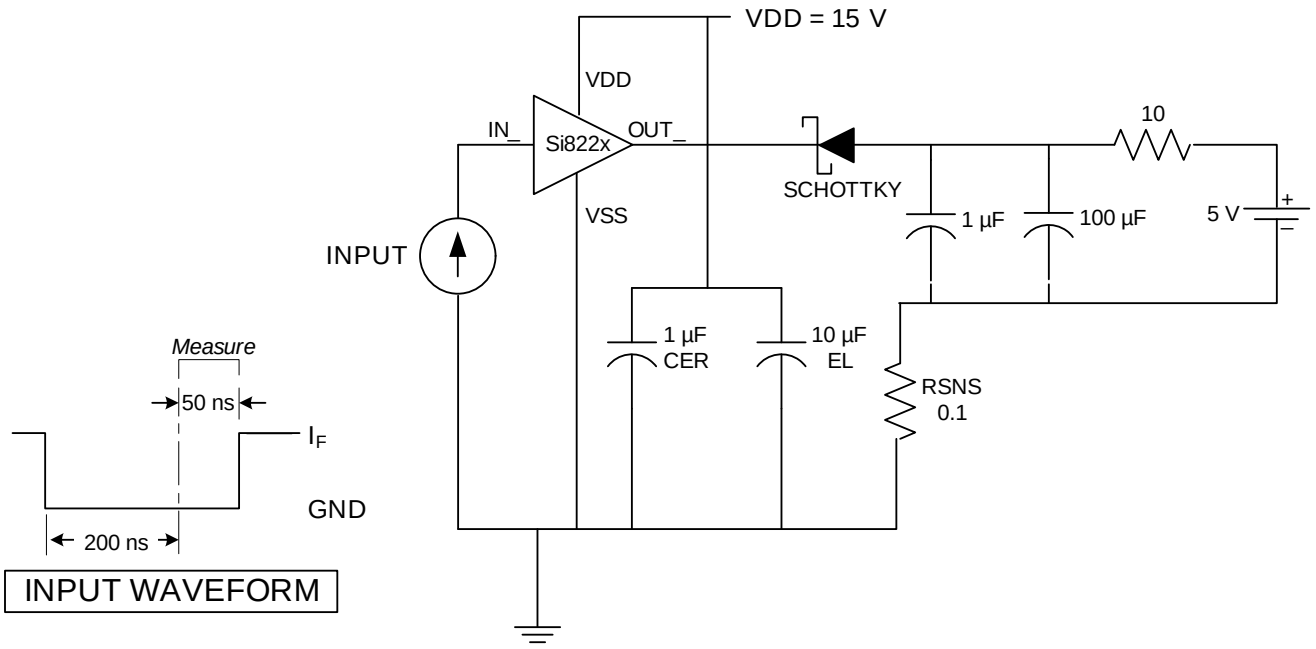


Figure 1. IOL Sink Current Test Circuit

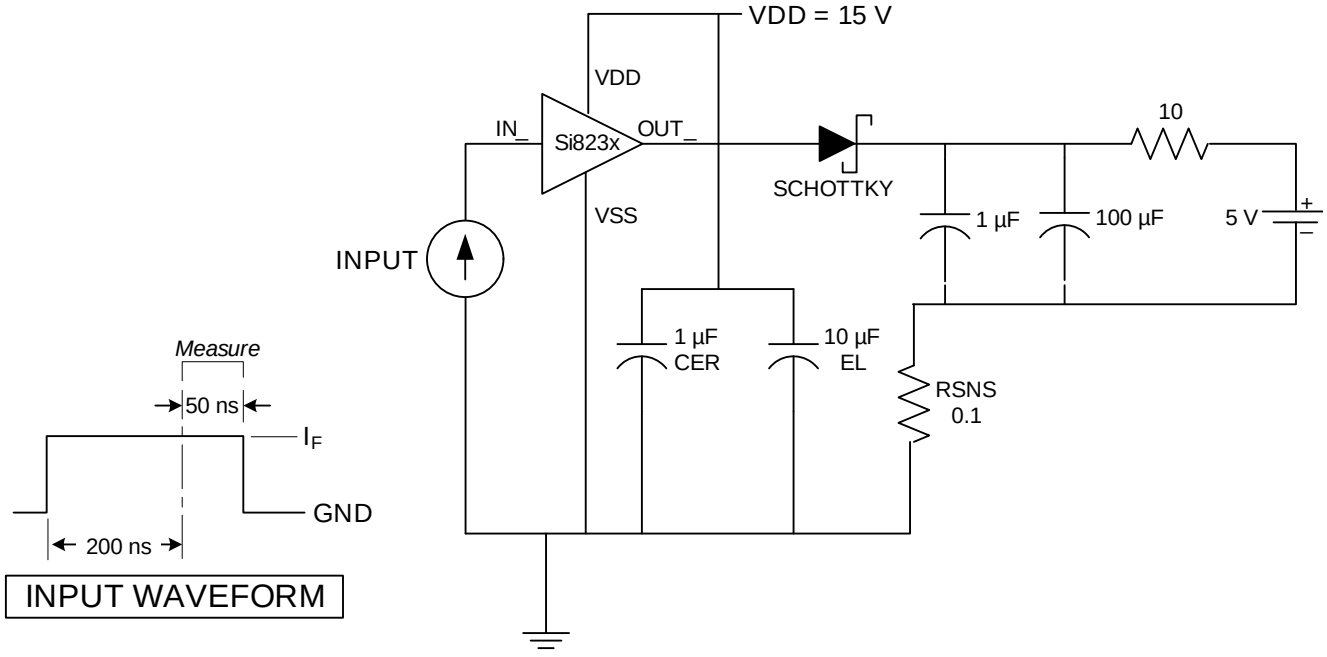


Figure 2. IOH Source Current Test Circuit

3. Regulatory Information

Table 2. Regulatory Information*

CSA
The Si82xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
VDE
The Si82xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
UL
The Si82xx is certified under UL1577 component recognition program. For more details, see File E257455.
***Note:** Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec. For more information, see "9.Ordering Guide" on page 21.

Table 3. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB SOIC-16	NB SOIC-8	
Nominal Air Gap (Clearance)[1]	L(IO1)		8.0 min	4.9 min	mm
Nominal External Tracking (Creepage)[1]	L(IO2)		8.0 min	4.01 min	mm
Minimum Internal Gap (Internal Clearance)			0.014	0.014	mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN IEC 60112/VDE 0303 Part 1	>175	>175	V
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	1.0	pF
Input Capacitance[3]	C_I		4.0	4.0	pF

Notes:

1. The values in this table correspond to the nominal creepage and clearance values as detailed in "12.Package Outline: 16-Pin Wide Body SOIC" on page 25, "10.Package Outline: 8-Pin Narrow Body SOIC" on page 23. VDE certifies the clearance and creepage limits as 8.5 mm minimum for the WB SOIC-16 package and 4.7 mm minimum for the NB SOIC-8 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-8 and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si82xx is converted into a 2-terminal device. Pins 1–8 (1–4, NB SOIC-8) are shorted together to form the first terminal and pins 9–16 (5–8, NB SOIC-8) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 4. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Conditions	Specification	
		NB SOIC8	WB SOIC 16
Basic isolation group	Material Group	IIIa	IIIa
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III	I-IV
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II	I-III
	Rated Mains Voltages ≤ 600 V_{RMS}	I-II	I-III

Table 5. IEC 60747-5-2 Insulation Characteristics for Si82xxxC*

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-16	NB SOIC-8	
Maximum Working Insulation Voltage	V_{IORM}		891	560	V peak
Input to Output Test Voltage	V_{PR}	Method a After Environmental Tests Subgroup 1 (V_{IORM} x 1.6 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	1590	896	V peak
		Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1375	1050	
		After Input and/or Safety Test Subgroup 2/3 (V_{IORM} x 1.2 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	1018	672	
Highest Allowable Overvoltage (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}		6000	4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		>10^9	>10^9	Ω

***Note:** This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si82xx provides a climate classification of 40/125/21.

Table 6. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Min	Typ	Max		Unit
					WB SOIC-16	NB SOIC-8	
Case Temperature	T_S		—	—	150	150	°C
Safety input, output, or supply current	I_S	θ_{JA} = 140 °C/W (NB SOIC-8), 100 °C (WB SOIC-16), V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	—	—	50	40	mA
Device Power Dissipation[2]	P_D		—	—	1.2	1.2	W

Notes:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 4.
2. The Si822x is tested with V_O = 24 V, T_J = 150 ºC, C_L = 200 pF, input a 2 MHz 50% duty cycle square wave.

Table 7. Thermal Characteristics

Parameter	Symbol	Min	Typ		Max	Unit
			WB SOIC-16	NB SOIC-8		
IC Junction-to-Air Thermal Resistance	θ_{JA}	—	100	140	—	ºC/W

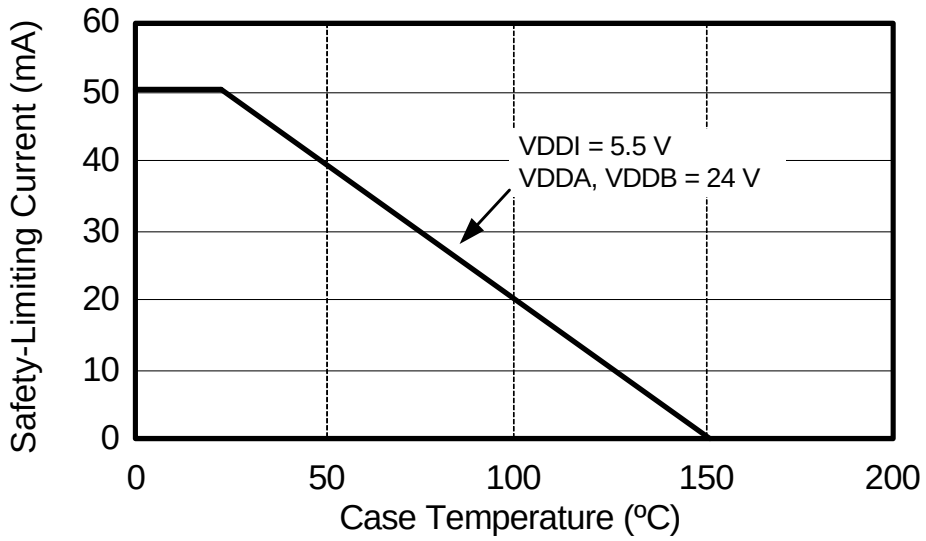


Figure 3. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

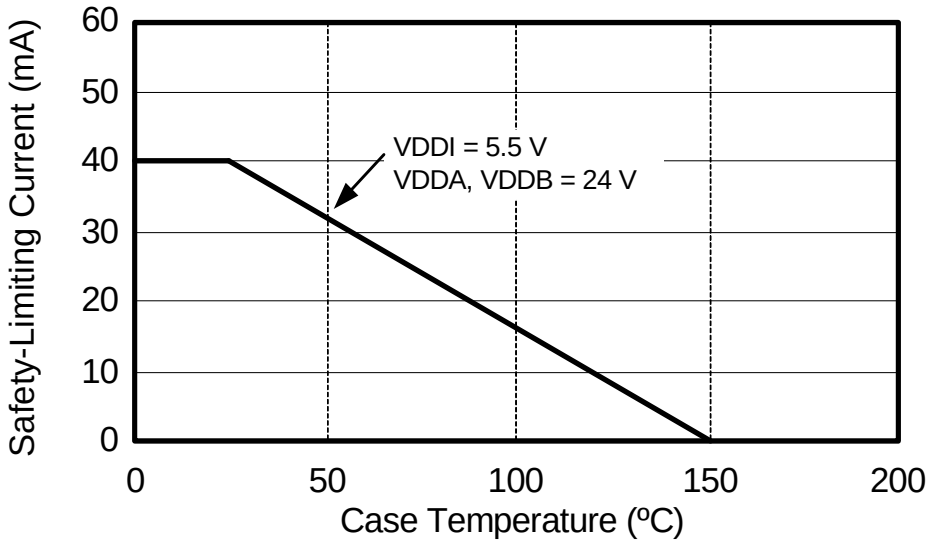


Figure 4. (NB SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

Table 8. Absolute Maximum Ratings[1]

Parameter	Conditions	Min	Typ	Max	Units
Storage temperature[2]	T_{STG}	–65	—	+150	°C
Operating temperature		–40	—	+125	°C
Output supply voltage	V_{DD}	–0.6	—	30	V
Output voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output current drive	I_O	—	—	10	mA
Input current	$IF_{(AVG)}$	–100	—	30	V
Lead solder temperature (10 s)		—	—	260	°C
Maximum Isolation Voltage (1 s) NB SOIC-8		—	—	4250	V_{RMS}
Maximum Isolation Voltage (1 s) WB SOIC-16		—	—	6500	V_{RMS}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.

4. Application Information

4.1. Theory of Operation

The Si8220/21 is a functional upgrade for popular opto-isolated drivers, such as the Avago HPCL-3120, HPCL-0302, Toshiba TLP350, and others. The operation of an Si8220/21 channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for the Si8220/21 is shown in Figure 5.

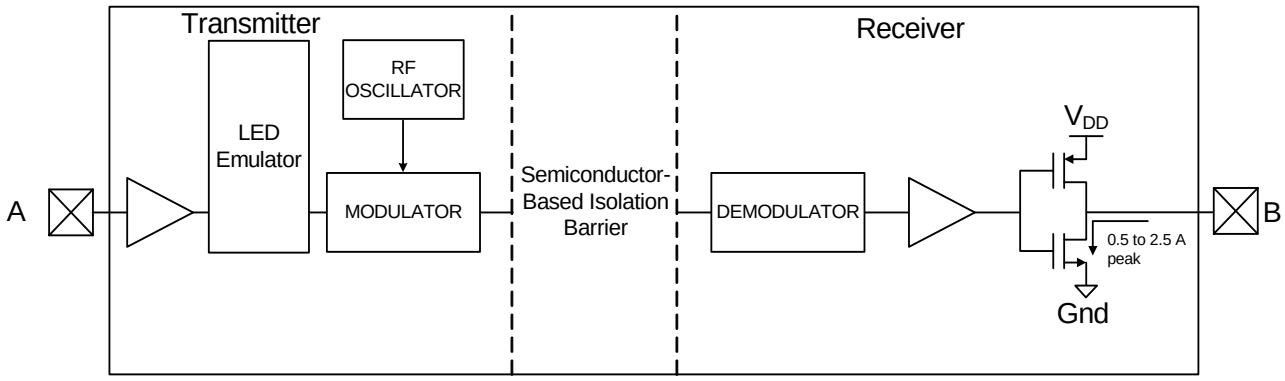


Figure 5. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 6 for more details.

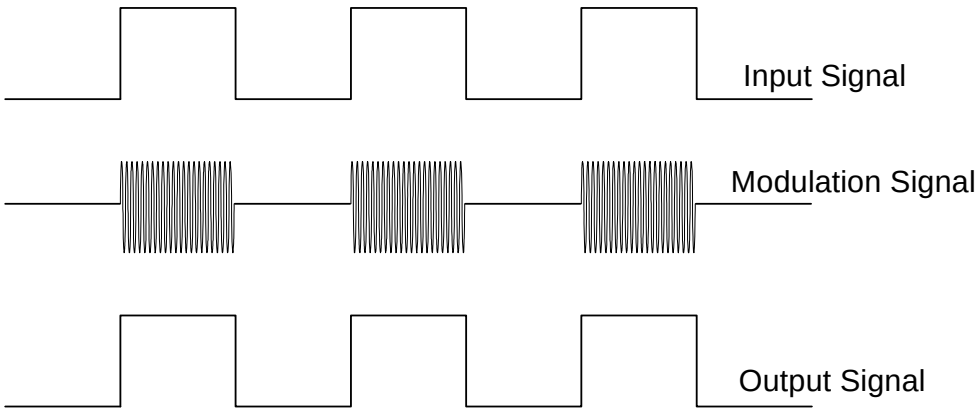


Figure 6. Modulation Scheme

5. Technical Description

5.1. Device Behavior

Truth tables for the Si8220/21 are summarized in Table 9.

Table 9. Si8220/21 Truth Table Summary

Cathode	Anode	Diode Current (I_F)	V_{DD}	VO	Comments
X	X	X	< UVLO	L	Device turned off
Hi-Z	X	0	> UVLO	L	Logic low state
X	Hi-Z	0	> UVLO	L	Logic low state
GND	GND	0	> UVLO	L	Logic low state
VF	VF	0	> UVLO	L	Logic low state
GND1	VF	< $I_{F(OFF}$	> UVLO	L	Logic low state
GND1	VF	≥ $I_{F(OFF)}$	> UVLO	H	Logic high state
Note: "X" = don't care.					

5.2. Device Startup

Output V_O is held low during power-up until V_{DD} rises above the UVLO+ threshold for a minimum time period of t_{START}. Following this, the output is high when the current flowing from anode to cathode is > $I_{F(ON)}$. Device startup, normal operation, and shutdown behavior is shown in Figure 7.

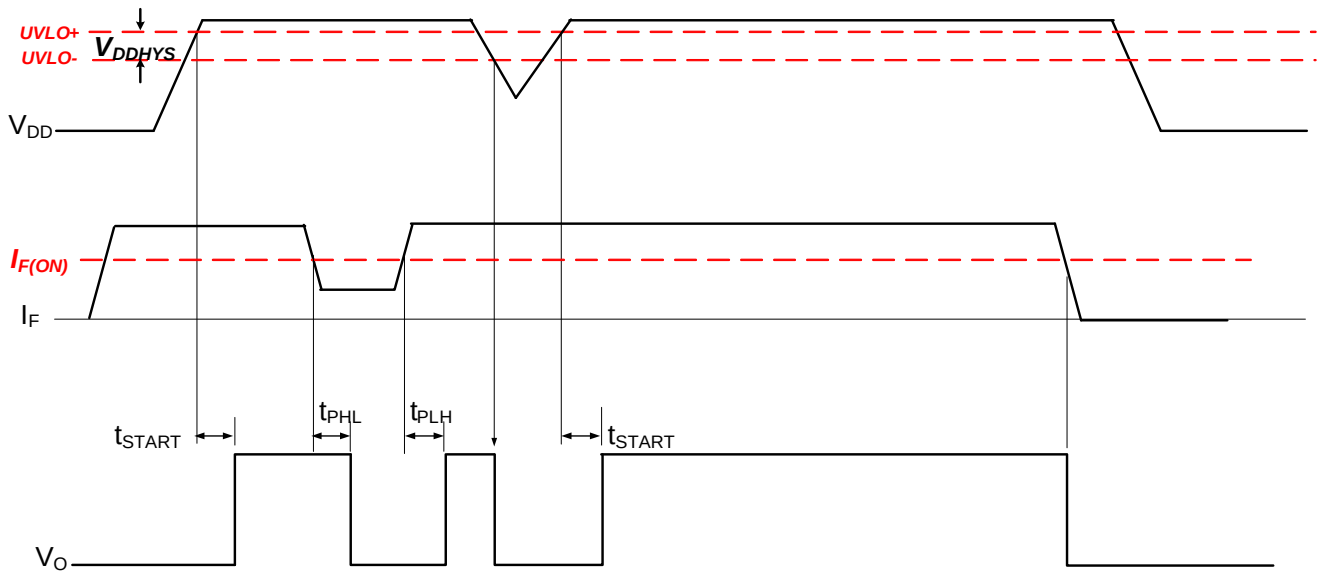


Figure 7. Si8220/21 Operating Behavior ($I_F \geq I_{F(MIN)}$ when $V_F \geq V_{F(MIN)}$)

5.3. Under Voltage Lockout (UVLO)

The UVLO circuit unconditionally drives V_O low when V_{DD} is below the lockout threshold. Referring to Figures 8 through 11, upon power up, the Si8220/21 is maintained in UVLO until VDD rises above VDD_{UV+}. During power down, the Si8220/21 enters UVLO when VDD falls below the UVLO threshold plus hysteresis (i.e., VDD $\leq$ VDD_{UV+} – VDD_{HYS}).

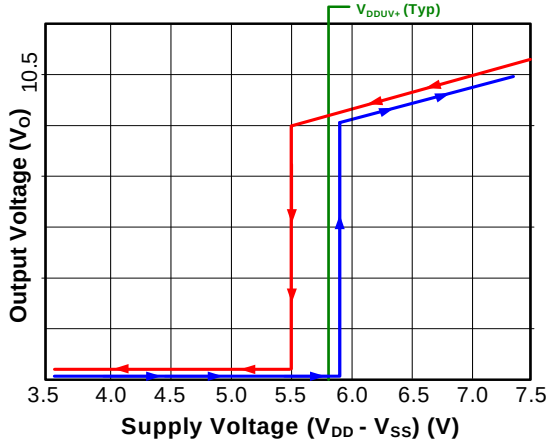


Figure 8. Si8220/21 UVLO Response (5 V)

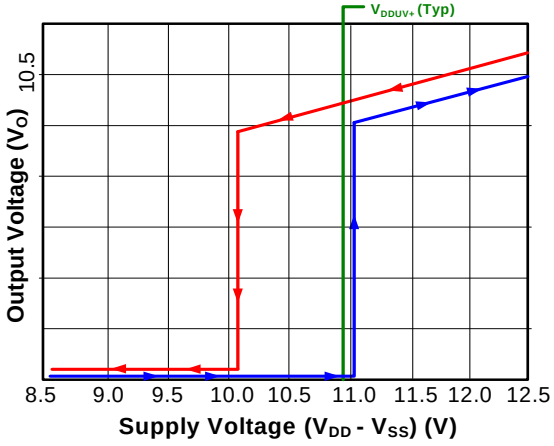


Figure 10. Si8220/21 UVLO Response (10 V)

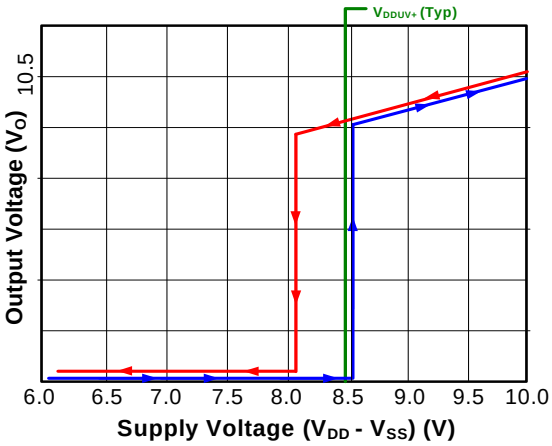


Figure 9. Si8220/21 UVLO Response (8 V)

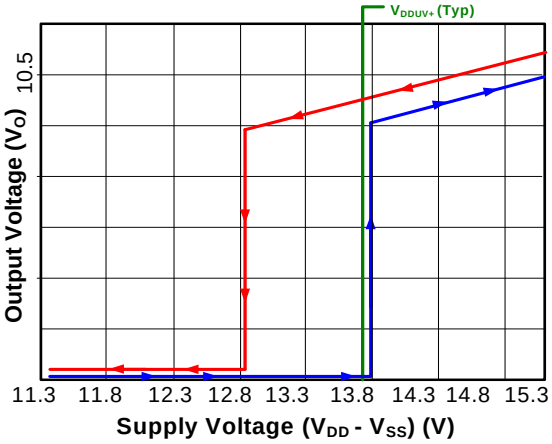


Figure 11. Si8220/21 UVLO Response (12.5 V)

6. Applications

6.1. Power Supply Connections

V_{SS} can be biased at, above, or below ground as long as the voltage on V_{DD} with respect to V_{SS} is a maximum of 24 V. V_{DD} decoupling capacitors should be placed as close to the package pins as possible. The optimum values for these capacitors depend on load current and the distance between the chip and its power source. It is recommended that 0.1 and 10 µF bypass capacitors be used to reduce high-frequency noise and maximize performance.

6.2. Layout Considerations

It is most important to minimize ringing in the drive path and noise on the V_{DD} lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si8220/21 as close to the device it is driving as possible. In addition, the V_{DD} supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and V_{DD} planes for power devices and small signal components provides the best overall noise performance.

6.3. Power Dissipation Considerations

Proper system design must assure that the Si8220/21 operates within safe thermal limits across the entire load range. The Si8220/21 total power dissipation is the sum of the power dissipated by bias supply current, internal switching losses, and power delivered to the load, as shown in Equation 1.

$$P_D = (V_F)(I_F) + (V_{DD})(I_{QOUT}) + (C_{int})(V_{DD}^2)(F) + 2(C_L)(V_{DD}^2)(F)$$

where:

P_D is the total Si8220 device power dissipation (W)

I_F is the diode current (10 mA max)

V_F is the diode anode voltage (2.8 V max)

I_{QOUT} is the driver maximum bias curent (5 mA)

C_{int} is the internal parasitic capacitance (370 pF)

V_{DD} is the driver-side supply voltage (24 V max)

F is the switching frequency (Hz)

Equation 1.

The maximum allowable power dissipation for the Si8220/21 is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2.

$$P_{D(MAX)} \leq \frac{T_{jmax} - T_A}{\theta_{ja}}$$

where:

$P_{D(MAX)}$ is the maximum allowable Si8220/21 power dissipation (W)

T_{jmax} is the Si8220/21 maximum junction temperature (145 °C)

T_A is the ambient temperature (°C)

θ_{ja} is the Si8220/21 package junction-to-air thermal resistance (125 °C/W)

Equation 2.

Substituting values for $P_{D(MAX)}$, T_{jmax}, T_A, and θ_{ja} into Equation 2 results in a maximum allowable total power dissipation of 0.95 W. The maximum allowable load is found by substituting this limit and the appropriate datasheet values from Table 1 on page 4 into Equation 1 and simplifying. The result is Equation 3, where V_F = 2.8 V, I_F = 10 mA, and V_{DD} = 18 V.

$$C_{L(max)} = \frac{1.35 \times 10^{-3}}{F} - 1.85 \times 10^{-10}$$

where:

$C_{L(max)}$ is the maximum load (pF) allowable at switching frequency F

Equation 3.

A graph of Equation 3 is shown in Figure 12. Each point along the load line in this graph represents the package dissipation-limited value of C_L for the corresponding switching frequency.

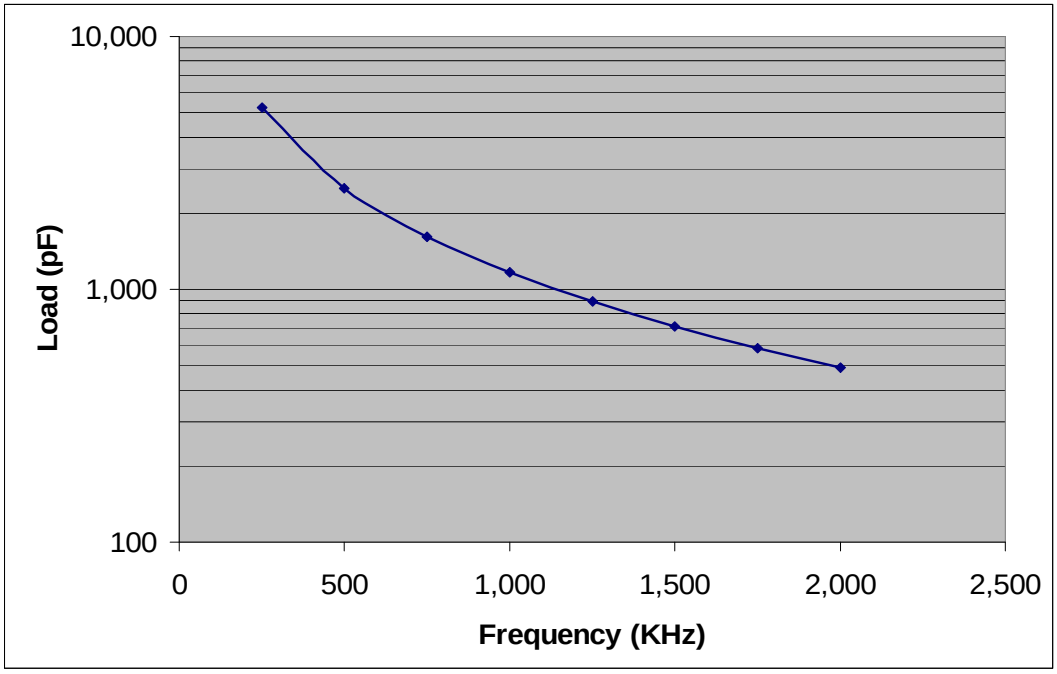


Figure 12. Maximum Load vs. Switching Frequency

6.4. Input Circuit Design

Opto driver manufacturers typically recommend the circuits shown in Figures 13 and 14. These circuits are specifically designed to improve opto-coupler input common-mode rejection and increase noise immunity.

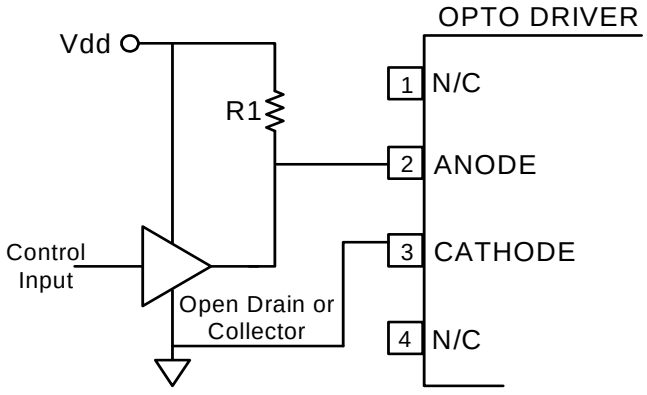


Figure 13. Opto Driver Input Circuit

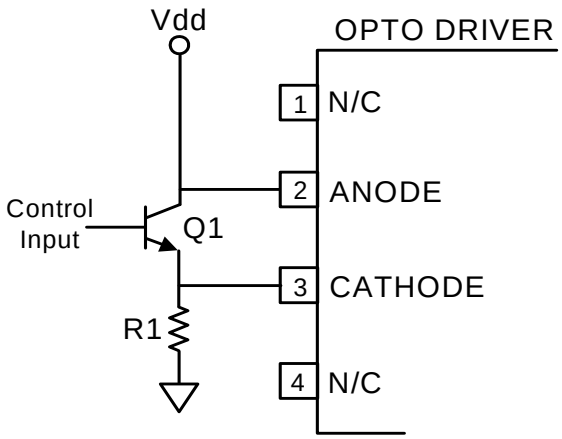


Figure 14. High CMR Opto Driver Input Circuit

The optically-coupled driver circuit of Figure 13 turns the LED on when the control input is high. However, internal capacitive coupling from the LED to the power and ground conductors can momentarily force the LED into its off state when the anode and cathode inputs are subjected to a high common-mode transient. The circuit shown in Figure 14 addresses this issue by using a value of R1 sufficiently low to overdrive the LED, ensuring it remains on during an input common-mode transient. Q1 shorts the LED off in the low output state, again increasing common-mode transient immunity. Some opto driver applications also recommend reverse-biasing the LED when the control input is off to prevent coupled noise from energizing the LED.

The Si8220/21 can be used with the input circuits shown in Figures 13 and 14; however, some applications will require increasing the value of R1 in order to limit I_F to a maximum of 10 mA. The Si8220/21 propagation delay and output drive do not change for values of I_F between $I_{F(MIN)}$ and $I_{F(MAX)}$. New designs should consider the input circuit configurations of Figure 15, which are more efficient than those of Figures 13 and 14. As shown, S1 represents any suitable switch, such as a BJT or MOSFET, analog transmission gate, processor I/O, etc. Also, note that the Si8220/21 input can be driven from the I/O port of any MCU or FPGA capable of sourcing a minimum of 5 mA (see Figure 15C).

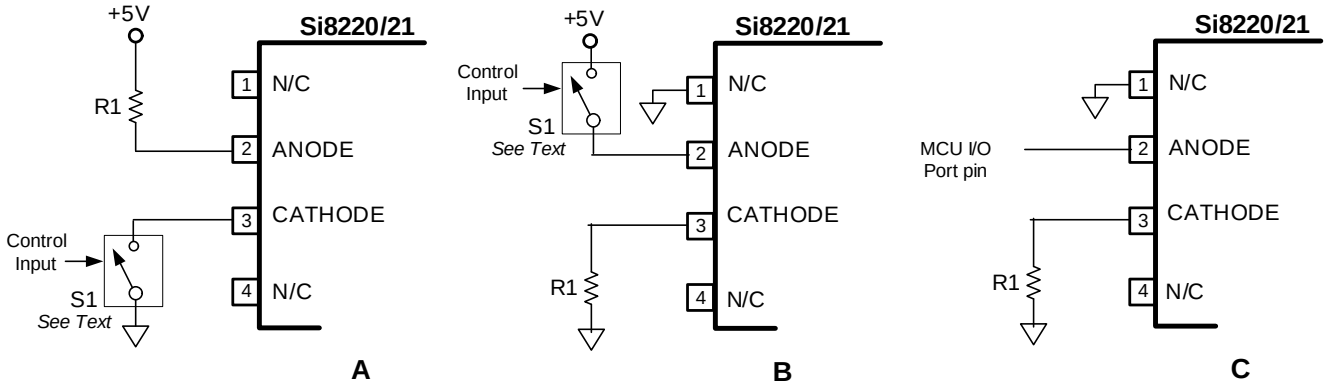


Figure 15. Si8220/21 Other Input Circuit Configurations

6.5. Parametric Differences between Si8220/21 and HCPL-0302 and HCPL-3120 Opto Drivers

The Si8220/21 is designed to directly replace HCPL-3120 and similar opto drivers. Parametric differences are summarized in Table 10 below.

Table 10. Parametric Differences of Si8220 vs. HCPL-3120

Parameter	Si8220	HCPL-3120	Units
Max supply voltage	24	30	V
ON state forward input current	5 to 20	7 to 16	mA
OFF state input voltage	–0.6 to +1.6	–0.3 to +0.8	V
Max reverse input voltage	0.5	–5	V
UVLO threshold (rising)	5.8 to 13.8	11.0 to 13.5	V
UVLO threshold (falling)	5.5 to 12.8	9.7 to 12.0	V
UVLO hysteresis	0.28 to 1	1.6	V
Rise/fall time into 10 Ω in series with 10 nF	20	100	ns

Table 11. Parametric Differences of Si8221 vs. HCPL-0302

Parameter	Si8221	HCPL-0302	Units
Max supply voltage	24	30	V
ON state forward input current	5 to 20	7 to 16	mA
OFF state input voltage	–0.6 to +1.6	–0.3 to +0.8	V
Max reverse input voltage	0.5	–5	V
UVLO threshold (rising)	5.8 to 13.8	11.0 to 13.5	V
UVLO threshold (falling)	5.5 to 12.8	9.7 to 12.0	V
UVLO hysteresis	0.28 to 1	1.6	V
Rise/fall time into 10 Ω in series with 10 nF	20	100	ns

6.5.1. Supply Voltage and UVLO

The supply voltage of the Si8220/21 is limited to 24 V, and the UVLO voltage thresholds are scaled accordingly. This will not be an issue for opto replacement applications operating with supply voltages of 24 V and below.

6.5.2. Input Diode Differences

The Si8220/21 input circuit requires less current and has twice the off-state noise margin compared to opto drivers. However, high CMR opto driver designs that overdrive the LED (see Figure 14) may require increasing the value of R1 to limit input current to 10 mA max. In addition, there is no benefit in driving the Si8220/21 input diode into reverse bias when in the off state. Consequently, opto driver circuits using this technique should either leave the negative bias circuitry unpopulated or modify the circuitry (e.g. add a clamp diode) to ensure that the anode pin of the Si8220/21 is no more than -0.8 V with respect to the cathode when reverse-biased.

6.6. RF Radiated Emissions

The Si822x family uses an RF carrier frequency of approximately 700 MHz. This results in a small amount of radiated emissions at this frequency and its harmonics. The radiation is not from the IC chip but, rather, is due to a small amount of RF energy driving the isolated ground planes, which can act as a dipole antenna.

The unshielded Si822x evaluation board passes FCC Class B (Part 15) requirements. Table 12 shows measured emissions compared to FCC requirements. Note that the data reflects worst-case conditions where all inputs are tied to logic 1 and the RF transmitters are fully active.

Radiated emissions can be reduced if the circuit board is enclosed in a shielded enclosure or if the PCB is a less efficient antenna.

Table 12. Radiated Emissions (Preliminary)

Frequency (MHz)	Measured (dBµV/m)	FCC Spec (dBµV/m)	Compared to Spec (dB)
712	29	37	–8
1424	39	54	–15
2136	42	54	–12
2848	43	54	–11
4272	44	54	–10
4984	44	54	–10
5696	44	54	–10

6.7. RF, Magnetic, and Common Mode Transient Immunity

The Si8220/21 families have very high common mode transient immunity while transmitting data. This is typically measured by applying a square pulse with very fast rise/fall times between the isolated grounds. Measurements show no failures at 30 kV/µs (minimum). During a high surge event, the output may glitch low for up to 20–30 ns, but the output corrects immediately after the surge event.

The Si8220/21 families pass the industrial requirements of CISPR24 for RF immunity of 10 V/m using an unshielded evaluation board. As shown in Figure 16, the isolated ground planes form a parasitic dipole antenna. The PCB should be laid-out to not act as an efficient antenna for the RF frequency of interest. RF susceptibility is also significantly reduced when the end system is housed in a metal enclosure, or otherwise shielded.

The Si8220/21 digital isolator can be used in close proximity to large motors and various other magnetic-field producing equipment. In theory, data transmission errors can occur if the magnetic field is too large and the field is too close to the isolator. However, in actual use, the Si8220/21 devices provide extremely high immunity to external magnetic fields and have been independently evaluated to withstand magnetic fields of at least 1000 A/m according to the IEC 61000-4-8 and IEC 61000-4-9 specifications.

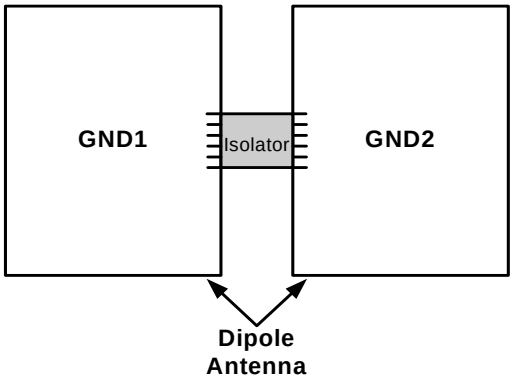


Figure 16. Dipole Antenna

7. Pin Descriptions (Narrow-Body SOIC)

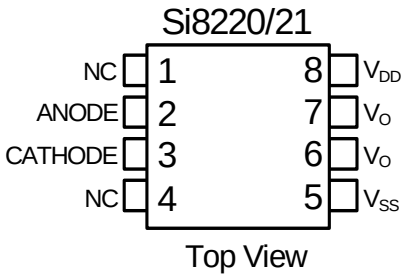


Figure 17. Pin Configuration

Table 13. Pin Descriptions (Narrow-Body SOIC)

Pin	Name	Description
1	NC	No connect.
2	ANODE	Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input.
3	CATHODE	Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input.
4	NC	No connect.
5	V_{SS}	External MOSFET source connection and ground reference for V_{DD}. This terminal is typically connected to ground but may be tied to a negative or positive voltage.
6	V_O	Output signal. Pins 6 and 7 are connected together internally.
7	V_O	Output signal. Pins 6 and 7 are connected together internally.
8	V_{DD}	Output-side power supply input referenced to V_{SS} (24 V max).
***Note:** No Connect. These pins are not internally connected.		

8. Pin Descriptions (Wide-Body SOIC)

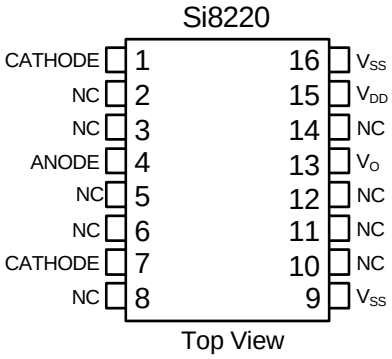
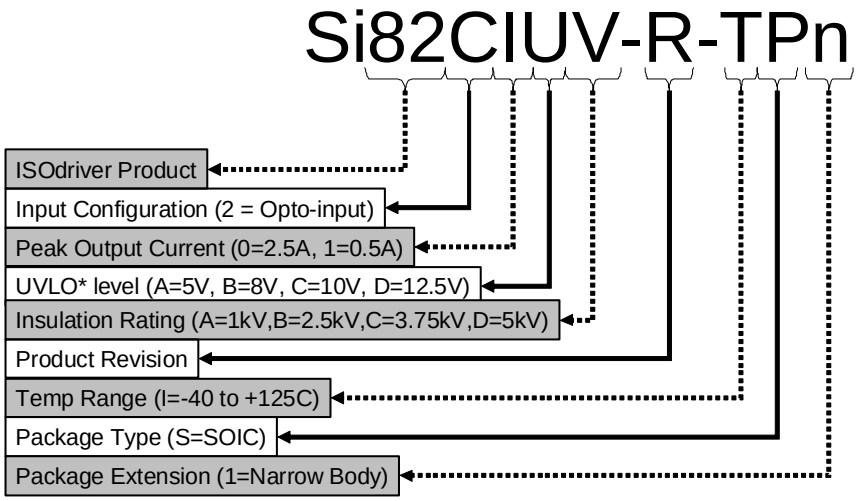


Table 14. Pin Descriptions (Wide-Body SOIC)

Pin	Name	Description
1,7	CATHODE	Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input.
2,3,5,6,8, 10,11,12, 14	NC*	No connect.
4	ANODE	Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input.
9,16	V_{SS}	External MOSFET source connection and ground reference for V_{DD}. This terminal is typically connected to ground but may be tied to a negative or positive voltage.
13	V_O	Output signal.
15	V_{DD}	Output-side power supply input referenced to V_{SS} (24 V max).
***Note:** No Connect. These pins are not internally connected.		

9. Ordering Guide

Not all possible device configuration options and their corresponding ordering part numbers (OPN) are included in the Ordering Guide table. However, if there is a specific device configuration of interest that is currently not listed in the Ordering Guide table, please contact your local Silicon Labs sales representative, or go to the Silicon Labs Technical Support web page at https://www.silabs.com/support/pages/contacttechnicalsupport.aspx and register to submit a request to create your specific device configuration and OPN.



*UVLO= Under Voltage Lock Out

Figure 18. Si8220/21 OPN Naming Convention

Table 15. Si8220/21 Ordering Guide*

New Ordering Part Number (OPN)	Ordering Options					
	Input Configuration	Peak Output Current (Cross Reference)	UVLO Voltage	Insulation Rating	Temp Range	Pkg Type
Si8220BB-A-IS	Opto input	2.5 A (HCPL-3120)	8 V default	2.5 kVrms	–40 to +125 °C	SOIC-8
Si8220CB-A-IS	Opto input	2.5 A (HCPL-3120)	10 V	2.5 kVrms	–40 to +125 °C	SOIC-8
Si8220DB-A-IS	Opto input	2.5 A (HCPL-3120)	12.5 V	2.5 kVrms	–40 to +125 °C	SOIC-8
Si8220BD-A-IS	Opto input	2.5 A (HCPL-3120)	8 V default	5.0 kVrms	–40 to +125 °C	WB SOIC-16
Si8220CD-A-IS	Opto input	2.5 A (HCPL-3120)	10 V	5.0 kVrms	–40 to +125 °C	WB SOIC-16
Si8220DD-A-IS	Opto input	2.5 A (HCPL-3120)	12.5 V	5.0 kVrms	–40 to +125 °C	WB SOIC-16
Si8221CC-A-IS	Opto input	0.5 A (HCPL-0302)	10 V	3.75 kVrms	–40 to +125 °C	SOIC-8
Si8221DC-A-IS	Opto input	0.5 A (HCPL-0302)	12.5 V	3.75 kVrms	–40 to +125 °C	SOIC-8

***Note:** All packages are RoHS-compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.

10. Package Outline: 8-Pin Narrow Body SOIC

Figure 19 illustrates the package details for the Si822x. Table 16 lists the values for the dimensions shown in the illustration.

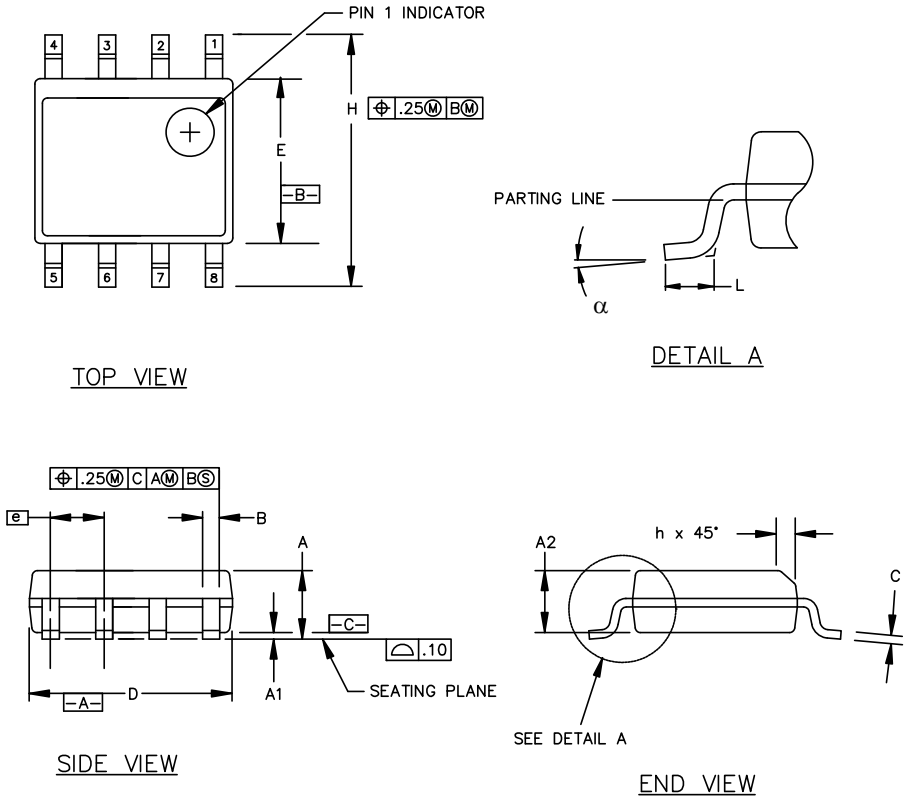


Figure 19. 8-pin Small Outline Integrated Circuit (SOIC) Package

Table 16. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
∝	0°	8°

11. Land Pattern: 8-Pin Narrow Body SOIC

Figure 20 illustrates the recommended land pattern details for the Si822x in an 8-pin narrow-body SOIC. Table 17 lists the values for the dimensions shown in the illustration.

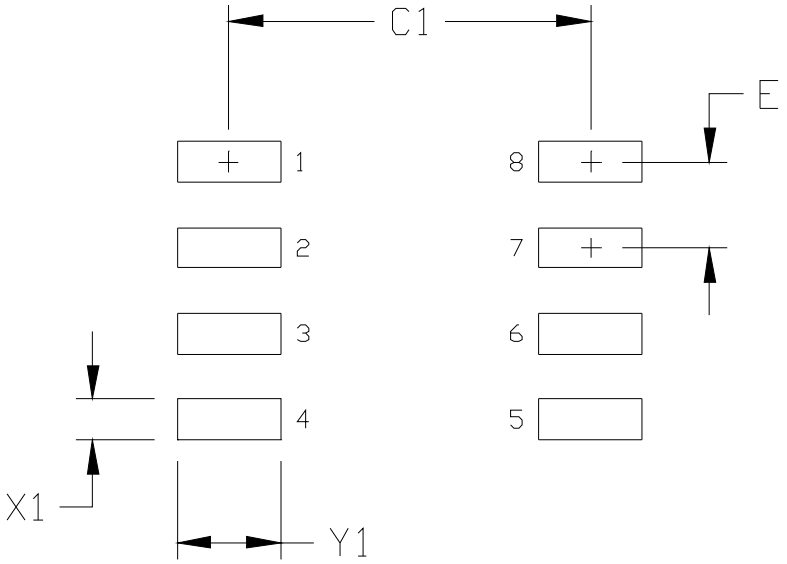


Figure 20. PCB Land Pattern: 8-Pin Narrow Body SOIC

Table 17. PCM Land Pattern Dimensions (8-Pin Narrow Body SOIC)

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

12. Package Outline: 16-Pin Wide Body SOIC

Figure 21 illustrates the package details for the Si822x Digital Isolator. Table 18 lists the values for the dimensions shown in the illustration.

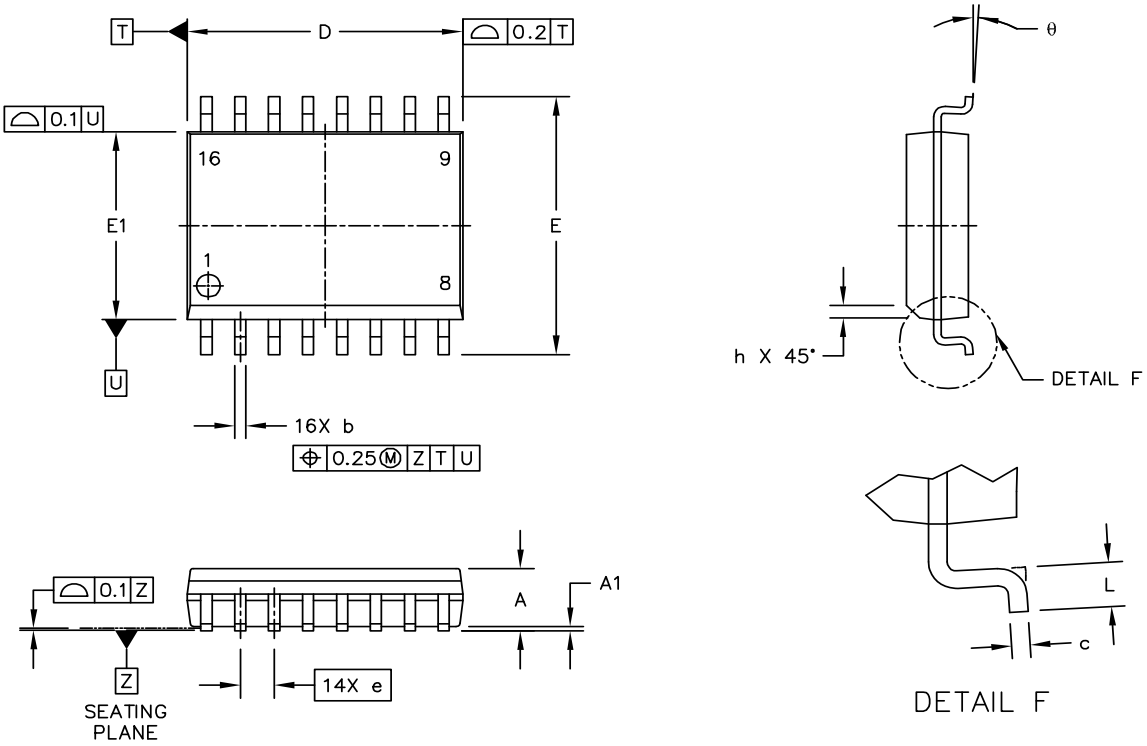


Figure 21. 16-Pin Wide Body SOIC

Table 18. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.1	0.3
D	10.3 BSC	
E	10.3 BSC	
E1	7.5 BSC	
b	0.31	0.51
c	0.20	0.33
e	1.27 BSC	
h	0.25	0.75
L	0.4	1.27
θ	0°	7°

13. Land Pattern: 16-Pin Wide-Body SOIC

Figure 22 illustrates the recommended land pattern details for the Si822x in a 16-pin wide-body SOIC. Table 19 lists the values for the dimensions shown in the illustration.

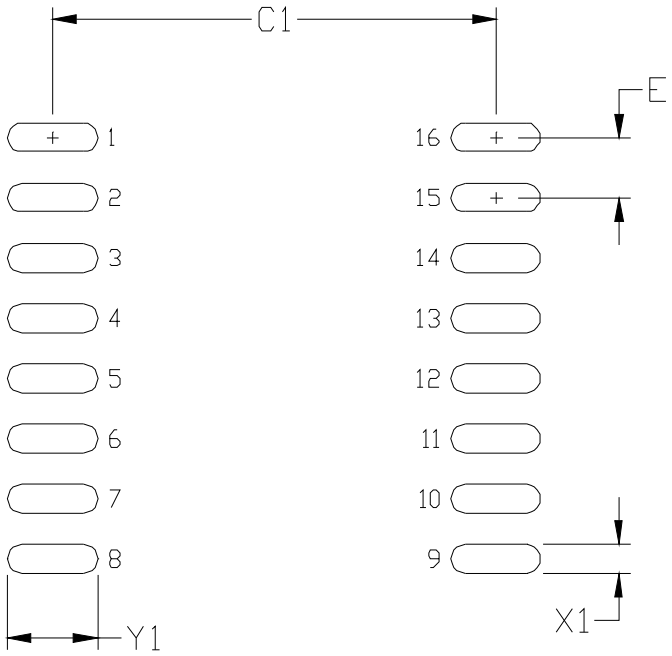


Figure 22. 16-Pin SOIC Land Pattern

Table 19. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

NOTES:

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