GM82C765B
FLOPPY DISK SUBSYSTEM CONTROLLER

General Description

The GM82C765B is a CMOS LSI device which interfaces a host microprocessor to the floppy disk drive. It integrates the function of the Formatter/Controller, Data Separator. Write Precompensation, Data rate selection, Clock Generation, High Current Output Drivers, and TTL compatible Schmitt Trigger Receivers. The GM82C765B consists of a microprocessor interface, a microsequencer and a disk drive interface.

The host microprocessor interface of the GM82C765B supports a 12MHz, 286 microprocessor bus without the use of wait states. All inputs within host microprocessor are Schmitt triggers, except for the data bus, XTAL, and the host output sink 12mA.

Output drive capability is 20 LSTTL load, allowing direct interconnection to bus structures without the use of buffers or transceivers. On the disk drive interface, the GM82C765B includes data seperation that has been designed to address high performance error rate on floppy disk drives, and contains all the necessary logic to achieve classical 2nd order, type2, phase locked loop performance. Write precompensation is included, in addition to the usual formatting, encoding, decoding, step motor control, and status sensing functions For PC/XT and PC/AT applications, the device provides qualification of interrupt and DMA requests.

The disk drive interface of the GM82C765B connects directly to up to four drives. All drive-related inputs are Schmitt triggers and the drive outputs are open drain, and sink 48 mA.

The GM82C765B uses two clock inputs which provide the necessary signals for internal timing. A 16MHz oscillator controls the data rate of 500, 250 and 125Kbits/sec, while a 9.6MHz oscillator controls the 300Kbit/sec data rate used in PC/AT designs.

The two XTAL oscillator circuits may be used for the 44-pin PLCC package, while TTL clock inputs must be provided when using the 40-pin DIP package.
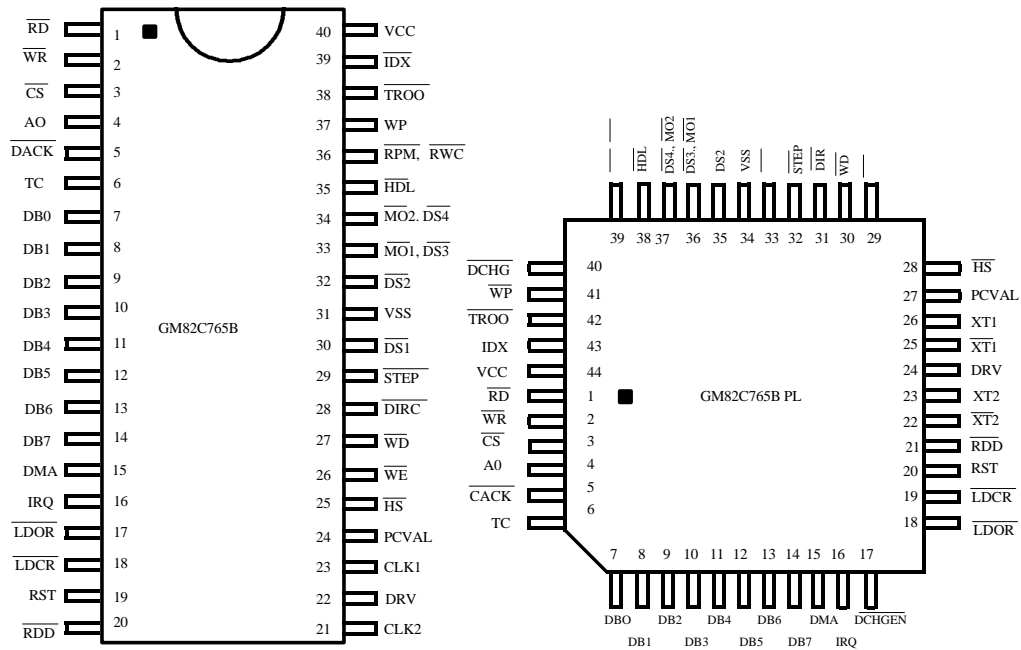
In the PLCC version of the GM82C765B pins 17 and 40, which were not utilized in DIP version of the GM82C765B, became $\overline{DCHGEN}$ (Disk Change Enable) and $\overline{DCHG}$ (Disk Change) respectively. Both are active LOW. $\overline{DCHGEN}$ is offered as an option for those designs that used the original GM82C765B part where $\overline{DCHG}$ did not exist as direct into the chip.

The GM82C765B has eight internal Registers. The 8 bit main status register contains status information of the GM82C765B and may be accessed any time. Another four status register under system control also give various status and error information. The Control Register provides support logic that latches the two LSBs used to select the desired data rate that controls internal clock generation. The Operations Register replaces the standard latched port used in floppy subsystem.

Features

* IBM PC compatible format (single and double density)
  – Floppy disk control and operations on chip
  – In PC AT mode, provides required signal qualification DMA channel
  – BIOS compatible and dual speed Spindle Drive support
* Integrates Formatter/Controller/Data Separation, Write Precompensation, Data rate Selection, Clock Generation, and drive interface Drivers and Receivers into one chip
* Multisector and Multitrack transfer capability.
* Direct Floppy Disk Drive interface with no buffers needed
  – 48mA sink output drivers
  – Schmitt trigger Line Receivers
* Enhanced Host Interface:
  – Supports 12MHz, 286 u-processor
  – Capable of driving 20 LSTTL Load
* Address mark detection circuitary internal to Floppy Disk Controller
* On chip Clock Generation Two TTL Clock Inputs for 40-DIP
* Two XTAL oscillator circuits for 44-Quad, PLCC
* User programmable Track Stepping Rate and Head load/unload time
* Drivers up to four Floppy or micro Floppy Disk Drives
* Data transfer DMA or non-DMA mode
* Parallel seek operations on up to four Drives
* Internal power up reset circuitry
* READ/WRITE access compatible register with 8 or 12MHz 286 microprocessor with 0 wait states.
* DMA timing corrected.
* LOW POWER CMOS, +5V SUPPLY

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Pin Configuration

1. Pin Descriptions

PIN NO		MNEMOMIC	SIGNAL NAME	I/O	FUNCTION
DIP	PLCC				
1	1	$\overline{RD}$	$\overline{READ}$	I ST	Control Signal for transfer of data or status onto the data bus by the GM82C765B
2	2	$\overline{WR}$	$\overline{WRITE}$	I	Control signal for latching data form the bus into the GM82C765B buffer register.
3	3	$\overline{CS}$	$\overline{CHIP\ SELECT}$	ST	Selected when 0 (Low) allowing $\overline{RD}$ or $\overline{WR}$ operation from the host
4	4	A0	ADDRESS LINE	I ST	Address line selecting data (=1) or status (=0) information (A0 = Logic 0 during $\overline{WR}$ is illegal)
5	5	$\overline{DACK}$	$\overline{DMA}$ $\overline{ACKNOWLEDGE}$	I ST	Used by the DMA Controller to transfer data from the GM82C765B onto the bus. Logical equivalent to $\overline{CS}$ and A0=1. In special or PC AT mode, this signal is qualified by DMAEN from the Operation Register.

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PIN		MENMO -MIC	SIGNAL NAME	I/O	FUNCTION
DIP	PLCC				
6	6	TC	TERMINAL COUNT	I ST	This signal indicates to GM82C765B that data transfer is complete. If DMA operational mode is selected for command execution, TC will be qualified by $\overline{DACK}$, but not in the programmed I/O execution. In PC AT or Special mode, qualification by $\overline{DACK}$ requires the Operations mode, qualification by $\overline{DACK}$ requires the operations resister signal DMAEN to be logically true. Note also that in PC AT mode, TC will be qualified by $\overline{DACK}$, whether in DMA or non-DMA host operation. programmed I/O in PC AT mode will cause an abnormal termination error at the completion of a command.
7-14	7-14	DBO thru DB7	DATA BUS 0 Thru DATA BUS 7	I/O BI	8-Bit bi-directional, tri-state, data bus. D0 is the least significant bit (LSB). D7 is the most significant bit (MSB)
15	15	DMA	DIRECT MEMORY ACCESS	O BI	DMA request for byte transfer of data. In Special or PC AT mode, this pin is tristated, enabled by the DMAEN signal from the Operation Register. This pin is driven in the Base mode.
16	16	IRQ	INTERRUPT REQUEST	O BI	Interrupt request indicating the completion of command execution or data transfer requests (in non DMA mode). Normally driven in base mode. In special or PC AT mode, this pin is tri-stated, enabled by the DMAEN signal from the Operations Resister.
	17	$\overline{DCHGEN}$	$\overline{DISK}$ $\overline{CHANGE}$ $\overline{ENABLE}$	I ST	This input must be at logic = 0 to enable $\overline{DCHG}$ input status at pin 40 to be placed on DB7 during a $\overline{RD}$ = 0 of $\overline{LDCR}$ = 0. Internal pull-up.
17	18	$\overline{LDOR}$	$\overline{LOAD}$ $\overline{OPERATIONS}$ REGISTER	I ST	Address decode which enables the loading of the Operations Resister. Internally gated with $\overline{WR}$ creates the strobe which latches the two LSBS from the data bus into the Operation Resister.
18	19	$\overline{LDCR}$	$\overline{LOAD}$ $\overline{CINTROL}$ REGISTER	I ST	Address decode which enables the loading of the Control Resister. Internally gated with $\overline{WR}$ creates the strobe which latches the two LSRs from thedata bus into the Control Resister.
19	20	RST	RESET	I ST	Reset controller, placing microsequencer in idle. Resets device outputs. Puts in base mode, not PC AT or Special mode.
20	21	$\overline{RDD}$	$\overline{READ\ DISK}$ $\overline{DATA}$	I ST	This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data.
	22	$\overline{XT2}$	$\overline{XTAL2}$	O N	XTAL oscillator drive output for 44 pin PLCC should be left floating if TTL inputs used at pin 23.
	23	XT2	XTAL2	I N	XTAL oscillator input used for non-standard data rates. It may be driven with a TTL level signal
21		CLK2	CLOCK2	I N	TTL level clock input used for non-standard data rates is 9.6MHz for 300 kbs, and can only be selected from the Control Register. * XT2 (PIN23) of 44 pin-PLCC

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22	24	DRV	DRIVE TYPE	I ST	Drive type input indicates to the device that a two-speed spindle motor is used if logic is O. In that case, the second clock input will never be selected and must be grounded.
	25	$\overline{XI1}$	$\overline{XTAL1}$	O ST	XTAL oscillator drive output for 44 pin PLCC should be left floating if TTL inputs used at pin 26.
	26	XT1	XTAL1	I N	XTAL oscillator input requiring 16MHz crystal. This oscillator is used for all standard data rates, and may be driven with a TTL level signal.
23		CLK1	CLOCK1	I N	TTL level clock input is used to generate all internal timings for standard data rates. Frequency must be 16MHz $\pm$0.1%, and may 40/60 or 60/40 duty cycle. * XT1 (PIN 26) of 44-PLCC
24	27	PCVAL	PRECOMPEN-SATION VALUE	I ST	PRECOMPENSATION VALUE select input. This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1 = 125nS, Logic 0 = 187nS
25	28	$\overline{HS}$	$\overline{HEAD}$ $\overline{SELECT}$	O HCD	High Current drive (HCD) output selects the head (side) of the floppy disk that is being read or written. Logic 1 = side 0. Logic 0 = side 1.
26	29	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	O HCD	This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head.
27	30	$\overline{WD}$	$\overline{WRITE\ DATA}$	O HCD	This HCD output $\overline{WRITE\ DATA}$. Each failing edge of the encoded data pulse stream causes a flux transition on the media.
28	31	$\overline{DIRC}$	$\overline{DIRECTION}$	O HCD	This HCD output determines the direction of the HEAD step motor. Logic 1 = outward motion. Logic 0 = inward motion.
29	32	$\overline{STEP}$	$\overline{STEP\ PULSE}$ $\overline{CONTROL}$	O HCD	This HCD output issues an active low pulse for each track to track movement of the head.
30	33	$\overline{DS1}$	$\overline{DRIVE\ SELECT1}$	O HCD	This HCD output, when active low, is $\overline{DRIVE\ SELECT1}$ in PC AT mode, enables the interface in disk drive. This signal comes from the Operations Register. In Base or Special mode, this output is #1 of the four decoded Unit Selects, as specified in the device command syntax.
31	34	VSS	GROUND		Ground
32	35	$\overline{DS2}$	$\overline{DRIVE\ SELECT2}$	O HCD	This HCD output, when active low, is $\overline{DRIVE\ SELECT2}$ in PC AT mode, enables the interface in disk drive. This signal comes from the Operations Register. In Base or Special mode, this output is # 2 of the four decoded Unit Selects, as specified in the device command syntax.
33	36	$\overline{MO1}$, $\overline{DS3}$	$\overline{MOTOR\ ON\ 1}$ $\overline{DRIVE\ SELECT3}$	O HCD	This HCD output, when active low, is MOTOR ON enable for disk drive #1, in PC AT mode. This signal comes from the OPERATIONS Register in the BASE or Special mode, this output is #3 of the four decoded Unit Selects as specified in the device command syntax.

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PIN NO		MNEMOM	SIGNAL NAME	I/O	FUNCTION
DIP	PLCC				
34	37	$\overline{\text{MO2}}$, $\overline{\text{DS4}}$	$\overline{\text{MOTOR ON 2}}$ $\overline{\text{DRIVE SELECT4}}$	O HCD	This HCD output, when active low, is MOTOR ON enable for disk drive #2, in PC AT mode. This signal comes from the Operations Reg. In the Base or Special mode, this output is #4 of the four decoded Unit Selects as specified in the device command syntax
35	38	$\overline{\text{HDL}}$	$\overline{\text{HEAD}}$ $\overline{\text{LOADED}}$	O HCD	This HCD output, when active low, causes the head to be loaded against the media in the selected drive.
36	39	$\overline{\text{RWC}}$ $\overline{\text{RPM}}$	$\overline{\text{REDUCED}}$ $\overline{\text{WRITE}}$ $\overline{\text{CURRENT,}}$ $\overline{\text{REVOLUTIONS}}$ PER MINUTE	O HCD	This HCD output, when active los, causes a $\overline{\text{REDUCED}}$ $\overline{\text{WRITE CURRENT}}$ when bit density is increased toward the inner tracks, becoming active when tracks>28 are accessed. This condition is valid for Base or Special mode, and is indicative of when write precompensation is necessary. In the PC AT mode, this signal will be active when CR0=1
	40	$\overline{\text{DCHG}}$	$\overline{\text{DISK}}$ $\overline{\text{CHANGE}}$	I ST	This ST input senses status from the drive, indicating active low that drive door is open or that the diskette has possibly changed since last drive selection.
37	41	$\overline{\text{WP}}$	$\overline{\text{WRITE}}$ $\overline{\text{PROTECTED}}$	I ST	This Schmitt Trigger (ST) input senses status from the disk drive, indicating active low when a diskette is $\overline{\text{WRITE}}$ $\overline{\text{PROTECTED}}$
38	42	$\overline{\text{TR00}}$	$\overline{\text{TRACK 00}}$	I ST	This ST input senses status from disk drive indicating active low when the head is positioned over the outermost track, $\overline{\text{TRACK 00}}$
39	43	$\overline{\text{IDX}}$	$\overline{\text{INDEX}}$	I ST	This ST input senses status from the disk drive, indicating active low when the head is positioned over the beginning of a track marked by an index hole.
40	44	VCC	+5V DC		Input power supply.

Note: N – NORMAL INPUT, OUTPUT PAD

BI – BIDIRECTIONAL I/O PAD

ST – SCHMITT TRIGGER INPUT PAD

HCD – OPEN DRAIN HIGH CURRENT DRIVE OUTPUT PAD

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2. Electrical Specifications.

2.1 Absolute Maximum Ratings
—OPERATING TEMPERATURE …………………….....0°C (32°F) to 70°C (158°F)
—STORAGE TEMPERATURE …………………..-55°C (-67°F) to +125°C (257°F)
—VOLTAGE on any pin with respect to ground ……………-0.3 V to Vcc +0.3V
—SUPPLY VOLTAGE with respect to ground ……………………....7.0 V………………

2.2 DC ELECTRICAL CHARACTERISTICS

NOTE: Maximum limits indicate where permanent device damage occurs.

Continous operation at these limits is not intended and should be limited to those conditions specified in the DC operating Characteristics

DC Operating Caracteristics: $T_A = 0°C\,(32°F)$ to $70°C\,(158°F)$; $V_{CC} = 5V \pm 10\%$

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{CC}	+5V DC POWER SUPPLY	4.5	5.5	V
VIL	Input LOW Voltage-DATA BUS & XTOSC		0.8	V
VIH	Input HIGH Voltage-DATA BUS & XTOSC	2.0		V
VILT	Input LOW Threshold Voltage-Schmitt Trigger	0.8		V
VIHT	Input HIGH Threshold Voltage-Schmitt Trigger		2.0	V
VOL	Output LOW-DBX, IRQ, DMA: lo=12.0mA		0.4	V
VOH	Output HIGH-DBX, IRQ, DMA: lo=-5.0mA	2.8		V
VOLHC	Output LOW-HIGH CURRENT: lo=48mA		0.4	V
ILUL	Latch up CURRENT LOW	40.0		mA
ILUH	Latch up CURRENT HIGH	-40.0		mA
ILLX	Leakage CURRENT LOW		20.0	mA
ILHX	Leakage CURRENT HIGH		-20.0	mA
ICC	Supply Current-100uA source Loads		45.0	mA
ICCHL	Supply Current-5mA source Loads		95.0	mA
PD	Power Dissipation-ICC Max*		425.0	mA
PDHL	Power Dissipation-ICCHL Max*		575.0	mA
VPQR	Power Qualified Reset Threshold	2.8	4.35	V

NOTE:*:Includes open DRAIN High current drives at VOL=0.4V

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2.3 AC Timing Specifications

$TA = 0°C\,(32°F)$ to $70°C\,(158°F)$: $VCC = +5V \pm 10\%$: $CL = 100\,pF$

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{CY}	Clock Period	60		nS
t_{PH}	Clock Active (High or Low)	25		nS
t_R	Clock Rise Time (Vin 0.8 to 2.0)		5	nS
t_F	Clock Fall Time (Vin 2.0 to 0.8)		5	nS
t_{AR}	A0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ Low	0		nS
t_{RA}	A0, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ High	0		nS
t_{RR}	$\overline{RD}$ Width	90		nS
t_{RD}	Data Access Time from $\overline{RD}$ Low		90	nS
t_{DF}	DB To Float Delay from $\overline{RD}$ High	10	65	nS
t_{AW}	A0, $\overline{CS}$, $\overline{DACK}$, $\overline{LDCR}$, $\overline{LDOR}$, Set Up Time to $\overline{WR}$ Low	0		nS
t_{WA}	A0, $\overline{CS}$, $\overline{DACK}$, $\overline{LDCR}$, $\overline{LDOR}$, Hold Time from $\overline{WR}$ High	0		nS
t_{WW}	$\overline{WR}$ Width	60		nS
t_{DW}	Data Set Up Time to $\overline{WR}$ High	80		nS
t_{WD}	Data Hold Time from $\overline{WR}$ High	0		nS
t_{RI}	IRQ Reset Delay Time from $\overline{RD}$ High	0	1MCY + 150nS	
t_{WI}	IRQ Reset Delay Time from $\overline{WR}$ High	0	1MCY + 150nS	
t_{MCY}	DMA Cycle Time	52		MCY
t_{AM}	DMA Reset Delay Time from $\overline{DACK}$ Low		140	nS
t_{MA}	$\overline{DACK}$ Delay Time from DMA High	0		nS
t_{AA}	$\overline{DACK}$ Width	90		nS
t_{TC}	TC Width	60		nS
t_{RST}	Reset Width-TTL Driven CLK1	250		nS
t_{SRST}	Reset Width-Software Reset	5		MCY
t_{RDD}	$\overline{RDD}$ Active Time Low	40		nS
t_{WDD}	$\overline{WD}$ Write Data Width Low	1/2 (TYP)		MCY
t_{DST}	$\overline{DIRC}$ Hold & Set Up to $\overline{STEP}$ Low	4		MCY
t_{STU}	$\overline{DSX}$ Hold Time from $\overline{STEP}$ Low	20		MCY
t_{STP}	$\overline{STEP}$ Active Time Low	24		MCY
t_{SC}	$\overline{STEP}$ Cycle Time	132		MCY

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| SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{IDX}	$\overline{IDX}$ Index Pulse Width	2		MCY
t_{STD}	$\overline{DIRC}$ Hold Time after $\overline{STEP}$	96		MCY
t_{MR}	$\overline{RD}$ Delay from DMA	0		nS
t_{MW}	$\overline{WR}$ Delay from DMA	0		nS
t_{MRW}	$\overline{RD}$ or $\overline{WR}$ Response from DMA High		48	MCY
t_{CA}	Chip Access Delay from RST Low-TTL	32		MCY
t_{CAS}	Chip Access Delay from t_{SRST} Low	40		MCY
t_{XCA}	Chip Access Delay from RST-OSC XT1 at 16MHz	500	uS	
t_{XTS}	XT2 Access Delay after RST 9.6MHz	1000		uS
t_{TCR}	TC Delay from Last DMA or IRQ, $\overline{RD}$	0	192	MCY
t_{TCW}	TC Delay from Last DMA or IRQ, $\overline{WR}$	0	384	MCY

Note: CY specifies CLK1 or XT1 period

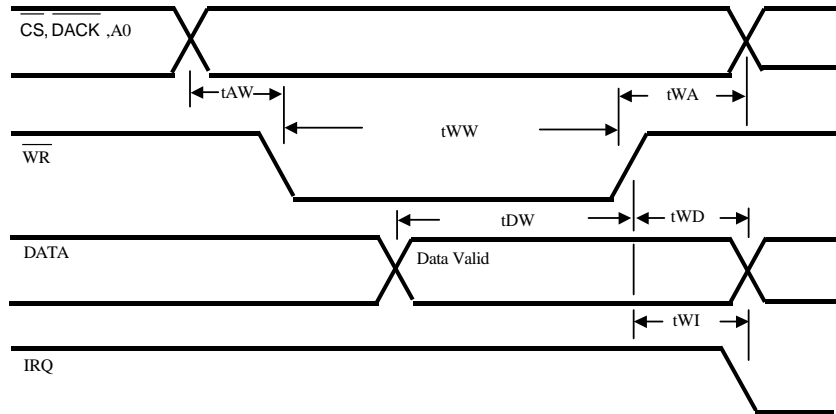MCY specifies MCLK period, dependent on selected data rate

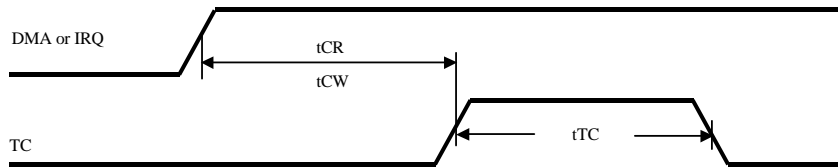WCY specifies WCLK period, dependent on selected data rate
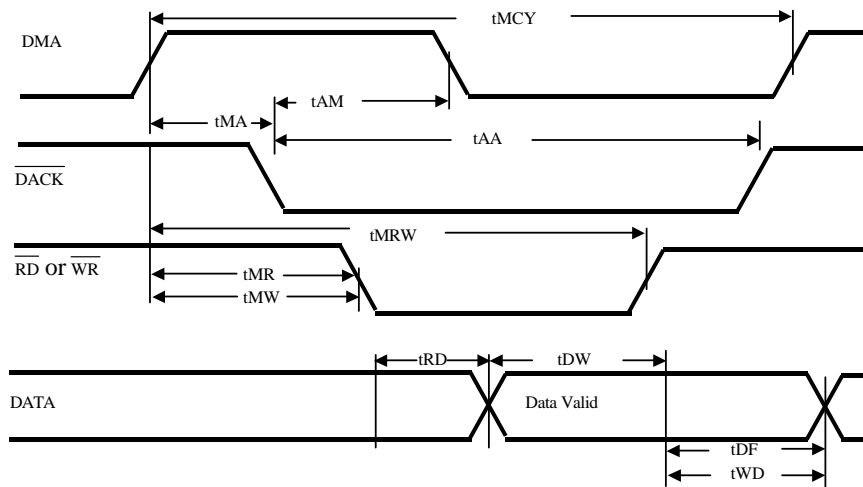
2.4 AC Timing Diagrams
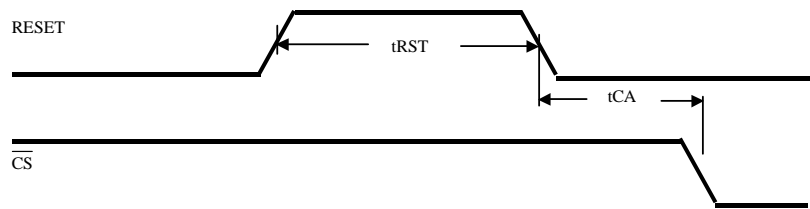
(1) READ Timing
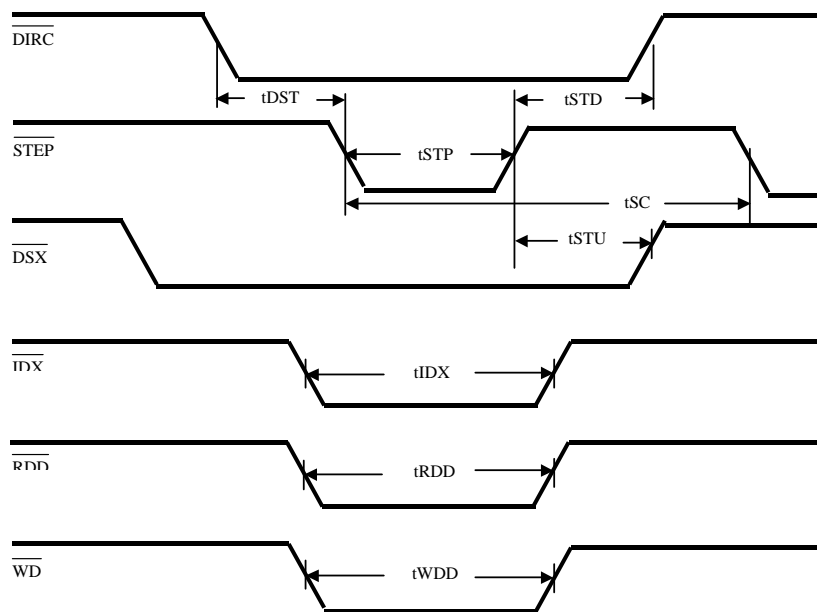

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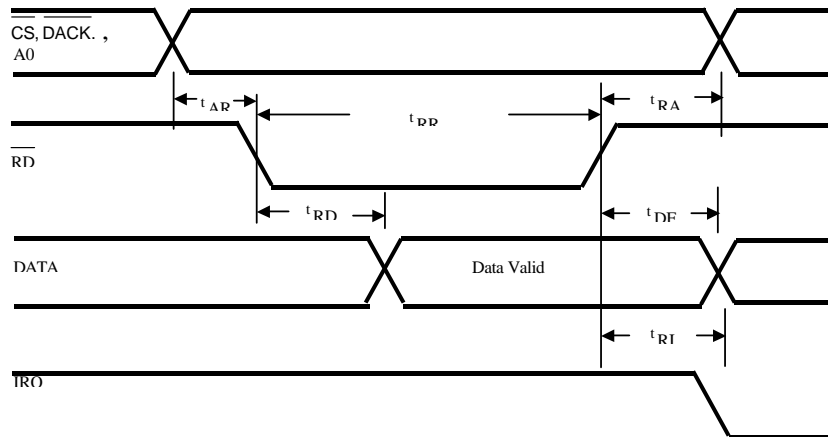
(2) WRITE Timing
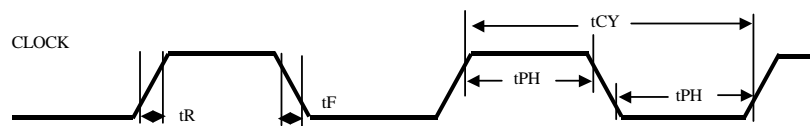

(3) TERMINAL COUNT (TC) COUNTING

(4) DMA TIMING

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(5) RESET Timing

(6) DISK DRIVE SELECT TIMING

(7) CLOCK Timing

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3. ARCHITECTURE

HOST INTERFACE

The GM82C765B Floppy Disk Subsystem Controller is a CMOS LSI device that provides all the needed functionality between the host u-processor peripheral Bus and the cable Connec-tor to the Floppy Disk Drive. This CHIP in-tegrates; Formatter/Controller Data Separation, Write Precompensation, Data rate Seletion, Clock generation, Drive interface drivers and receivers.

The host interface is the host microprocessor peripheral bus. This bus is composed of eight control signals and eight data signals. In the special or PC AT modes, IRQ and DMA request are tri-stated and qualified enable, internally provided by the operations register. The data bus, DMA, and IRQ outputs are designed to handle 20 LS-TTL loading.
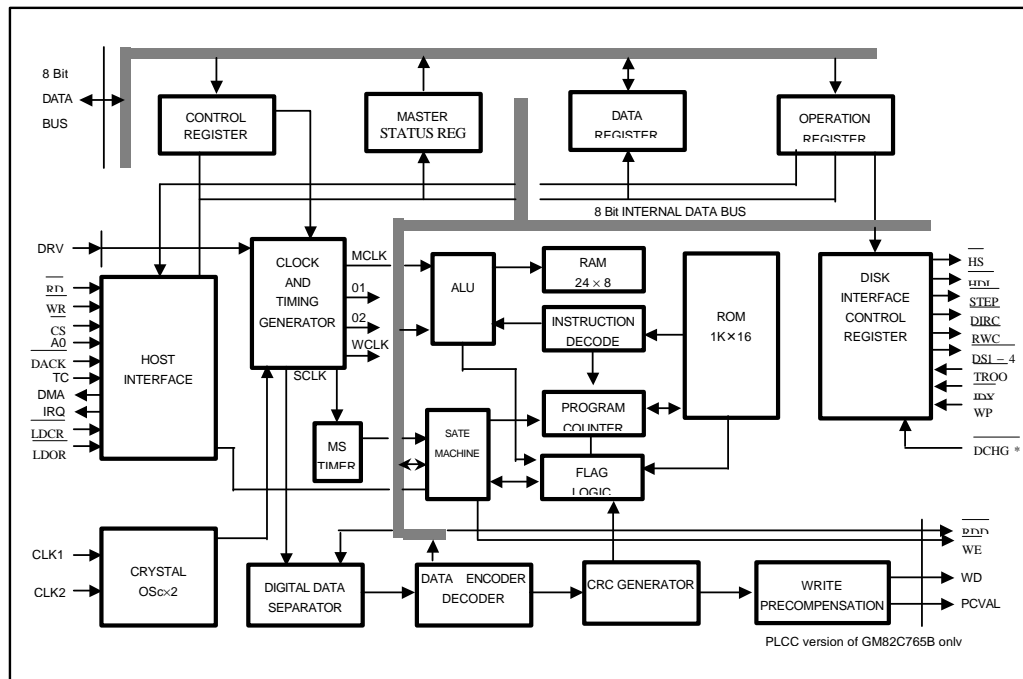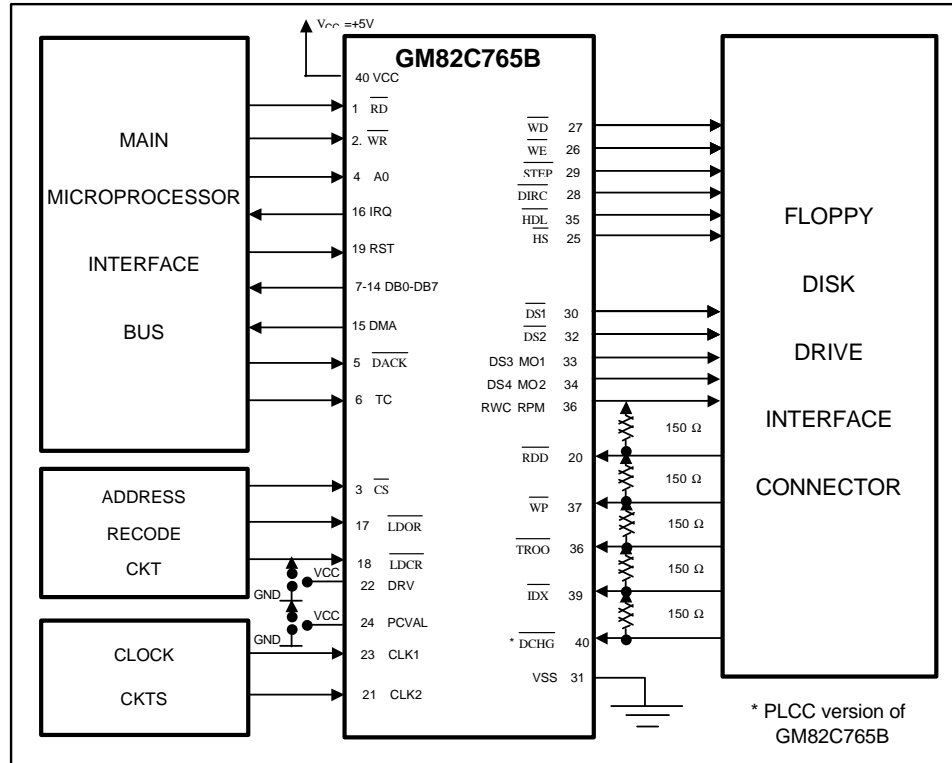
Fig 1. GM82C765B Internal Block Diagram

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Fig 2. TYPICAL GM 82C765B APPLICATION SYSTEM

Inputs, except the data bus, are Schmitt trig-ger receivers and can be hooked up to a bus or backplane without any additional buffering.

During the command or result phases, the main status Register must be ready by the processor before each byte of information is written into or read from the data Register. After each byte of data is read from or written into the data Register, the CPU should wait for 12uS before reading the main status Register. Bits D6 and D7 in the main status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the GM82C765B. Many of the command require multiple bytes. As a result, the Main status Register must be read prior to each byte transfer to the GM82C765B. During the result phase,

Bits D6 and D7 in the Main status Register must both be 1's (D6-1 and D7-1) before reading each byte from the Data Register. Note that this regarding of the main status Register before each byte transfer to the GM82C765B is re-quired only in the Command and result phases, and not during the Execution phase. Note also that DB6 and DB7 in the MSR can be polled in-stead of waiting 12uS. When they have the right bit settings, the GM82C765B is ready for com-mands. This might save some time.

During the Execution phase, the main status register need not be read. If the GM82C765B is in the non-DMA Mode, then the receipt of each data byte is indicated by an interrupt signal on pin 16 (IRQ-1). The generation of a Read signal (RD-0) will clear the interrupt as well as

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output the data onto the data bus.

If the processor can not handle interrupt fast enough (every 13uS for the MFM mode and 27uS for the FM mode), then it may poll the main status Register and bit D7 (RQM) functions as the Interrupt signal.

If a Write Command is in process then the $\overline{WR}$ Signal performs the reset to the Interrupt signal.

All timings mentioned above double for mini floppy data rates. Note that in the non-DMA mode it is necessary to examine the main Status Register to determine the cause of the interrupt signs is could be a data interrupt or a command terminaton interrupt, either normal or abnormal. If the GM82C765B is in the DMA mode, no inter-rupt signals are generated during the Execution phase. This signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, the Interrupt is auto-matically cleared (IRQ=0). It should be noted that in PC AT usage, non-DMA Host transfers and not the normal procedure. If the user chooses to do so, the GM82C765B will successfully complete commands, but will always give abnormal termination error status since TC is qualified by an inactive $\overline{DACK}$.

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while Dack is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed I/O operations.

If the non-DAM mode is chosen, the $\overline{DACK}$ signal should be pulled up to V_{CC}. It is important to note that during the Result phase all bytes shown in the Command Table must be read. The Read Data Command for example, has several bytes of data in the Result phase. All seven bytes must be read Data command. The GM82C765B will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result phase. The GM82C765B contains five Status Registers. The Main Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only after completing a command.

The particular command that has been executed determines how many of the Status Registers will be read.

The byte of data which are sent to the GM82765B to form the command phase, and are read out of the GM82C765B in the result phase, must occur in the order shown in the command Table. The command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the command or Result phase is allowed. After the last byte of data in the Command phase is sent to the GM83C765B, the Execution phase of automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the GM82C765B is ready for a new command.

CONTROL REGISTER

The Control Register provides support logic that latches the two LSBs of the data bus upon receiving $\overline{LDCR}$ and $\overline{WR}$. $\overline{CS}$ should not be active when this happens. These bits are used to select the desired data rate, which in turn controls the internal clock generation. Clock switchover is internally "deglitched" allowing continuous operation after change data rates.

If the Control Register is not used, the data rate is governed by the supplied clock or crystal. The frequency must be 64X the desired MFM data rate, up to a maximum frequency of 16 MHz. This implies a maximum data rate of 250 kb/S. unless the Control Register is used. Switching this clock must be "glitchless" or the device will need to be reset.

Table 1 presents the Control Register.

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TABLE 1. CONTROL REGISTER

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (In PC AT MODE)
0	0	X	500K	MFM	1
0	0	X	250K	FM	1
0	1	0	250K	MFM	0
0	1	1	300K	MFM	0
1	0	X	250K	MFM, RST Default	1
1	0	X	125K	FM, RST Default	1
1	1	X	125K		0

MASTER STATUS REGISTER

The Master Status Register is an eight-bit register that contains the status information of the FDC, any may be accessed at any time. Only the Master Status Register may be read and used to facilitate the transfer of data between the processor and GM82C765B. The DIO and RQM bits in the Master Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during a Command or Result phase and DIO and RQM getting set is 12us if 500 kb/S MFM data rate is selected. (If 250 kb/s MFM is selected, the delay is 24uS.) For this reason, everytime the Master Status Register is read, the CPU should 12us. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB4 (FDC busy) goes low is 12 uS.

TABLE 2. MASTER STATUS REGISTER BITs

BIT			DESCRIPTION
NO.	NAME	SYMBOL	
DB0	FDD 0 BUSY	D0B	FDD number 0 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB1	FDD 1 BUSY	D1B	FDD number 1 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB2	FDD 2 BUSY	D2B	FDD number 2 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB3	FDD 3 BUSY	D3B	FDD number 3 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB4	FDC BUSY	CB	A READ or READ command is in progress. FDC will not accept any other commands.
DB5	EXECUTION MODE	EXM	This bit is set only during Execution phase in non-DMA Mode. When DBS goes low Execution phase has ended and Results phase has started. It operates only during non-DMA Mode of operation.
DB6	DATA INPUT	DI0	Indicates direction of data transfer between FDC and DATA Register. If DIO=1, then transfer is from DATA Register to the Processor. If DIO=0, transfer is from Processor to the Data Register.
DB7	REQUEST FOR MASTER	RQM	Indicates Data Register is ready to send or receive data to or from the Process. Both bits DIO and RQM should be used to perform the handshaking function of "ready" and "direction" to the Processor.

TABLE 3. STATUS REGISTER 0 BITs

BIT			DESCRIPTION
NO	NAME	SYMBOL	
D7	INTERRUPT CODE	IC	D7 = 0 and D6 = 0, Normal termination of command was completed properly executed. D7 = 0 and D6 = 1, Abnormal termination of command (AT). Execution of command was started but was not successfully completed.
D6			D7 = 1 and D6 = 0. Invalid comand issue, (IC). Command which was issued was never started.
D5	SEEK END	SE	When FDC completes the SEEK comand, this flag is set to 1 (HIGH)
#D4	EQUIPMENT CHECK	EC	If the Track 0, signal fails to occur after 255 step pulses (Recalibrate command). Then this flag is set.
#D3	NOT READY	NR	Since drive ready is always persumed true. This will always be a LOGIC 0.
D2	HEAD SELECT	HS	This flag is used to indicate the state of HEAD at interrupt
D1	UNIT SELECT 1	US1	This flag is used to indicate a DRIVE UNIT Number at interrupt
D0	UNIT SELECT 0	US0	This flag is used to indicate a DRIVE UNIT Number at interrupt

TABLE 4. STATUS REGISTER 1 BITs

BIT			DESCRIPTION
NO	NAME	SYMBOL	
D7	END OF CYCLINDER	EN	When the FDC tries to access a sector beyond the final sector of a cylinder,this flag is set.
D6			Not used. This bit is always 0 (low)
D5	DATA ERROR	DE	When the FDC detects a * CRC error in either the ID field or a cylinder, this flag is set.
D4	OVERRUN	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D3	NOT DATA		Not used. This bit is always 0 (low)
D2	NO DATA	ND	During execution of READ DATA, WRITE DELETED DATA, or SCAN command, if the FDC cannot find the sector specified in the * * IDR Register, this flag is set. During execution of the READ ID command, if the FDC cannot read the ID field without an error, then this flag is set. During execution of the READ A TRACK command, if the starting sector cannot be found, then this flag is set.
D1	NOT WRITEABLE	NW	During execution of WRITE DATA, WRITE DELETED DATA or RORMAT A TRACK commands. If the FDC detects a WP signal from the FDC, then this flag is set.

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TABLE 4. STATUS REGISTER 1 BITs

BIT			DESCRIPTION
NO	NAME	SYMBOL	
D0	MISSING ADDRESS MARK	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time the MD (Missing Address Mark in data field) of Status Register 2 is set.

TABLE 5. STATUS REGISTER 2 BITs

BIT			DESCRIPTION
NO	NAME	SYMBOL	
D7			Not Used. This bit is always 0 (low)
D6	CONTROL MARK	CM	During executing of the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D5	DATA ERROR	DD	If the FDC detects a CRC error in the data field, then this flag is set.
D4	WRONG CYLINDER	WC	This bit is related to the ND bit, and when the contents of * * * C on the medium is different from that stored in the IDR, this flag is set.
D3	SCAN EQUAL	SH	During execution of the SCAN command, if the condition of "equal" is satisfied this flag is set.
D2	SCAN NOT	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D1	BAD CYLINDER	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR, and the contents of C is FF, then this flag is set.
D0	MISSING ADDRES MARK IN DATA FIELD	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted data Address Mark, then this flag is set.

TABLE 6. STATUS REGISTER 3 BITs

BIT			DESCRIPTION
NO	NAME	SYMBOL	
#D7			Not used. Will always be logic 0.
D6	$\overline{\text{WRITE}}$ $\overline{\text{PROTECTED}}$	$\overline{\text{WP}}$	This bit is used to indicate the status of the $\overline{\text{WRITE}}$ $\overline{\text{PROTECTED}}$ signal from the FDD
#D5	READY	RY	This bit will always be a logic 1. Drive is presumed to be ready.
D4	TRACK 0	TO	This bit is used to indicate the status of the Track 0 signal from the FDD.
#D3	$\overline{\text{WRITE}}$ $\overline{\text{PROTECTED}}$	$\overline{\text{WP}}$	This bit is used to indicate the status of the $\overline{\text{WRITE}}$ $\overline{\text{PROTECTED}}$ signal from the FDD
D2	HEAD SELECT	HS	This bit is used to indicate the status of the Side Select signal to the FDD
D1	UNIT SELECT 1 CYLINDER	US1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD
D0	UNIT SELECT 2	US0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD

Note : *   CRC - Cyclic Redundancy Check
     * *   IDR - internal Data Register
     * * *   C - Cylinder
     #   - Different from NEC765

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* DATA REGISTER

The eight-bit data Register stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command.

The relationship between the Master Status Register and the Data Register Status Register and the Data Register and the signals $\overline{RD}$, $\overline{WR}$, and A0 are shown in Table 7.

TABLE 7. MASTER STATUS AND DATA REGISTERS Relationships

A0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	ILLEGAL
0	0	0	ILLEGAL
1	0	0	ILLEGAL
1	0	1	READ from DATA REGISTER
1	1	0	WRITE into DATA REGISTER

* OPERATIONS REGISTER

The Operations Register provides support logic that latches the data bus upon receiving $\overline{LDOR}$ ad $\overline{WR}$. CS should not be active when this happens. The Operations Register replaces the typical latched port found

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in floppy subsystems used to control disk drive spindle motors and to select the desired disk drive. Table 8 represents the operations Register

TABLE 8. OPERATIONS REGISTER

OR0	DSEL	: Drive Select, if low and MOEN1 = 1, then $\overline{DS1}$ is active. If high and MOEN2 = 1, then $\overline{DS2}$ is active, but only in the PC AT mode
OR1	(X)	: In GM82C765B this mist be logic 0 for $\overline{DS1}$ and $\overline{DS2}$ to become active. No defined function in GM82C765B.
OR2	$\overline{SRST}$	: Soft reset, active low.
OR3	DMAEN	: DMA enable, active in Special and PC AT modes, Qualifies DMA and IRQ outputs and $\overline{DACK}$ input.
OR4	MOEN1	: Motor On enable, inverted output $\overline{MO1}$ is active only in PC AT
OR5	MOEN2	: Motor On enable, inverted output $\overline{MO2}$ is active in PC AT
OR6	(X)	: Has no defined function. A spare.
OR7	(MSEL)	: Mode Select, During a soft reset condition, may be used to select between Special mode (1) and PC AT mode (0).

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* BASE, SPECIAL, AND PC AT MODES

Base, Special, and PC AT modes allow subtle differences which the user may find desirable. The Control Register may be used in any mode without altering functionality.

* BASE MODE

After a hardware reset, RST active, the GM82C765B will be held on soft reset, $\overline{SRST}$ active, with the normally driven signals, DMA request and IRQ request outputs tristated. Base mode may be initiated at this time by a chip access by the host. Although this may be any read or write, it is strongly recommended that the Base mode user's first chip access be a read of the Master Status Register. Once Base mode is entered, the soft reset is released, and IRQ and DMA are driven. Base mode prohibits the use of the Operations Register, hence there can be no qualifying by DMAEN and no soft resets. The Drive Select outputs, $\overline{DS1}$ to $\overline{DS4}$, offer a 1 of 4 decoding of the Unit Select bits resident in the command structure.
Pin $\overline{RWC}$ represents Reduce Write Current and is indicative of when write precompensation is necessary.

* SPECIAL MODE

Special mode allows use of the Operations Register for the DMAEN signal as a qualifier and to do a software driven device reset, $\overline{SRST}$. To enter Special mode, the Operations Register is loaded with (1X00X0XX), setting mode Select to a logic 1 disabling MOEN1 and MOEN2 and causing $\overline{SRST}$ to be active. Then a read of the Control Register address, $\overline{LDCR}$ and $\overline{RD}$, will set the device into Special mode. The $\overline{DS1}$ through $\overline{DS4}$ is again offered in this mode, as is $\overline{RWC}$.

* PC AT Mode

For PC AT compatibility, users will write to the Operations Register, $\overline{LDOR}$ and $\overline{WR}$; this action, performed after a hardware reset, or in the Base mode, initiates PC AT mode. PC

AT mode can also be entered from Special mode by loading the Operations Mode Select to a logic 0, disabling MOEN1 and MOEN2, and causing $\overline{SRST}$ to be active. Then a read of the Control Register address sets the device into PC AT mode. The $\overline{DS}$ outputs are now replaced with the DSEL and MOEN signals buffered from the Operations Register. DMAEN and $\overline{SRST}$ are supported and compatible with the current BIOS. $\overline{RWC}$ pinfunction is now $\overline{RPM}$ so that users with two speed drives may reduce spindle speed per minute to 300 revolutions per minute when active low, used to reduce write current when a slower data rate is selected for a given drive. Figure 3 illustrates the relationship among the three modes.
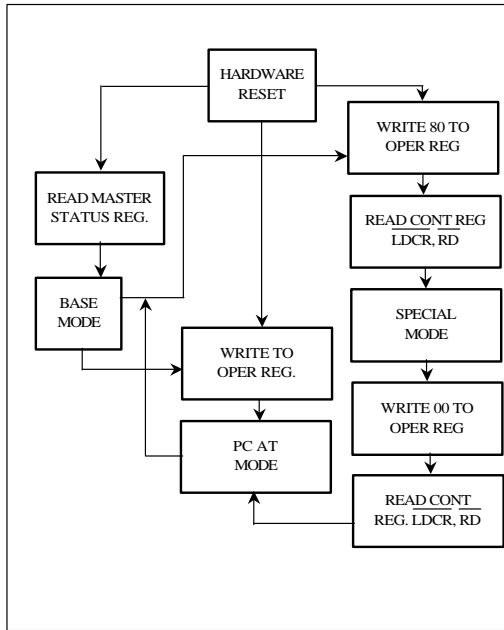
Fig. 3 Flow Diagram Depicting Relationship of Base, Special, and PC AT modes.

After any reset the GM82C765B, (a hard RST or soft $\overline{SRST}$, will automatically go into a Polling routine. In between commands (and between step pulse in the SEEK Command), the GM82C765B polls all four FDDs looking for a change in the ready line from any of the drives. Since the drive is always presumed ready, an interrupt will only be generated following a reset. This occurs because a reset forces Not ready status, which then promptly becomes ready.

Note that in special or PC AT mode if DMAEN is not valid prior to 1mS after reset goes inactive, then IRQ may be already set and pending when finally enabled onto the bus. The polling of the ready line by the GM82C765B occurs continuously between commands. Each drive is polled every 1,024mS, except during the READ/WRITE commands. For minifloppies, the polling rate is 2,048mS. The drive polling sequence is 1-2-4-3. Please note that in the PC AT mode, the user will not see the polling at the Drive Select signals, figure 4 illustrates the Drive Select Polling time

● POLLING ROUTINE
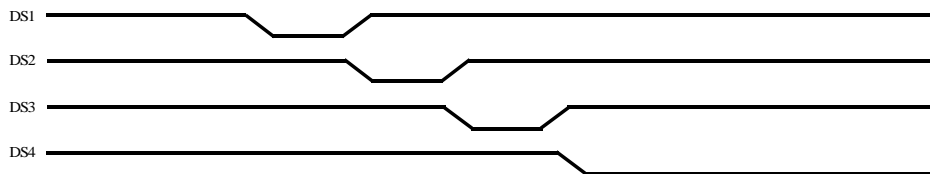
Fig. 4. Drive select polling timing

* DEVECE RESETS

The GM82C765B supports both hardware reset (RST) pin (19) and a software reset ($\overline{SRST}$) through use of the Operations Register. The RST pin will cause a device reset for the active duration. RST causes a default to Base mode, and default selects 250k MFM (or 125k FM, code dependent) as the data rate (16 MHz input clock). $\overline{SRST}$ will reset the microcontroller as did the RST, but will not affect the value set for the internal timers-HUT, FTL, and SRT.

If the XTAL oscillators are used, instead of the TTL driven clock inputs, the hardware RST active time requirement will bootstrap the circuit into guaranteed oscillation in a fixed amount of time.

The extended reset time allows the growth of the oscillation to produce stable internal clock timing

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[*] **DATA SEPARATOR**

The Data Separator is a Digital Phase Lock
Loop Floppy Disk Data Separator (DPLL). It was
designed to address high performance error rates on
floppy disk drives, and to provide superior
performance in terms of available bit jitter tolerance. It
contains the necessary logic to achieve classical 2nd
order, type 2, phase locked loop performance. DPLL is
used as the Data Separator in the GM82C765B system.
Figure 5 illustrates the DPLL implified block diagram.
The bit jitter tolerance for the data separator is 60%,
Which guarantees an error rate of   < 10E-9.

[*] **WRITE PRECOMPENSATION**

The BM82C765B maintains the stand first level
algorithm to determine when write precompensation
should be applied.
The EARLY and LATE signals are used internally to

select the appropriate delay in the write data pulse
stream.
  The encoded WRITE DATA signal is synchronized to
the 16 MHz clock if this is the frequency on CLK1 pin
(23), and clocked through a shift register before a
multiplexer gates the chosen bit to the output.
  The output data pulse width has a 25% duty cycle,
i.e., one fourth of the bit cell period, and equal to one
half the WCLK period.
  When PCVAL pin (24) = 1, all data will be
precompensated by + 187nS precompensation will be
generated. For frequencies other than 16 MHz on the
CLK1 pin, the precompensation values will be two and
three clock cycles respectively.
When the non-standard data rate using CLK2 is chosen,
the MFM precompensation will always be two clock
cycles.
For 9.6MHz, this is +208nS. In this case, this PCVAL
function is disabled
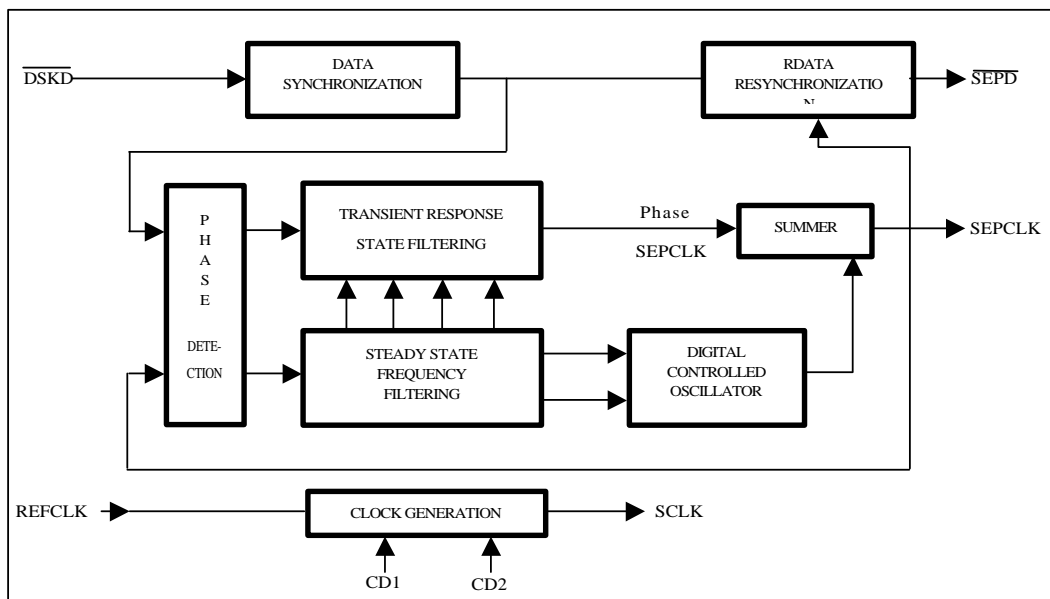
Fig. 5. DPLL Simplified BLOCK DIAGRAM

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* CLOCK GENERATION

This logical block provides all the clocks needed by the GM82C765B. They are: Sampling clock (SCLK), Write clock (WCLK), and the MASTER CLOCK (MCLK). SCLK drives the DPLL Data Separator used during data recovery. This Clocks's frequency is always 32 times the selected data rate. WCLK is used by the encoder logic to place MFM or FM on the serial WD-stream to the disk. WCLK always has a frequency two times the selected data rate. MCLK is used by the microsequencer. MCLK and MCLK clock all latches in a two-phase scheme.

One microinstruction cycle is four MCLK cycles. MCLK has a frequency times the FM data rate.

Table 9 presents the Clock Data Rate. Figure 6 illustrates the XTAL oscillator circuits for the 44-pin PLCC configuration.

TABLE 9. CLOCK DATA RATE

DATARATE	CODE	SLCK	MCLK	WCLK
500Kbit/S	MFM	16.0MHz	4.0MHz	1.0MHz
250Kbit/S	FM	8.0MHz	4.0MHz	500.0MHz
250Kbit/S	MFM	8.0MHz	2.0MHz	500.0MHz
125Kbit/S	FM	4.0MHz	2.0MHz	250.0MHz
300Kbit/S	MFM	9.6MHz	2.4MHz	600.0MHz
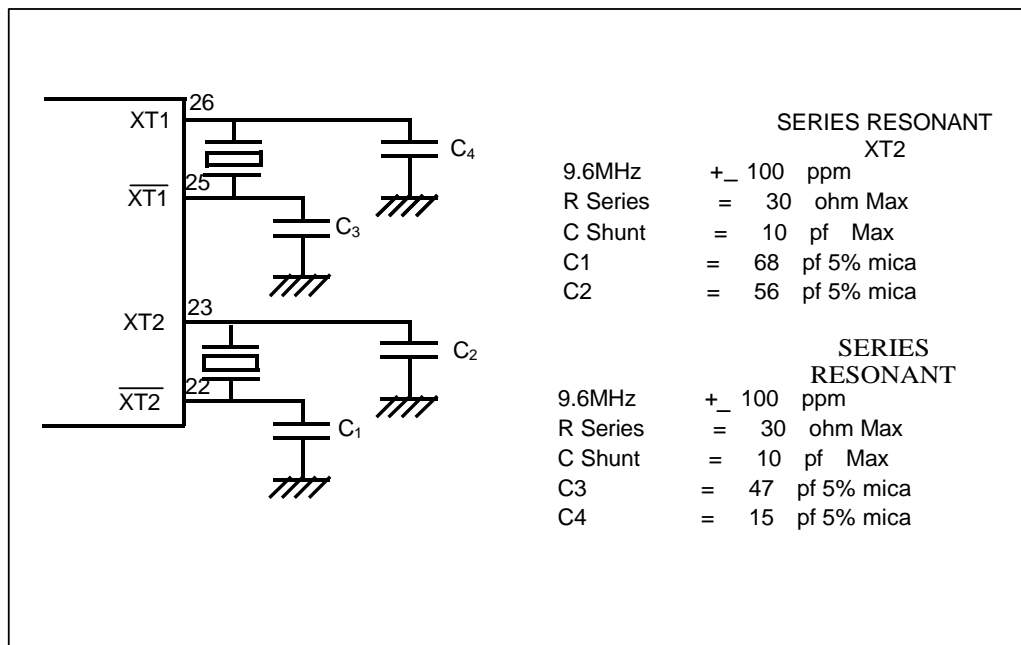
Fig 6. XTAL Oscillator circuits for the 44 pin PLCC

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* COMMAND PARAMETERS

The GM82C765B is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The results after execution of the command may also be a multibyte transfer back to the processor. The commands consist of three phases : Command phase, Execution phase, and the Result phase.

Command phase − The Floppy Disk Controller (FDC) receives all information required to perform a particular operation from the processor.

Execution phase − The FDC performs the operation it was in structed to do.

Result phase − After completion of the operation, status and other housekeeping in formation are made available to the processor

TABLE 10. GM82C765B COMMANDS

READ DATA
READ DELETED DATA
WRITE DATA
WRITE DELETED DATA
READ A TRACK
READ ID
FORMAT A TRACK
SCAN EQUAL
SCAN LOW OR EQUAL
SCAN HIGH OR EQUAL

Table 10. lists the 15 GM82C765B commands.
Table 11. through 25 are presented to show the required parameters and results for each command. Most commands require nine command bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written. An "R" indicates a result byte.

TABLE 11. READ DATA

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W W	MT X	MF X	SK X	0 X		0 X	1 HS	1 US1	0 US0	Command Codes
	W W W W W W W					←— C —→ ←— H —→ ←— R —→ ←— N —→ ←— EOT —→ ←— GPL —→ ←— DTL —→					Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
EXECUTION											Data transfer between FDD and main system
RESULTS	R R R R R R R					←— STO —→ ←— ST1 —→ ←— ST2 —→ ←— C —→ ←— H —→ ←— R —→ ←— N —→					Status information after command execution. Sector ID information after command execution.

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TABLE 12. READ DELETED DATA

	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W W	MT X	MF X	SK X	0 X		1 X	1 HS	0 US1	0 US0	Command Codes
	W W W W W W W				←——— C ———→ ←——— H ———→ ←——— R ———→ ←——— N ———→ ←——— EOT ———→ ←——— GPL ———→ ←——— DTL ———→						Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
EXECUTION											Data transfer between FDD and main system
RESULTS	R R R R R R R				←——— ST0 ———→ ←——— ST1 ———→ ←——— ST2 ———→ ←——— C ———→ ←——— H ———→ ←——— R ———→ ←——— N ———→						Status information after command execution. Sector ID information after command execution.

TABLE 13. WRITE DATA

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W W	MT X	MF X	0 X	0 X		0 X	1 HS	0 US1	1 US0	Command Codes
	W W W W W W W				←——— C ———→ ←——— H ———→ ←——— R ———→ ←——— N ———→ ←——— EOT ———→ ←——— GPL ———→ ←——— DTL ———→						Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
EXECUTION											Data transfer between FDD and main system
RESULTS	R R R R R R R				←——— ST0 ———→ ←——— ST1 ———→ ←——— ST2 ———→ ←——— C ———→ ←——— H ———→ ←——— R ———→ ←——— N ———→						Status information after command execution. Sector ID information after command execution.

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TABLE 14. WRITE DELETED DATA

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W W	MT X	MF X	0 X	0 X		1 X	0 HS	0 US1	1 US0	Command Codes
	W					C					Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W					H					
	W					R					
	W					N					
	W					EOT					
	W					GPL					
	W					DTL					
EXECUTION											Data transfer between FDD and main system
RESULTS	R					STO					Status information after command execution.
	R					ST1					
	R					ST2					
	R					C					Sector ID information after command execution.
	R					H					
	R					R					
	R					N					

TABLE 15. READ A TRACK

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W W	0 X	MF X	SK X	0 X		0 X	0 HS	1 US1	0 US0	Command Codes
	W					C					Sector ID information prior to command execution.
	W					H					
	W					R					
	W					N					
	W					EOT					
	W					GPL					
	W					DTL					
EXECUTION											Data transfer between FDD and main system. FDD reads all data fields from index hole to EOT
RESULTS	R					STO					Status information after command execution.
	R					ST1					
	R					ST2					
	R					C					Sector ID information after command execution.
	R					H					
	R					R					
	R					N					

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TABLE 16. READ ID

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W W	0 X	MF X	0 X	0 X		1 X	0 HS	1 US1	0 US0	Command Codes
EXECUTION											The first correct ID information on the cylinder is stored in Data Register.
RESULTS	R R R R R R R				◄— STO —► ◄— ST1 —► ◄— ST2 —► ◄— C —► ◄— H —► ◄— R —► ◄— N —►						Status information after command execution. Sector ID information after command execution.

TABLE 17. FORMAT A TRACK

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W W W W W W	0 X ◄— ◄— ◄— ◄—	MF X	0 X	0 X N —► SC —► GPL —► D —►		1 X	1 HS	0 US1	1 US0	Command Codes Bytes / Sector Sector/Track Gap 3 Filler Byte
EXECUTION											Floppy Disk Controller (FDC) formats an entire track.
RESULTS	R R R R R R R				◄— STO —► ◄— ST1 —► ◄— ST2 —► ◄— C —► ◄— H —► ◄— R —► ◄— N —►						Status information after command execution. In this case, ID information has no meaning.

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TABLE 18. SCAN EQUAL

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W	MT	MF	SK	1		0	0	0	1	Command Codes
	W	X	X	X	X		X	HS	US1	US0	
	W	←				C				→	Sector ID information prior to command execution.
	W	←				H				→	
	W	←				R				→	
	W	←				N				→	
	W	←				EOT				→	
	W	←				GPL				→	
	W	←				STP				→	
EXECUTION											Data transfer between FDD and main system
RESULTS	R	←				STO				→	Status information after command execution.
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	Sector ID information after command execution.
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

TABLE 19. SCAN LOW OR EQUAL

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W	MT	MF	SK	1		1	0	0	1	Command Codes
	W	X	X	X	X		X	HS	US1	US0	
	W	←				C				→	Sector ID information prior to ommand execution.
	W	←				H				→	
	W	←				R				→	
	W	←				N				→	
	W	←				EOT				→	
	W	←				GPL				→	
	W	←				STP				→	
EXECUTION											Data transfer between FDD and main system
RESULTS	R	←				STO				→	Status information after command execution.
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	Sector ID information after command execution.
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

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TABLE 20. SCAN HIGH OR EQUAL

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W W	MT X	MF X	SK X	1 X		1 X	1 HS	0 US1	1 US0	Command Codes
	W					←——— C ———→					Sector ID information prior to command execution.
	W					←——— H ———→					
	W					←——— R ———→					
	W					←——— N ———→					
	W					←——— EOT ———→					
	W					←——— GPL ———→					
	W					←——— STP ———→					
EXECUTION											Data transfer between FDD and main system
RESULTS	R					←——— STO ———→					Status information after command execution.
	R					←——— ST1 ———→					
	R					←——— ST2 ———→					
	R					←——— C ———→					Sector ID information after command execution.
	R					←——— H ———→					
	R					←——— R ———→					
	R					←——— N ———→					

TABLE 21. RECALIBARTE *

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W W	0 X	0 X	0 X	0 X		0 X	1 HS	1 US1	1 US0	Command Codes
EXECUTION											Head retracted to Track zero

TABLE 22. SENSE INTRRUPT STATUS

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W	0	0	0	0		0	1	1	1	Command Codes
RESULTS	R										Status information about the FDC at the end of seak operation

TABLE 23. SPECIFY

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W W	0 SRT	0	0	0 HLT		0	0 HUT	1	1 ND	Command Codes
EXECUTION											Head retracted to Track zero

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TABLE 24. SENSE DRIVE STATUS

PHASE	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W W	0 X	0 X	0 X	0 X		0 X	0 HS	0 US1	0 US0	Command Codes
EXECUTION	ST3										Status information about the FDC

TABLE 25. SEEK

	R/W	D7	D6	D5	D4		D3	D2	D2	D0	REMARKS
COMMAND	W W W	0 X	0 X	0 X	0 X		1 X NCN	1 HS	1 US1	1 US0	Command Codes
EXECUTION											Head is positioned over proper cylinder on the diskette.

Table 26 defines, in alphabetical order, the symbols used in Command Tables 11 through 25.

TABLE 26. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
A0	ADDRESS LINE 0	A0 Controls selection of Main Status Register (A0 = 0) or Data Register (A0 =1)
C	CYLINDER NUMBER	C stands for the current/selected cylinder (track) numbers 0 through 255 of the medium.
D	DATA	D stands for the data pattern which is going to be written into a sector.
D7-D0	DATA BUS	8-bit DATA BUS, where D7 stands for a most significant bit, and D) stands for a least significant bit.
DTL	DATA LENGTH	When N is defined as 00, DTL stands for the DATA LENGTH which users are going to read out or write into the sector.
EOF	END OF TRACK	EOT stands for the final sector number on a cylinder. During read or Write operations. FDC will stop data transfer after a sector number equal to EOT.
GPL	GAP LENGTH	GPL stands for the length of Gap 3. During the FORMAT Command. It determines the size of Gap 3.
H HLT HS	HEAD ADDRESS HEAD LOAD TIME HEAD SELECT	H stands for head number 0 or 1, as specified in the ID field. HLT stands for the HEAD LOAD TIME in FDD (2 to 254ms in 2ms increments) HS stands for a selected head number 0 or 1 and controls the polarity of pin 25 (in 40 pin DIP) or pin 28 (in 44 pin PLCC)
HUT	HEAD UNLOAD TIME	HUT stands for the HEAD UNLOAD TIME after a Read or Write operation has occurred (16 to 240ms in 16ms increments).
MF	FM or MFM	If MF is low, FM mode is selected. If it is high, MFM mode is selected.
MT	MULTITRACK	If MT is high, a MULTITRACK operation is performed. If MT =1 after finishing Read / Write operation on side 0, FDC will automatically start searching for sector 1 on side 1

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SYMBOL	NAME	DESCRIPTION
N	NUMBER	N stands for the NUMBER of data bytes written in a sector.
NCN	NEWCYLINDER NUMBER	NCN stands for a NEW CYLINDER NUMBER which is going to be reached as a result of the Seek operation. Desired position of head.
ND	NON-DMA MODE	ND stands for operation in the NON-DMA MODE.
PCN	PRESENT CYLINDER	PCN stands for the cylinder number at the completion of the SENSE INTERRUPT STATUS Command position of head at present time..
R	RECORD	R stands for the sector number which will be read or written.
R/W	READ/WRITE	R/W stands for either READ or WRITE signal.
SC	SECTOR	SC indicates the number of sectors per cylinder.
SK	SKIP	SK stands for SKIP Deleted Data Address mark.
SRT	STEP RATE TIME	STR stands for the Stepping Rate for the FDD (1 to 16ms in 1ms increments). Stepping Rate applies to all drives. In 2's complement format, F(Hes) = 1ms, E(Hex) =2ms, etc
ST0 ST1 ST2 ST3	STATUS 0 STATUS 1 STATUS 2 STATUS 3	STO = 3 stands for one of four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main Status Register (selected by A0 = 0). ST0=3 may be read only after 3 command has been executed and contains information relevant to that particular command.
STP		During a SCAN operation, if STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP=2, then alternate sectors are read and compared.
US0, US1	UNIT SELECT	US stands for a selected drive; binary encoded, 1 of 4.

COMMAND DESCRIPTIONS

Read Data

A set of nine byte words are required to place the FDC into the Read Data Mode.

After the Read Data command has been issued, the FDC loads the head (if it is unloaded state), warts the specified head setting time (defined in the Specify Command begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data bit) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector number is incremented by one, and the data from the next sector is read and output on the data bus.

This continuous read function is called a "Multi-sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal.

TC should be issued at the same time that the $\overline{\text{DACK}}$ for the last byte of data is sent.

Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sectors, check CRC (Cyclic Redundancy Count) bytes, and the end of the sector terminate the read data command.

The amount of data which can be handled with a single command to the FEC depends upon MT (multi-track), MF(MFM/FM), and N(number of bytes/sector). Table 27 lists the transfer Capacity. The "Multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and

completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N=0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the

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data beyond DTL in the sector is not sent to the Data Bus. The FDC reads (internally) the complete sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexadecimal.

TABLE 27. TRANSFER CAPACITY

Multi-track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Number of Sectors)	Final Sector Read from Diskettes
0 0	0 1	00 01	(128) (26) – 3.328 (256) (26) – 6.656	26 at Side 0 or 26 at Side 1
1 1	0 1	00 01	(128) (52) – 6.658 (256) (52) –13.312	26 at Side1
0 0	0 1	01 02	(256) (15) – 3.840 (512) (15) – 7.680	15 at Side 0 or 15 at Side 1
1 1	0 1	01 02	(256) (30) – 7.680 (512) (30) – 15,360	15 at Side 1
0 0	0 1	02 03	(512) (8) – 4.096 (1024) (8) – 8.192	8 at Side 0 or 8 at Side 1
1 1	0 1	02 03	(512) (16) – 8.192 (1024) (16) – 16.384	8 at Side 1

At the completion of the Real data Command, the head is not unloaded until after head unload time interval (specified in the specify Command) has elapsed. If the processor issues another command before the head unloads, then the head setting time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the index Hole twice without finding the right sector, (indicated in 'R'), then the FDC sets the ND (No Data) flag in status Register 1to a 1 (high), and terminates the Read Data command (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes If a read error is detected (incorrect CRC in ID field), the FDC sets the DE(Data Error) flag in Status Register 1 to 1 (High) If a CRC error occurs in the data field, the FDC also sets the DD(Data Error in Data Field) flag in Status Register 2 to 1(High) and terminates the Read data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark

off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK =0), then the FDC sets the CM(control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data command, after reading all the data in the sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk Data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 us in the FM mode, land every 13 us in the MFM mode, or the FDC sets the OR (Overrun) flag in status Register. 1 to a 1 (high), and terminates the Read Data command.

TABLE 28. C, H, R, and VALUES

MT	HD	Final Sector Transferred to processor	ID information at Result Phase			
			C	H	R	N
0	0	Less then EOT	NC	NC	R+1	NC
	0	Equal to EOT	C+ 1	NC	R=01	NC
	1	Less then EOT	NC	NC	R+1	NC
	1	Equal to EOT	C+1	NC	R=01	NC
1	0	Less then EOT	NC	NC	R+1	NC
	0	Equal to EOT	NC	LSB	R=01	NC
	1	Less then EOT	NC	NC	R+1	NC
	1	Equal to EOT	C+1	LSB	R=01	NC

Notes : NC (No Change) : The same value the one at the beginning of command execution. LSB (Least Significant Bit): The Least significant bit of H is complemented.

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Write Data

A set of nine bytes is required to set the into DC the Write Data mode, after the commawrite data and has been issued the FDC loads the head (if is in the unloaded state), waits the specified head settling time (defined in the specify command), and beings reading ID fields, when all four bytes loaded during the command (C,H,R,N) match the four byte of ID field from the processor byte-by-byte via the data bus and outputs it to the FDD. After writing data into the current sector, the sector number stored in 'Rr' is incremented by one, and the next data field is written into. The FDC continues this multisector Write Operation' until the issuance of Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written remainder of the data field is filled zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets the DE (DATA Error) flag of Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same., and one should refer to the Read data command for details.

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to following items are the same, and one the Read Data command for details:

- Transfer capacity
- EN (End of Cylinder) flag
- ND (No Data) flag
- Head Unload Time interval
- ID information When the processor terminates command
- Definition of DTL when N=0 and when N=0
   In the Write Data mode, data transfers between the processor and FDC via the data bus, must occur every 27 uS in the FM mode and every 13 us in the MFM mode. If the time interval between data transfers is longer than this, then the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high) and terminal the Write Data Address mark.

Write Deleted Data

This command is the same as the Write Data command except a Deleted Data Address mark is written at the beginning of the data field instead of the normal Data Address mark.

Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field (and SK = 0 (low)), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skps the sector with the Data Address mark and reads the next sector.

Read A Track

This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately of the sectors is read. Immediately after sensing the index hole. The FDC starts reading all data fields on the track as continuous biocks of data.

If the FDC finds an error in the ID or Data CRC check bytes, it continues to. This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address mark on the diskette after it senses index hole for the second time, it sets the MA (Missing Address mark) flag in Status Register 1 to a 1 (high) and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

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READ ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, then the MA (Missing Address mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1to a 1 to a 1 (high). The command is then terminated with bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format A Track

The format command allows an entire track to be formatted. After the index hold is detected, data is written on the diskette; Gaps , Address marks, ID fields and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format are recorded. The particular format which will be written is controlled by the values Programed into N (number of bytes/sector), SC (secros/cylinder), GPL (gap length), and D (data pattern) which are supplied by the processor during the Command phase. The data field for each sector is supplied by the processor; that is four data requests per sector are made by the FDC for C (cylinder number). H (Head number), R (sector number) and N (number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processors must send new values for C, H, R, and N to the WD37C65/A/B for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA interrupts per sector and the processor must supply C,H,R, and N loads for each sector. The contents of the R register are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the FDC deters the index hole

for the second time, where upon it terminates the command. Table 29 shows the relationship between N, SC, and GPL for various sector sizes

TABLE 29. N, SC AND GPL RELATIONSHIP

Format	Sector Size	N	SC	GPL'	GPL"
	8" Standard Floppy				
FM Mode	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode [4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	30	08	35	74
	4096	05	02	C3	FF
	8192	06	01	C3	FF
	5 1/4 " Minifloppy				
FM Mode	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode [4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	04	C8	FF
	4096	05	01	C8	FF
	3 1/2 "Sony Microfloppy				
FM Mode	128	0	0F	07	1B
	258	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode [4]	256	1	0F	1B	54
	512	2	09	1B	54
	1024	3	05	35	74

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Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of D FDD=D Processor, D FDD<D Processor, or D FDD>D Processor. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF-largest number, 00=smallest number). After a whole sector of data is compared, if the conditions art not met, the sector number is incremented (R+STP−R), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), on the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high) and terminates the Scan command. The receipt of a Terminal Count signal from the processor or DMA controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 30 shows the status of bits SH and SN under various conditions of Scan.

If the FDC encounters a Deleted Data Address mark on one of the sectors (and K=0), then it regards the sector as the last sector on the cylinder, sets the CM (Control mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK=1, the FDC skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK=1), the FDC sets the CM (Control mark) flag of Status Register 2 to a 1 (high) in order to show that a delected sector had been encountered.

TABLE 30. STATUS of BITS SH AND SN

Command	Status Register 2		Comments
	Bit 2-SN	Bit 3-SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} = D_{Processor}$
Scan low Or Equal	0	0	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	1	0	$D_{FDD} < D_{Processor}$

When either the STP (contiguous sectors=01,or alternate sectors=02) sectors are read or the MT (Multitrack) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP=02, MT=0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following will happen: sectors 21,23 and 25will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the OR (Overrun) flag set in Status Register 1, it is necessary to have the data available in less then 27 us (FM mode) or 13 us (MFM mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

SEEK

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The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent Present Cylinder Registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference, performs the following operations:

PCN<NCN: Direction signal to FDD set to a 1 (high), and step pulses are issued. (Step In)

PCN>NCN: Direction signal to FDD set to a 0 (low), and step pulses are issued. (Step Out)

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued NCN is compared against PCN, and NCN=PCN, the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits BOB-D3B in the Main status Register are set during the seek operation and are cleared by the sense interrupt status command.

During the command phase of the Seek operation the FDC is in the FDC busy state: but during the Execution phase, it is in the non-busy state, another Seek command may be issued, and in this manner parallel Seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process sending step pulses to any drive

If the time to write three bytes of Seek command exceeds 150 uS, the timing between the first two step pulses may be shorter than set in the Specify command by as much as 1ms.

RECALIBRATE

The function of this command is to retract the Read/Write head within the FDD to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0

signal is low, the Direction signal remains 0 (Low) and step pulses are issued. When the Track 0 signal goes high, the SE (Seek End) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 step pulses have been issued for the GM82C765B,the FDC sets the SE (Seek End) and EC (Equipment Check) flag of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively. The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also applies to the Recalibrate command.

Sense Interrupt Status

An interrupt signal is generated by the FDC for one of the following reasons.
1. Upon entering the Result phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Cylinder command
   g. Write Deleted Data command
   h. Scan commands
2. Ready line of FDD changes state
3. End of Seek or Recalibrate command
4. During Executing phase in the non-DMA mode

Interrupts caused by reasons 1and 4 above occur during normal command operations and are easily discernible by the processor. During and Executing phase in non-DMA mode. DB5 in the Main Status Register is high. Upon entering the Result phase, this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused +y reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued, resets the Interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

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TABLE 31. INTERRUPT CAUSE

Seek End Interrupt Code			Cause
Bit 5	Bit 6	Bit 7	Ready Line dhanged state, either polarity
0	1	1	Normal Termination of Seek or Recalibrate command
1	0	0	Abnormal Termination of Seek or Recalibrate command
1	1	0	Abnormal Termination of Seek or Recalibrate command

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no Result phase. When the disk drive has reached the desired head position, the GM82C765B will set the Interrupt line true. The host CPU must then issue a Sense interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives.

The Specify command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240mS in increments of 16mS (01 = 16mS, 02 = 32mS … OF16 = 240mS). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16mS in increments of 1ms (F = 1ms, E = 2ms, D = 3ms, etc.). The HLT (Head load Time)defines the time between when the Head Load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254ms in increments of 2ms (01 = 2ms, 02 = 4ms, 03 = 6ms …7F = 254ms). (01 = 2ms. 02 = 4ms, 03 = 6ms ..7F = 254ms).
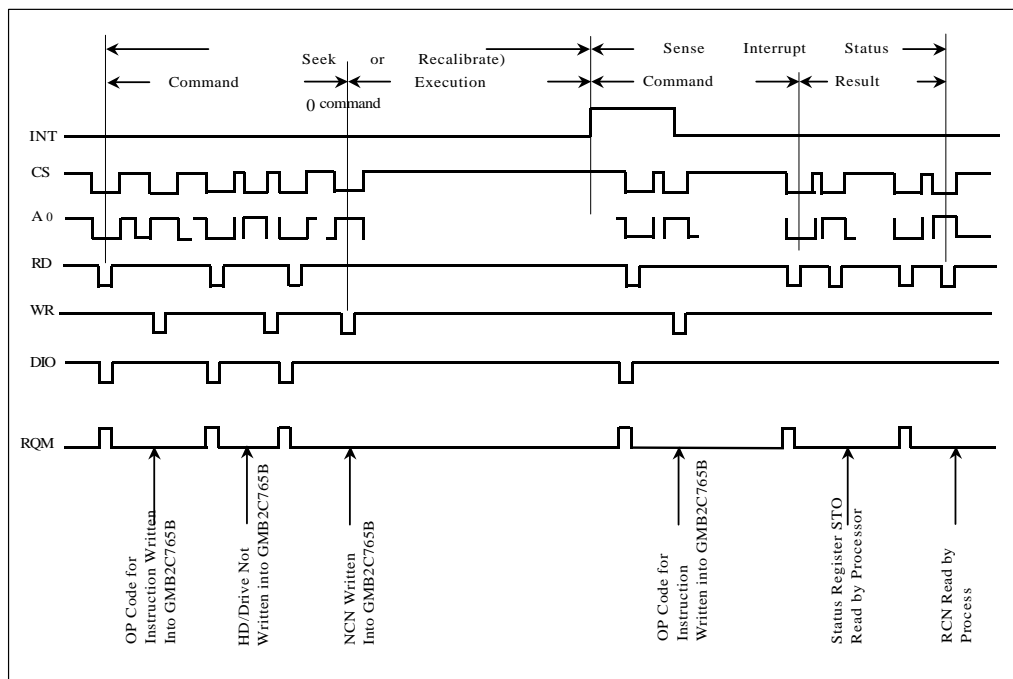

Fig. 7. Recalibrate and Sense Interrupt Relationship

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The Specify command sets the initial values for each of the three internal timers. The HUT(Head Unload Time) defines the time from the end of the Execution phase of one of the Read Write commands to the head unload state This timer is programmable from 16 to 24Oms in increments of 16ms.(01=16ms, 02=32ms …OF16=240ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16ms in increments of 1ms (F=1ms, E=2ms, D=3ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254ms in increments of 2ms (01=2ms, 02=4ms, 03=6ms .7F=254ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 23). Times indicated above are for a 16MHz clock; if the clock was reduced to 8MHz, then all time intervals are increased by a factor of 2.

Sense Drive Satus

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in DFC registers.

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the GM82C765B is in the Result phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0, it will find an 80 hex, indicating an Invalid command was received. A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt; otherwise the FDC will consider the next command to be an invalid command.

GAP4a 40x FF	SYNC 6X 00	IAM FC	GAP1 26x FF	SYNC 6x 00	IDAM FE	C Y L	H D	S E C	N O	C R C	GAP 11x FF	SYNC 6x 00	DATA AM FB OR F8	DATA1	C R C	GAP3	GAP4b

Index Repeat N Times

Fig 8. GM82C765B FM mode Format

GAP4a 80x FF	SYNC 12x 00	IAM		GAP1 50x 4E	SYNC 12x 00	IDAM		C Y L	H D	S E C	N O	C R C	GAP2 22x 00	SYNC 12x 00	DATA AM	DATA 1	C R C	GAP3 1	GAP4b
		3x C2	FC			3x A1	FE								3x FB A1 F8				

Index Repeat N Times

Fig 9. Gm82c765B MFM mode Format