1. Features

- IEEE 802.3/u 10Base-T/100Base-TX compatible
- Ethernet Switch Ports:
  - Two 10/100Mbps PHY
  - One MII/RMII interface with Reversed - MII support
- Supports auto crossover function - HP Auto-MDIX
- Flow Control
  - Supports IEEE 802.3x Flow Control in Full-duplex mode
  - Supports Back Pressure Flow Control in Half-duplex mode
- Per port support bandwidth, ingress and egress rate control
- Per port support priority queues
  - Each port with four queues
  - Port-based, 802.1P VLAN, or IP TOS priority
- Support 802.1Q VLAN for up-to 16 VLAN groups
- Support VLAN ID tag/untag options
- Support special Tag, double tag header
- Supports up-to 1K Uni-cast MAC addresses
- Supports store and forward switching approach
- Supports Broadcast Storming filter function
- Supports Serial Data Management Interface
- Automatic aging scheme
- Snooping Hardware Support
  - IGMP v1
  - IGMP v2
  - MLD v1
- Support STP/RSTP
- Support LFP (Link Fault Pass-through)
- Support MIB counters for diagnostic
- EEPROM interface for power up configurations
- EEPROM 93C46 or 93C56 auto detection
- Package
  - 64-pin LQFP
  - 56-pin QFN
- Power
  - 3.3V single voltage support,

    1.8V internal core
  - Compatible with 3.3V and 5.0V tolerant I/Os

2. General Description

The DM8603 is Davicom's new fully integrated, high performance, and cost-effective three port 10M/100Mbps Fast Ethernet Controller. As a fast Ethernet switch, the DM8603 consists of two PHY ports and a port with either MII or RMII interface. As the DM8603 was designed with our customers' requirements in mind, the switch has built-in versatility and is specifically designed for various data, voice, and video applications needs.

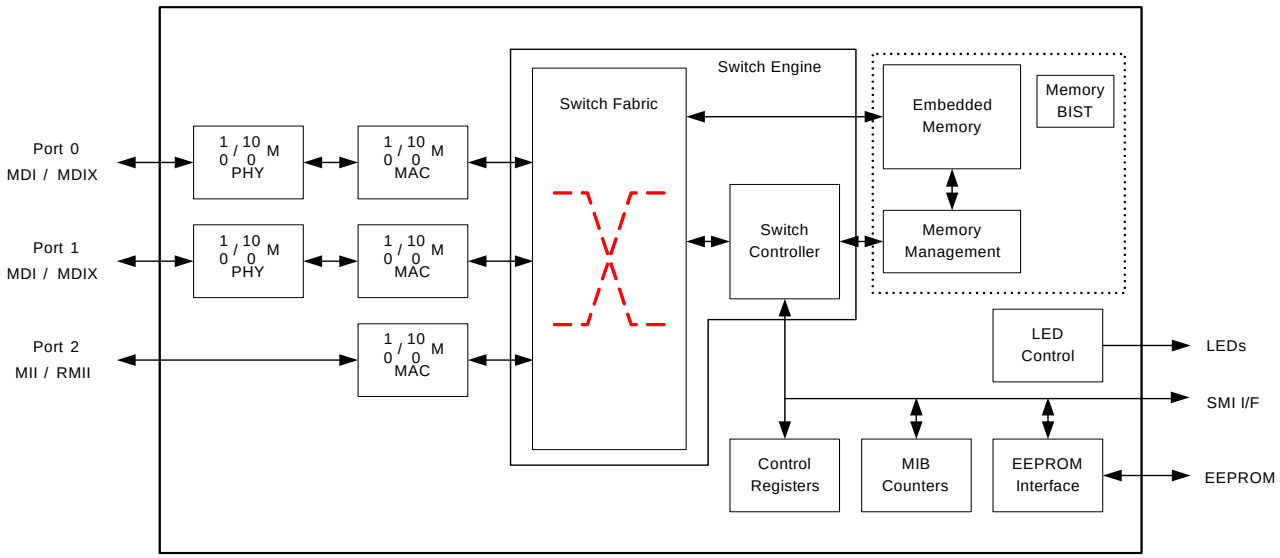
The two PHY ports on the DM8603 are IEEE 802.3/u standards compliant. Aside for the first two PHY ports and in an effort for maximum application flexibility, the other port on the DM8603 offer the options to either connect with an Ethernet PHY, reversed MII, or RMII. The reversed MII configuration is used to connect with SoC's with a MII interface. The RMII interface is the alternative interface configuration in case of the need to connect a lower pin count Ethernet PHY or SoC.

To maximize the performance of each port, the DM8603 was designed with many features in mind. For proper bandwidth, each port also supports ingress and/or egress rate control. In support of efficient packet forwarding, the DM8603 has port-based VLAN with tag/un-tag functions for up to 16 groups of 802.1Q. Each

port includes MIB counters, port security, loop-back capability, IGMP snooping, and the build in memory self test (BIST) for system and board level diagnostic.

In designing for the requirements of various data, voice, and video applications, enough internal memory has been provided for usage of the DM8603's three ports, and the internal memory supports an up to 1K uni-cast MAC address table. Then to meet the demands of various bandwidth and latency issues in data, voice, and video applications, each port of the DM8603 has four priority transmit queues. These queues can be defined either through port-based operation, 802.1p VLAN, or the IP packet TOS field automatically.

4. Block Diagram



5. Application

IPTV, VoIP CPE (ATA, IP Phone, Video Phone), IP STB, IPC, POS, Internet Radio

6. Order Information

Part Number	Pin Count	Package
DM8603EP	64	LQFP
DM8603NP	56	QFN

DAVICOM Semiconductor, Inc.
No.6, Li-Hsin Rd.VI, Science Park, Hsin-Chu, Taiwan, R.O.C.
TEL: 886-3-5798797
FAX: 886-3-5646929
E-mail: sales@davicom.com.tw