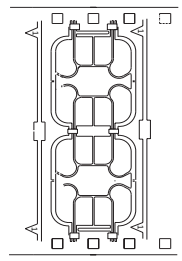
ST1305B

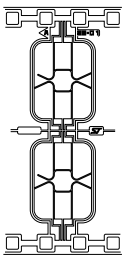
Memory Card IC 192 bit High Endurance EEPROM With Secure Logic Access Control

DATA BRIEFING

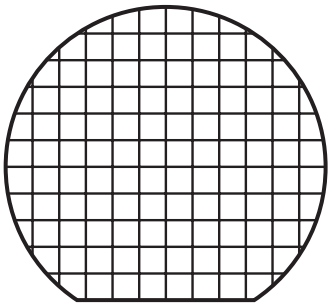
- Single Supply Voltage (5 V)
- Memory Divided Into:
  - 16 bits of Circuit Identification
  - 48 bits of Card Identification
  - 48 bits of Count Data
  - 16 bits of Certificate
  - 24 bits of Transport Code
  - 64 bits of Issuer Data
- Counting Capability up to 262,144
- Circuit Protected by Transport Code for Delivery from ST to the Customer
- 5 External Contacts Only (ISO 7816 Compatible)
- Answer to Reset (Fully Compatible with ISO 7816-3)
- E.S.D. Protection Greater Than 4000 V
- Power-On and Low V_{CC} Reset
- 1 Million Erase/Write Cycles (minimum)
- 10 Year Data Retention (minimum)
- 5 ms Programming Time (typical)



Micromodule (D10)



Micromodule (D15)



Wafer

DESCRIPTION

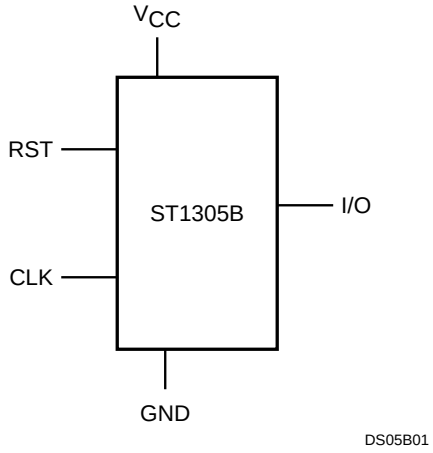
The ST1305B is a 192-bit EEPROM device with associated security logic to control memory access. The circuit includes counting capabilities and thus is very well adapted to prepaid card applications.

The ST1305B is protected by hard-wired security logic and special fuses. The memory is arranged as a matrix of 24x8 cells, accessed in a serial bit-

Table 1. Signal Names

CLK	Clock
RST	Reset
I/O	Serial Data Input/Output
V_{CC}	Supply Voltage
GND	Ground

Figure 1. Logic Diagram



Complete data available under NDA.

wise fashion for reading and programming, and in a byte-wise fashion for internal erasing.

The device recognises three commands issued via the RST and CLK pins (as described in the full data sheet):

– RESET: to reset the internal address register to 00d
– READ: to increment the internal address register, and read the data bit at that address
– PROG: to program the bit at the current address.

The device offers two distinct configurations:

– ISSUER: for the card manufacturer, allowing special data to be written to the chip, during initialisation
– USER: for the end user of the card, restricting access to the chip.

Before delivery, from ST to the card issuer, the device is placed in the ISSUER configuration. This operation is performed by blowing the “test fuse”.

Figure 2. Memory Map

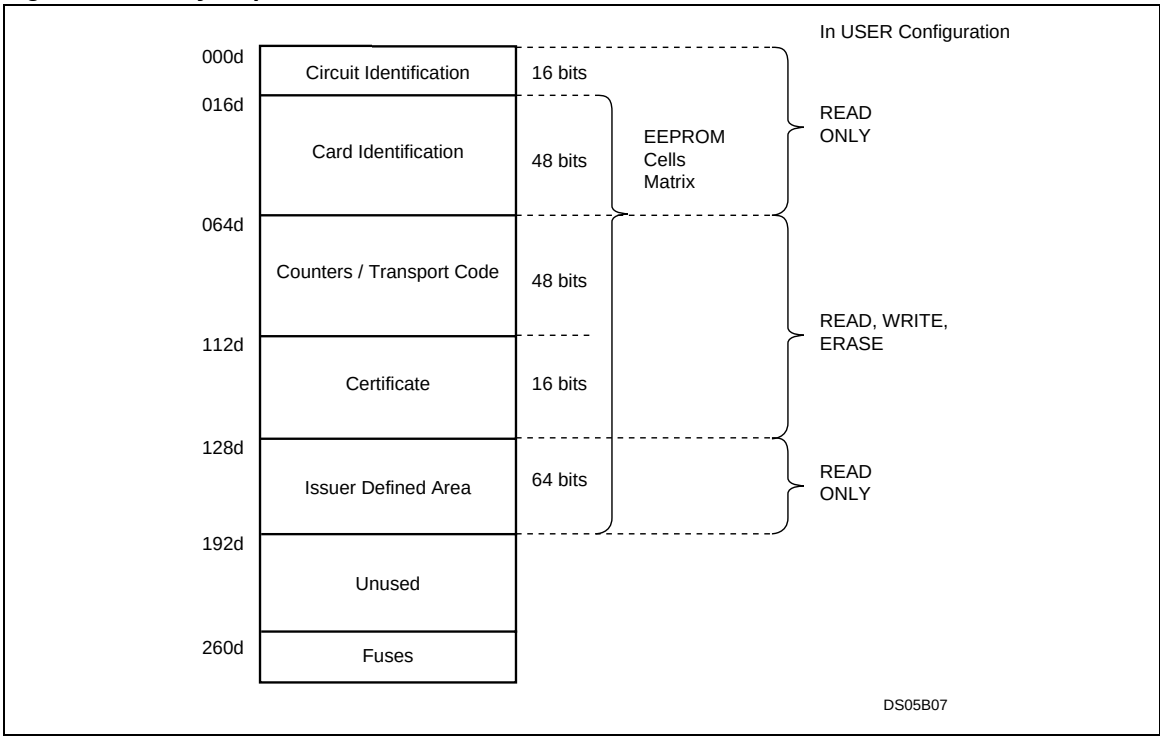


Table 2. Ordering Information Scheme

Example: ST1305B - W4 / XX YY

Delivery Form	
D10	Micromodule on Super 35 mm reel
D15	Micromodule on Super 35 mm reel
W4	Wafer (180 µm thickness)

Transport Code
Given by ST

Customer Code
Given by the Issuer