National Semiconductor

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DP8406 (54F/74F632)
32-Bit Parallel Error Detection and Correction Circuit

General Description

The DP8406 device is a 32-bit parallel error detection and correction circuit (EDAC) in a 52-pin or 68-pin package. The EDAC uses a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDAC to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all LOWs or all HIGHs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

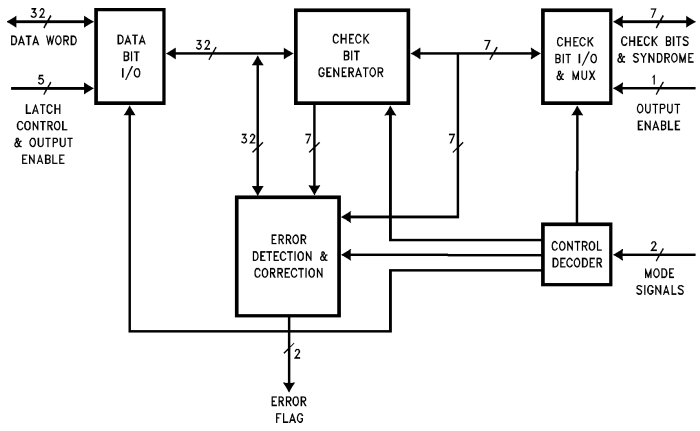
Read-modify-write (byte-control) operations can be performed by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB}}_0$ through $\overline{\text{OEB}}_3$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the Data Bit and Check Bit input latches. These will determine if the failure occurred in memory or in the EDAC.

Features

- Detects and corrects single-bit errors
- Detects and flags dual-bit errors
- Built-in diagnostic capability
- Fast write and read cycle processing times
- Byte-write capability
- Guaranteed 4000V minimum ESD protection
- Fully pin and function compatible with TI's SN74ALS632A thru SN74ALS635 series

Simplified Functional Block



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Device	Package	Byte-Write	Output
DP8406	52-Pin	yes	TRI-STATE®
DP8406	68-Pin	yes	TRI-STATE®

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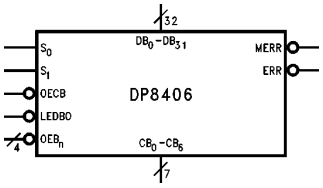
Logic Symbol



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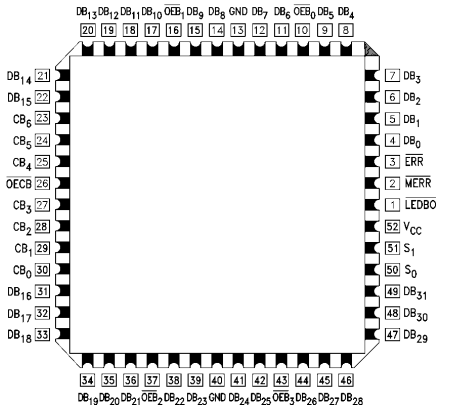
Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CB_0-CB_6	Check Word Bit, Input	3.5/1.083	70 μA/−650 μA
	or TRI-STATE® Output	150/40 (33.3)	−3 mA/24 mA (20 mA)
DB_0-DB_{31}	Data Word Bit, Input	3.5/1.083	70 μA/−650 μA
	or TRI-STATE Output	150/40 (33.3)	−3 mA/24 mA (20 mA)
$\overline{OEB}_0-\overline{OEB}_3$	Output Enable Data Bits	1.0/1.0	20 μA/−0.6 mA
$\overline{LEDBO}$	Output Latch Enable Data Bit	1.0/1.0	20 μA/−0.6 mA
$\overline{OECB}$	Output Enable Check Bit	1.0/1.0	20 μA/−0.6 mA
S_0, S_1	Select Pins	1.0/1.0	20 μA/−0.6 mA
$\overline{ERR}$	Single Error Flag	50/33.3	−1 mA/20 mA
$\overline{MERR}$	Multiple Error Flag	50/33.3	−1 mA/20 mA

Connection Diagrams

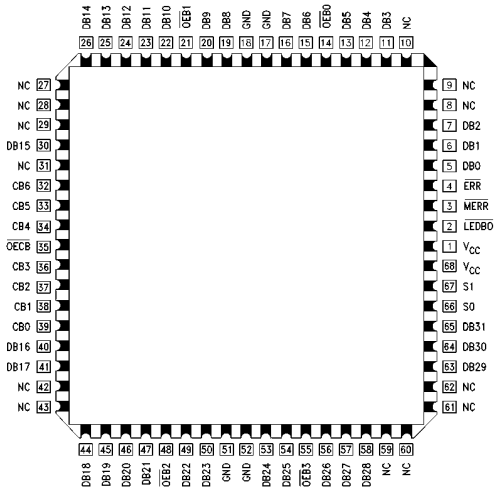
Pin Assignment for LCC and PCC 52-Pin



TL/F/9579–3

Order Number DP8406QV (74F632QC)
See NS Package Number V52A

Pin Assignment for LCC and PCC 68-Pin



NC—No internal connection

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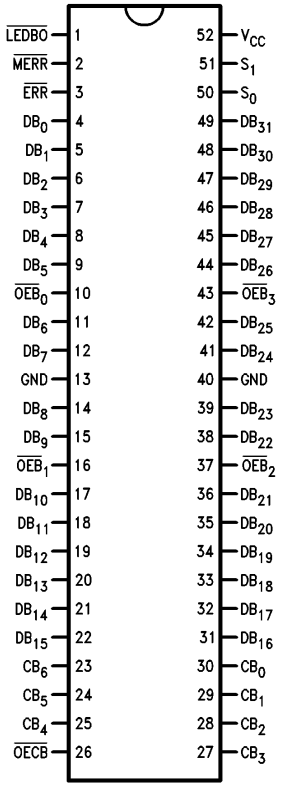
Order Number DP8406V (74F632VC)
See NS Package Number V68A

Connection Diagram (Continued)

Pin Assignment for Side Brazed DIP



TL/F/9579–2

Order Number DP8406D (74F632DC)
See NS Package Number D52A

Functional Description

MEMORY WRITE CYCLE DETAILS

During a memory write cycle, the check bits (CB_0 through CB_6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table II. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.

ERROR DETECTION AND CORRECTION DETAILS

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the HIGH level.

The first case in Table III represents the normal, no-error conditions. The EDAC presents HIGHs on both flags. The next two cases of single-bit errors give a HIGH on $\overline{MERR}$ and a LOW on $\overline{ERR}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal LOWs on both $\overline{ERR}$ and $\overline{MERR}$, which is the interrupt indication for the CPU.

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits is correct, it is assumed that no error has occurred and both error flags will be HIGH.

TABLE I. Write Control Function

Memory Cycle	EDAC Function	Control S_1	Control S_0	Data I/O	DB Control $\overline{OEB_n}$	DB Output Latch $\overline{LEDBO}$	Check I/O	CB Control $\overline{OECB}$	Error Flags $\overline{ERR}$	Error Flags $\overline{MERR}$
Write	Generate Check Word	L	L	Input	H	X	Output Check Bit*	L	H	H

*See Table II for details of check bit generation.

Functional Description (Continued)

TABLE II. Parity Algorithm

Check Word Bit	32-Bit Data Word																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB_0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB_1				X		X		X		X		X		X	X	X				X		X		X		X		X		X	X	X
CB_2	X		X			X	X		X			X	X			X	X		X			X	X		X			X	X			X
CB_3			X	X	X				X	X	X				X	X			X	X	X				X	X	X				X	X
CB_4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB_5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB_6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by X for each bit.

TABLE III. Error Function

Total Number of Errors		Error Flags		Data Correction
32-Bit Data Word	7-Bit Check Word	$\overline{ERR}$	$\overline{MERR}$	
0	0	H	H	Not Applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

H = HIGH Voltage Level
L = LOW Voltage Level

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set LOW. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{ERR}$) will be set LOW while the dual error flag ($\overline{MERR}$) will remain HIGH.

Any 2-bit error will change the state of an even number of check bits. The 2-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set LOW when any 2-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all LOWs and all HIGHs will be detected.

As the corrected word is made available on the data I/O port (DB_0 through DB_{31}), the check word I/O port (CB_0 through CB_6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table V for syndrome decoding.

READ-MODIFY-WRITE (BYTE CONTROL) OPERATIONS

The ’F632 device is capable of byte-write operations. The 39-bit word from memory must first be latched into the Data Bit and Check Bit input latches. This is easily accomplished by switching from the read and flag mode (S_1 = H, S_0 = L) to the latch input mode (S_1 = H, S_0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{LEDBO}$ from a LOW to a HIGH.

Byte control can now be employed on the data word through the $\overline{OEB}_0$ through $\overline{OEB}_3$ controls. $\overline{OEB}_0$ controls DB_0–DB_7 (byte 0), $\overline{OEB}_1$ controls DB_8–DB_{15} (byte 1), $\overline{OEB}_2$ controls DB_{16}–DB_{23} (byte 2), and $\overline{OEB}_3$ controls DB_{24}–DB_{31} (byte 3). Placing a HIGH on the byte control will disable the output and the user can modify the byte. If a LOW is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking controls S_1 and S_0 LOW. Table VI lists the read-modify-write functions.

DIAGNOSTIC OPERATIONS

The ’F632 is capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control. In the diagnostic mode (S_1 = L, S_0 = H), the check word is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known check word. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be LOW. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be LOW. After the check word is latched into the input latch, it can be verified by taking $\overline{OECB}$ LOW. This outputs the latched check word. The diagnostic data word can be latched into the output data latch and verified. By changing from the diagnostic mode (S_1 = L, S_0 = H) to the correction mode (S_1 = H, S_0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table VII lists the diagnostic functions.

Functional Description (Continued)

TABLE IV. Read, Flag and Correct Function

Memory Cycle	EDAC Function	Control S_1	Control S_0	Data I/O	DB Control $\overline{OEB_n}$	DB Output Latch $\overline{LEDBO}$	Check I/O	CB Control $\overline{OECB}$	Error Flags $\overline{ERR}$ $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled (Note 1)
Read	Latch Input Data & Check Bits	H	H	Latched Input Data	H	L	Latched Input Check Word	H	Enabled (Note 1)
Read	Output Corrected Data & Syndrome Bits	H	H	Output Corrected Data Word	L	X	Output Syndrome Bits (Note 2)	L	Enabled (Note 1)

Note 1: See Table III for error description.

Note 2: See Table V for error location.

TABLE V. Syndrome Decoding

Syndrome Bits 6	5	4	3	2	1	0	Error
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-Bit
L	L	L	L	L	H	L	2-Bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-Bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-Bit (Note 2)
L	L	L	H	L	L	L	2-Bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB_{31}
L	L	L	H	L	H	H	2-Bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-Bit
L	L	L	H	H	H	L	2-Bit
L	L	L	H	H	H	H	DB_{30}
L	L	H	L	L	L	L	2-Bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB_{29}
L	L	H	L	L	H	H	2-Bit
L	L	H	L	H	L	L	DB_{28}
L	L	H	L	H	L	H	2-Bit
L	L	H	L	H	H	L	2-Bit
L	L	H	L	H	H	H	DB_{27}
L	L	H	H	L	L	L	DB_{26}
L	L	H	H	L	L	H	2-Bit
L	L	H	H	L	H	L	2-Bit
L	L	H	H	L	H	H	DB_{25}
L	L	H	H	H	L	L	2-Bit
L	L	H	H	H	L	H	DB_{24}
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-Bit

Syndrome Bits 6	5	4	3	2	1	0	Error
L	H	L	L	L	L	L	2-Bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB_7
L	H	L	L	L	H	H	2-Bit
L	H	L	L	H	L	L	DB_6
L	H	L	L	H	L	H	2-Bit
L	H	L	L	H	H	L	2-Bit
L	H	L	L	H	H	H	DB_5
L	H	L	H	L	L	L	DB_4
L	H	L	H	L	L	H	2-Bit
L	H	L	H	L	H	L	2-Bit
L	H	L	H	L	H	H	DB_3
L	H	L	H	H	L	L	2-Bit
L	H	L	H	H	L	H	DB_2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-Bit
L	H	H	L	L	L	L	DB_0
L	H	H	L	L	L	H	2-Bit
L	H	H	L	L	H	L	2-Bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-Bit
L	H	H	L	H	L	H	DB_1
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	2-Bit
L	H	H	H	L	L	L	2-Bit
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-Bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB_6

CB_X = Error in check bit X
DB_Y = Error in data bit Y
2-Bit = Double-bit error
unc = Uncorrectable multi-bit error

Note: 2-bit and unc condition will cause both $\overline{ERR}$ and $\overline{MERR}$ to be LOW
Note 1: Syndrome bits for all LOWs. $\overline{MERR}$ and $\overline{ERR}$ LOW for all LOWs, only $\overline{ERR}$ LOW for DB_{30} error.
Note 2: Syndrome bits for all HIGHs.

Functional Description (Continued)

TABLE V. Syndrome Decoding (Continued)

Syndrome Bits							Error
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-Bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-Bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-Bit
H	L	L	L	H	H	L	2-Bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-Bit
H	L	L	H	L	H	L	2-Bit
H	L	L	H	L	H	H	DB_{15}
H	L	L	H	H	L	L	2-Bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB_{14}
H	L	L	H	H	H	H	2-Bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-Bit
H	L	H	L	L	H	L	2-Bit
H	L	H	L	L	H	H	DB_{13}
H	L	H	L	H	L	L	2-Bit
H	L	H	L	H	L	H	DB_{12}
H	L	H	L	H	H	L	DB_{11}
H	L	H	L	H	H	H	2-Bit
H	L	H	H	L	L	L	2-Bit
H	L	H	H	L	L	H	DB_{10}
H	L	H	H	L	H	L	DB_9
H	L	H	H	L	H	H	2-Bit
H	L	H	H	H	L	L	DB_8
H	L	H	H	H	L	H	2-Bit
H	L	H	H	H	H	L	2-Bit
H	L	H	H	H	H	H	CB_5

Syndrome Bits							Error
6	5	4	3	2	1	0	
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-Bit
H	H	L	L	L	H	L	2-Bit
H	H	L	L	L	H	H	DB_{23}
H	H	L	L	H	L	L	2-Bit
H	H	L	L	H	L	H	DB_{22}
H	H	L	L	H	H	L	DB_{21}
H	H	L	L	H	H	H	2-Bit
H	H	L	H	L	L	L	2-Bit
H	H	L	H	L	L	H	DB_{20}
H	H	L	H	L	H	L	DB_{19}
H	H	L	H	L	H	H	2-Bit
H	H	L	H	H	L	L	DB_{18}
H	H	L	H	H	L	H	2-Bit
H	H	L	H	H	H	L	2-Bit
H	H	L	H	H	H	H	CB_4
H	H	H	L	L	L	L	2-Bit
H	H	H	L	L	L	H	DB_{16}
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-Bit
H	H	H	L	H	L	L	DB_{17}
H	H	H	L	H	L	H	2-Bit
H	H	H	L	H	H	L	2-Bit
H	H	H	L	H	H	H	CB_3
H	H	H	H	L	L	L	unc (Note 1)
H	H	H	H	L	L	H	2-Bit
H	H	H	H	L	H	L	2-Bit
H	H	H	H	L	H	H	CB_2
H	H	H	H	H	L	L	2-Bit
H	H	H	H	H	L	H	CB_1
H	H	H	H	H	H	L	CB_0
H	H	H	H	H	H	H	None

CB_X = Error in check bit X
DB_Y = Error in data bit Y
2-Bit = Double-bit error
unc = Uncorrectable multi-bit error

Note: 2-bit and unc condition will cause both $\overline{ERR}$ and $\overline{MERR}$ to be LOW
Note 1: Syndrome bits for all LOWs. $\overline{MERR}$ and $\overline{ERR}$ LOW for all LOWs, only $\overline{ERR}$ LOW for DB_{30} error.
Note 2: Syndrome bits for all HIGHs.

Functional Description (Continued)

TABLE VI. Read-Modify-Write Function

Memory Cycle	EDAC Function	Control S_1	Control S_0	BYTEn*	$\overline{OEB}$n*	DB Output Latch $\overline{LEDBO}$	Check I/O	CB Control $\overline{OECB}$	Error Flags $\overline{ERR}$	Error Flags $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch Input Data & Check Bits	H	H	Latched Input Data	H	L	Latched Input Check Word	H	Enabled	
Read	Latch Corrected Data Word into Output Latch	H	H	Latched Output Data Word	H	H	High Z	H	Enabled	
							Output Syndrome Bits	L		
Modify/ Write	Modify Appropriate Byte or Bytes & Generate New Check Word	L	L	Input Modified $BYTE_0$	H	H	Output Check Word	L	H	H
				Output Unchanged $BYTE_0$	L					

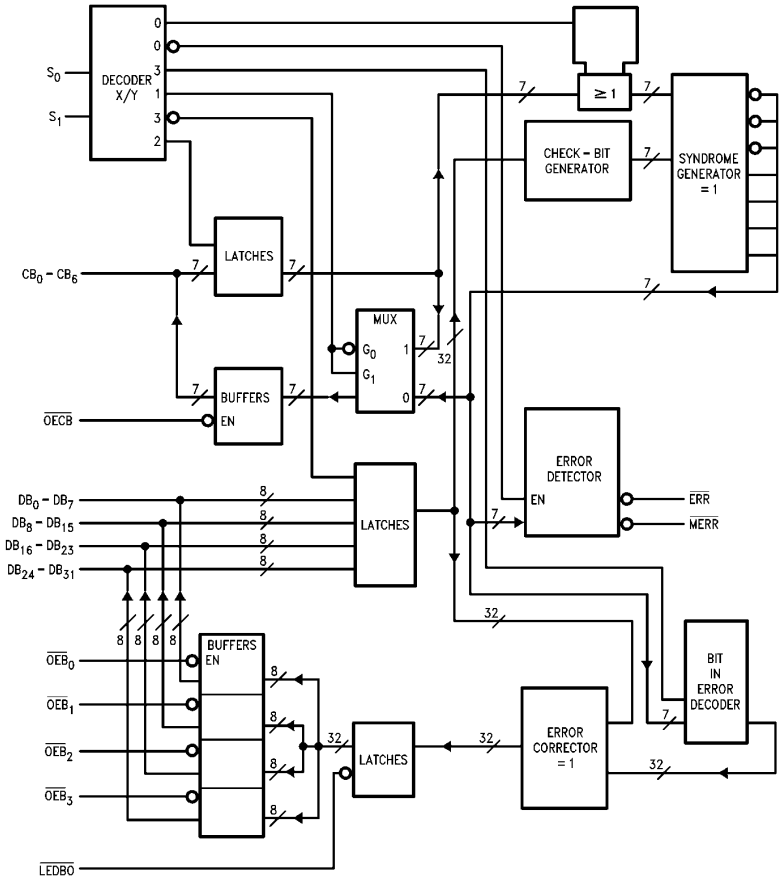
*$\overline{OEB}_0$ controls DB_0–DB_7 ($BYTE_0$); $\overline{OEB}_1$ controls DB_8–DB_{15} ($BYTE_1$); $\overline{OEB}_2$ controls DB_{16}–DB_{23} ($BYTE_2$); $\overline{OEB}_3$ controls DB_{24}–DB_{31} ($BYTE_3$).

TABLE VII. Diagnostic Function

EDAC Function	Control S_1	Control S_0	Data I/O	DB Byte Control $\overline{OEB}_n$	DB Output Latch $\overline{LEDBO}$	Check I/O	CB Control $\overline{OECB}$	Error Flags $\overline{ERR}$	Error Flags $\overline{MERR}$
Read & Flag	H	L	Input Correct Data Word	H	X	Input Correct Check Bits	H	H	
Latch Input Check Word while Data Input Latch Remains Transparent	L	H	Input Diagnostic Data Word*	H	L	Latched Input Check Bits	H	Enabled	
Latch Diagnostic Data Word into Output Latch	L	H	Input Diagnostic Data Word*	H	H	Output Latched Check Bits	L	Enabled	
						High Z	H		
Latch Diagnostic Data Word into Input Latch	H	H	Latched Input Diagnostic Data Word	H	H	Output Syndrome Bits	L	Enabled	
						High Z	H		
Output Diagnostic Data Word & Syndrome Bits	H	H	Output Diagnostic Data Word	L	H	Output Syndrome Bits	L	Enabled	
						High Z	H		
Output Corrected Diagnostic Data Word & Output Syndrome Bits	H	H	Output Corrected Diagnostic Data Word	L	L	Output Syndrome Bits	L	Enabled	
						High Z	H		

*Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case,the diagnostic data word will contain errors in two bit locations.

Block Diagram



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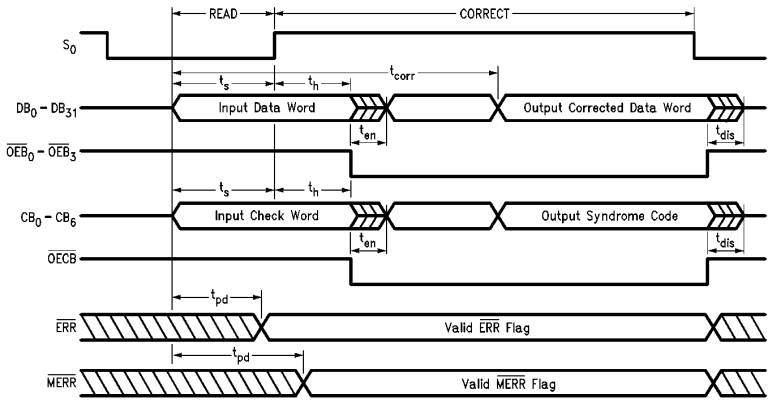
Timing Waveforms

Read, Flag and Correct Mode



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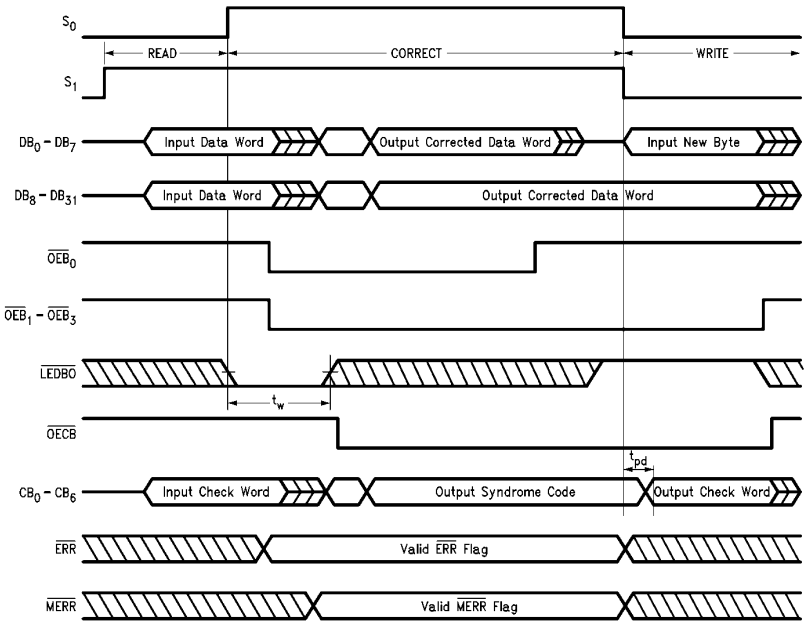
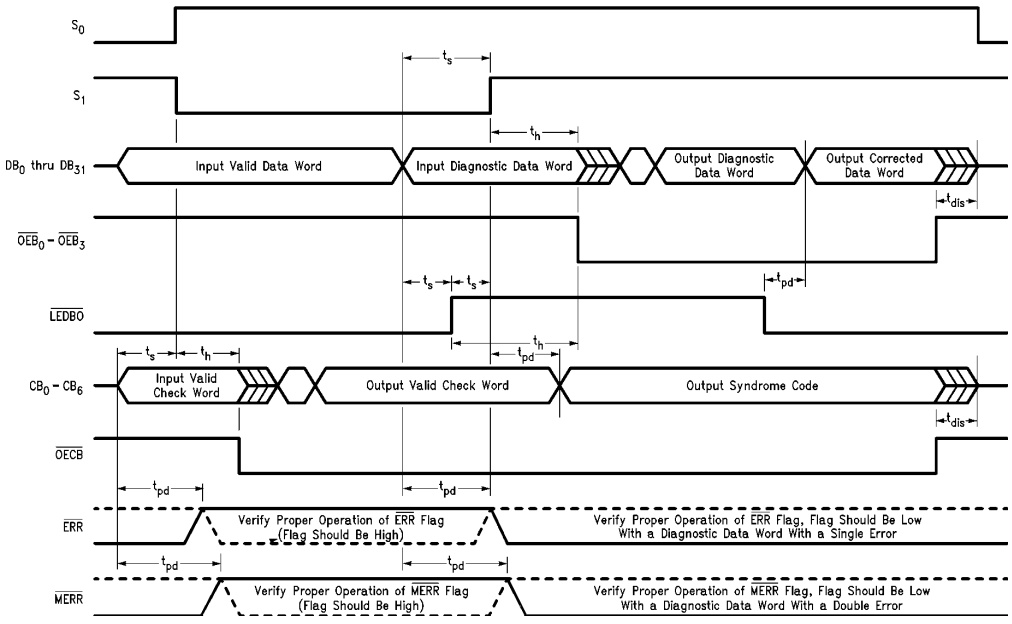
Timing Waveforms (Continued)

Read, Correct and Modify Mode



TL/F/9579–6

Diagnostic Mode



TL/F/9579–7

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA ($\overline{ERR}$, $\overline{MERR}$, DB_n, CB_n)
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA (DB_n, CB_n)
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA ($\overline{ERR}$, $\overline{MERR}$, DB_n, CB_n)
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA (DB_n, CB_n)
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA ($\overline{ERR}$, $\overline{MERR}$, DB_n, CB_n)
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA (DB_n, CB_n)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA ($\overline{ERR}$, $\overline{MERR}$, DB_n, CB_n)
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA ($\overline{ERR}$, $\overline{MERR}$)
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA (DB_n, CB_n)
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V (S_0, S_1, $\overline{OEB_n}$, $\overline{OECB}$, $\overline{LEDBO}$)
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V (S_0, S_1, $\overline{OEB_n}$, $\overline{OECB}$, $\overline{LEDBO}$)
		74F			7.0			
I_{BVIT}	Input HIGH Current Breakdown (I/O)	54F			1.0	mA	Max	V_{IN} = 5.5V (CB_n, DB_n)
		74F			0.5			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (S_0, S_1, $\overline{OEB_n}$, $\overline{OECB}$, $\overline{LEDBO}$)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	$V_{I/O}$ = 2.7V (CB_n, DB_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	$V_{I/O}$ = 0.5V (CB_n, DB_n)
I_{OZH}	Output Leakage Current				70	μA	Max	$V_{I/O}$ = 2.7V (CB_n, DB_n)
I_{OZL}	Output Leakage Current				−650	μA	Max	$V_{I/O}$ = 0.5V (CB_n, DB_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V (CB_n, DB_n)
I_{CC}	Power Supply Current				340	mA	Max	T_A = 0°C–25°C
I_{CC}	Power Supply Current				325	mA	Max	T_A = 25°C–70°C

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F $T_A, V_{CC} =$ Mil, $C_L = 50$ pF		74F $T_A, V_{CC} =$ Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay DB or CB to $\overline{ERR}$	4.0 4.0	14.0 10.5	27.0 18.0			4.0 4.0	31.0 20.0	ns
t_{PLH} t_{PHL}	Propagation Delay DB to $\overline{ERR}$	4.0 4.0	21.0 14.0	27.0 18.0			4.0 4.0	31.0 20.0	ns
t_{PLH} t_{PHL}	Propagation Delay DB or CB to $\overline{MERR}$	5.0 5.0	17.0 16.0	27.0 27.0			5.0 5.0	31.0 31.0	ns
t_{PLH} t_{PHL}	Propagation Delay DB to $\overline{MERR}$	5.0 5.0	23.0 19.0	27.0 27.0			5.0 5.0	31.0 31.0	ns
t_{PLH} t_{PHL}	Propagation Delay S_0 and S_1, LOW, to DB	4.0 4.0	12.0 12.0	16.0 16.0			4.0 4.0	20.0 20.0	ns
t_{PLH} t_{PHL}	Propagation Delay S_1 to CB	4.0 4.0	10.5 9.0	14.0 14.0			4.0 4.0	15.0 15.0	ns
t_{PLH}	Propagation Delay S_0 or S_1 to $\overline{ERR}$ or $\overline{MERR}$	2.0	11.5	13.0			2.0	14.0	ns
t_{PLH} t_{PHL}	Propagation Delay DB to CB	4.0 4.0	16.0 18.0	23.0 23.0			4.0 4.0	25.0 25.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEDBO}$ to DB	2.0 2.0	11.0 11.0	13.0 13.0			2.0 2.0	14.0 14.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEB}_n$ to DB	1.0 1.0	6.0 6.0	10.0 10.0			1.0 1.0	10.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEB}_n$ to DB	10 1.0	5.0 4.0	10.0 10.0			1.0 1.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OECB}$ to CB	1.0 1.0	6.0 6.0	10.0 10.0			1.0 1.0	10.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OECB}$ to CB	1.0 1.0	5.0 4.0	10.0 10.0			1.0 1.0	10.0 10.0	ns

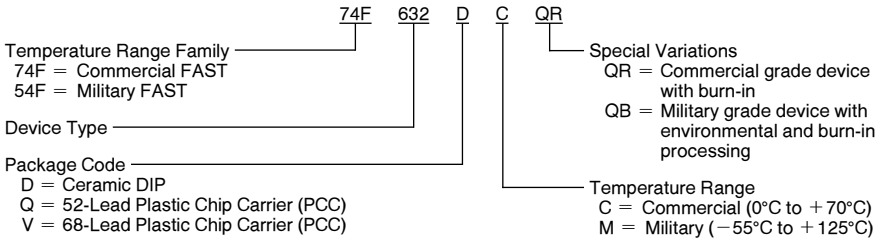
AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	Min	Max	
t_s	Setup Time, HIGH or LOW DB/CB before S_0 HIGH (S_1 HIGH)	3.0				3.0		ns
$t_s(H)$	Setup Time, HIGH S_0 HIGH before $\overline{LEDBO}$ HIGH	12.0				14.0		ns
$t_s(H)$	Setup Time, HIGH $\overline{LEDBO}$ HIGH before S_0 or S_1 LOW	0				0		ns
$t_s(H)$	Setup Time, HIGH $\overline{LEDBO}$ HIGH before S_1 HIGH	0				0		ns
t_s	Setup Time, HIGH or LOW Diagnostic DB before S_1 HIGH	0				0		ns
t_s	Setup Time, HIGH or LOW Diagnostic CB before S_1 LOW or S_0 HIGH	3.0				3.0		ns
t_s	Setup Time, HIGH or LOW Diagnostic DB before $\overline{LEDBO}$ HIGH (S_1 LOW, S_0 HIGH)	8.0				8.0		ns
$t_h(L)$	Hold Time, LOW S_0 LOW after S_1 HIGH	8.0				8.0		ns
t_h	Hold Time, HIGH or LOW DB and CB Hold after S_0 HIGH	8.0				8.0		ns
t_h	Hold Time, HIGH or LOW DB Hold after S_1 HIGH	8.0				8.0		ns
t_h	Hold Time, HIGH or LOW CB Hold after S_1 LOW or S_0 HIGH	5.0				5.0		ns
t_h	Hold Time, HIGH or LOW Diagnostic DB after $\overline{LEDBO}$ HIGH (S_1 LOW, S_0 HIGH)	0				0		ns
$t_w(L)$*	$\overline{LEDBO}$ Pulse Width	8.0				8.0		ns
t_{corr}*	Correction Time		25.0				28.0	ns

*__Note:__ These parameters are guaranteed by characterization or other tests performed.

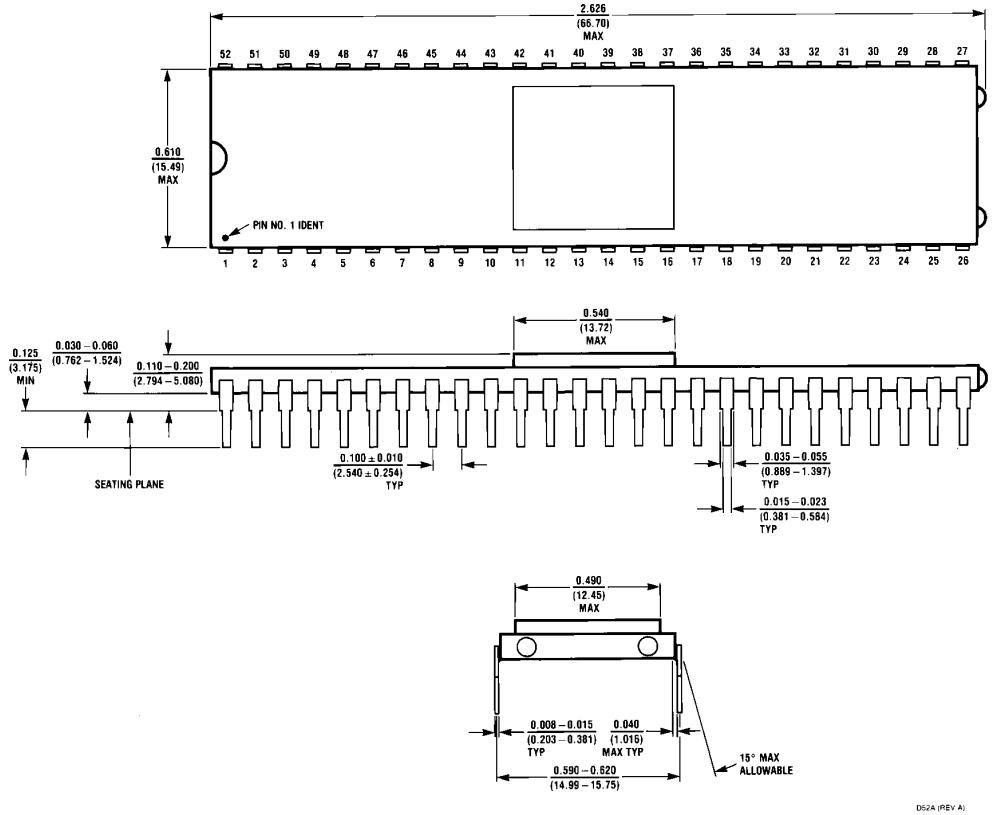
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

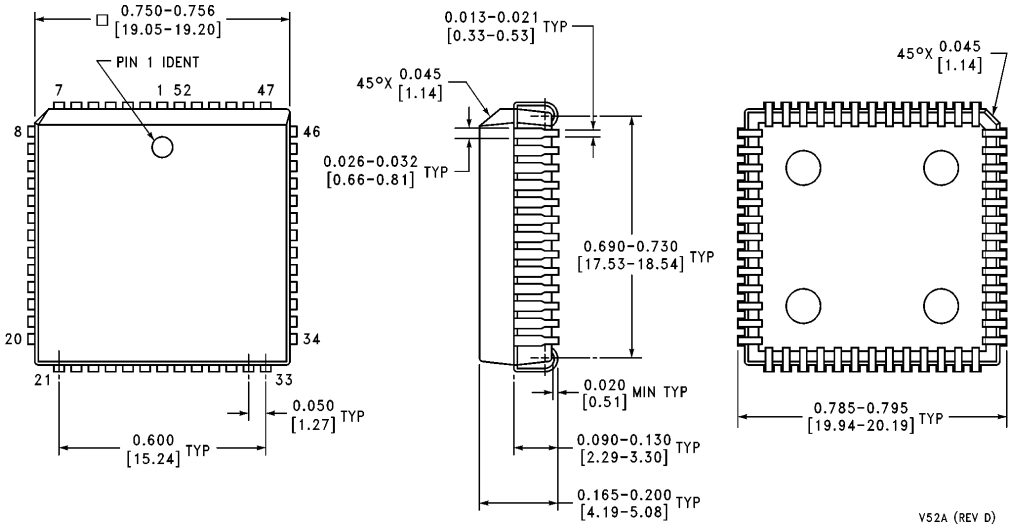


*Order DP8406QV, DP8406V or DP8406D

Physical Dimensions inches (millimeters)

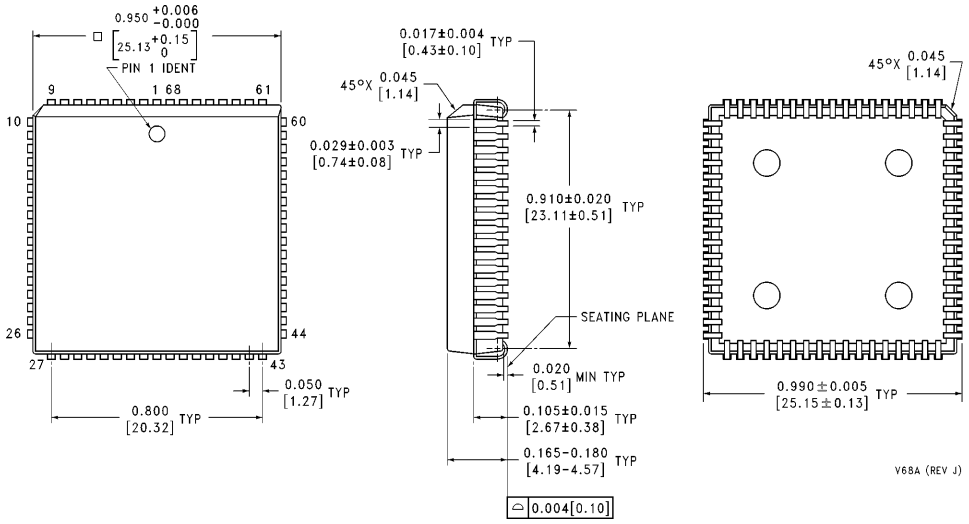


52-Lead Side-Brazed Ceramic Dual-In-Line Package (D)
NS Package Number D52A



52-Lead Plastic Chip Carrier (Q)
NS Package Number V52A

Physical Dimensions inches (millimeters) (Continued)



68-Lead Plastic Chip Carrier (V)
NS Package Number V68A

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