

**Features**

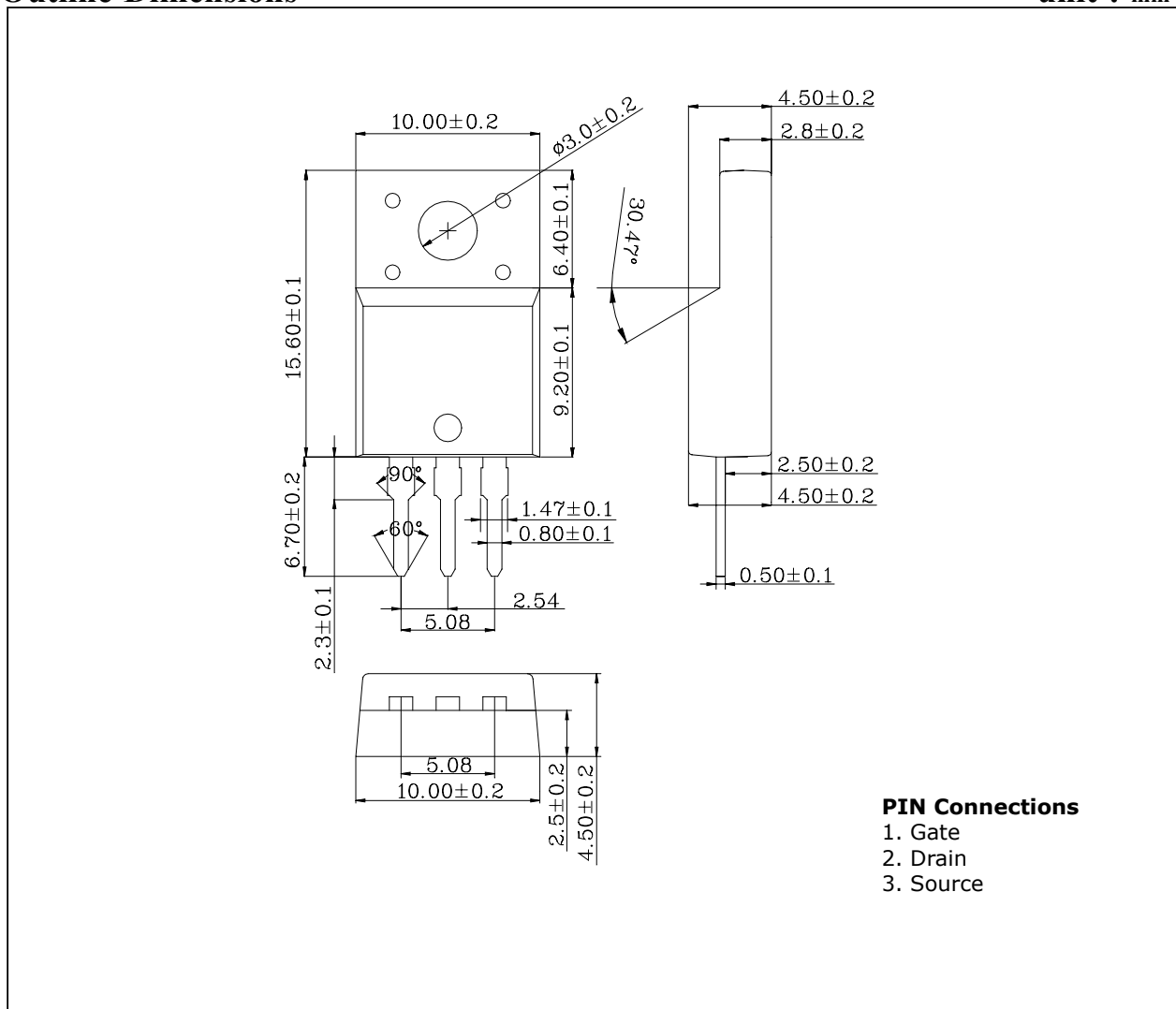
- Avalanche rugged technology.
- Low input capacitance.
- Improved gate charge.
- Low leakage current : 10uA (Max.) @  $V_{DS}=400V$ .

**Ordering Information**

Type NO.	Marking	Package Code
STK730FC	STK730	TO-220F-3SL

**Outline Dimensions**

unit : mm



**PIN Connections**

1. Gate
2. Drain
3. Source

## Absolute maximum ratings

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	$V_{DSS}$	400	V
Gate-Source voltage	$V_{GS}$	$\pm 30$	V
Continuous Drain current (Tc=25°C)	$I_D$	5.5*	A
Continuous Drain current (Tc=100°C)	$I_D$	3.5*	A
Drain Current-Pulsed ①	$I_{DM}$	22	A
Power Dissipation (Tc=25°C)	$P_D$	38	W
Linear Derating Factor		0.3	W/°C
Single Pulsed Avalanche Energy ②	$E_{AS}$	346	mJ
Avalanche current ①	$I_{AR}$	5.5	A
Repetitive Avalanche Energy ①	$E_{AR}$	7.3	mJ
Peak Diode Recovery dv/dt	dv/dt	4.0	V/ns
Operating Junction and Storage temperature range	$T_J, T_{stg}$	-55~150	°C
Maximum lead temp. for soldering Purpose, 1/8" from case for 5-seconds	$T_L$	300	°C

\* Limited by Maximum junction Temperature

## Thermal Resistance

Characteristic	Symbol	Typ.	Max	Units
Junction-to-Case	$R_{\theta JC}$		3.31	°C/W
Case-to-Sink	$R_{\theta CS}$	0.5		
Junction-to-Ambient	$R_{\theta JA}$		62.5	

## Electrical Characteristics (Tc=25°C unless otherwise specified)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-Source breakdown voltage	$BV_{DSS}$	$I_D=250\mu A, V_{GS}=0$	400			V
Gate-Threshold voltage	$V_{GS(th)}$	$I_D=250\mu A, V_{DS}=5V$	2.0		4.0	V
Drain-source leakage current	$I_{DSS}$	$V_{DS}=400V$			10	$\mu A$
Gate-source leakage	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 30V$			$\pm 100$	nA
Drain-Source on-resistance ④	$R_{DS(on)}$	$V_{GS}=10V, I_D=2.75A$			1.0	$\Omega$
Forward transconductance ④	$g_{fs}$	$V_{DS}=50V, I_D=2.75A$		4.03		S
Input capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=25V, f=1MHz$		790	1000	pF
Output capacitance	$C_{oss}$			80	100	
Reverse transfer capacitance	$C_{rss}$			20	26	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=200V, I_D=5.5A$ $R_G=12\Omega$		15	40	ns
Rise time	$t_r$			18	50	
Turn-off delay time	$t_{d(off)}$			62	140	
Fall time	$t_f$			22	60	
Total gate charge	$Q_g$	$V_{DS}=320V, V_{GS}=10V,$ $I_D=5.5A$		32	42	nC
Gate-source charge	$Q_{gs}$			4.6		
Gate-drain("Miller")charge	$Q_{gd}$			16.6		

## Source-Drain Diode Ratings and Characteristics

Characteristic	Symbol	Test Condition	Min	Typ	Max	Units
Continuous source current	$I_S$	Integral reverse pn-diode in the MOSFET			5.5	A
Pulsed-source current ①	$I_{SM}$				22	
Diode forward voltage ④	$V_{SD}$	$T_J=25^\circ C, V_{GS}=0V, I_S=5.5A$			1.5	V
Reverse recovery time	$t_{rr}$	$T_J=25^\circ C, I_F=5.5A$ $di_F/dt=100A/us$		259		ns
Reverse recovery charge	$Q_{rr}$			1.81		$\mu C$

Note ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ②  $L=20mH, I_{AS}=5.5A, V_{DD}=50V, R_G=27\Omega$  , starting  $T_J=25^\circ C$
- ③  $I_{SD} \leq 5.5A, di/dt \leq 140A/us, V_{DD} \leq BV_{DSS}$ , starting  $T_J=25^\circ C$
- ④ Pulse Test : Pulse Width=250us, Duty cycle $\leq 2\%$
- ⑤ Essentially independent of operating temperature

Electrical Characteristic Curves

Fig. 1  $I_D - V_{DS}$

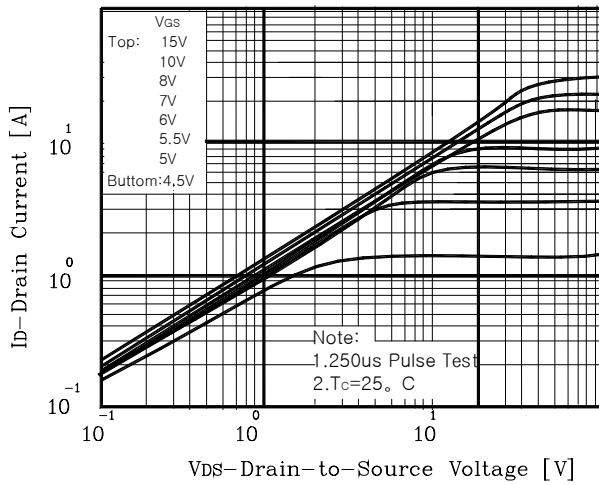


Fig. 2  $I_D - V_{GS}$

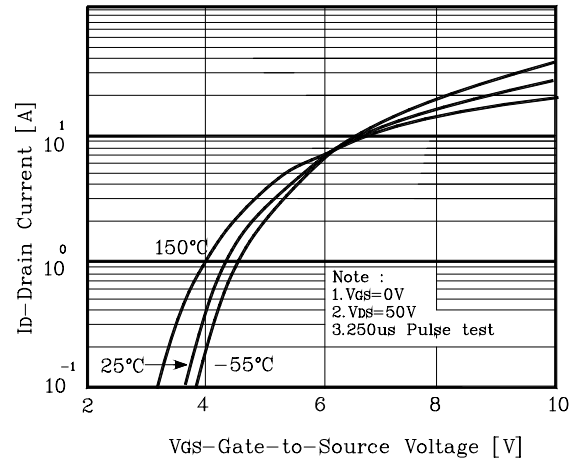


Fig. 3  $R_{DS(on)} - I_D$

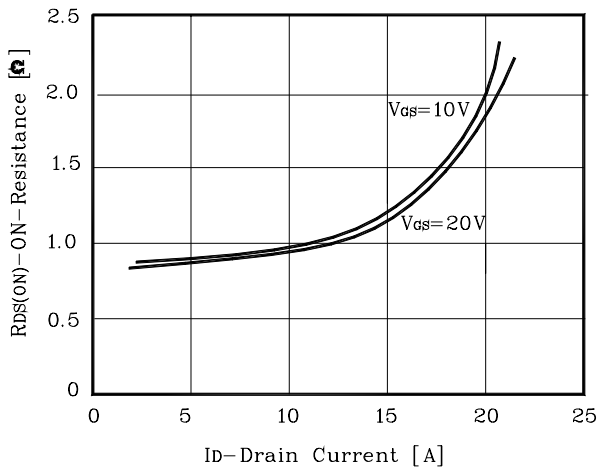


Fig. 4  $I_{DR} - V_{SD}$

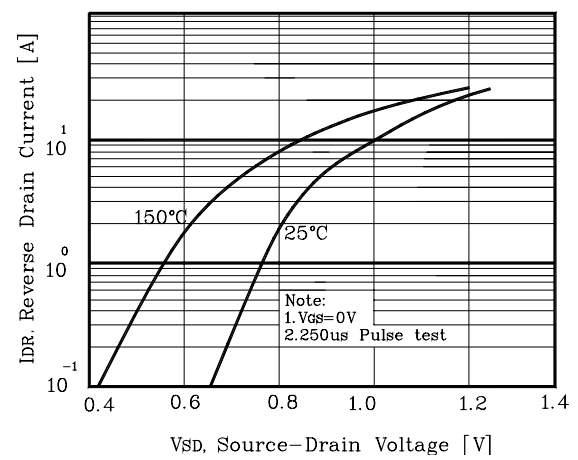


Fig. 5 Capacitance -  $V_{DS}$

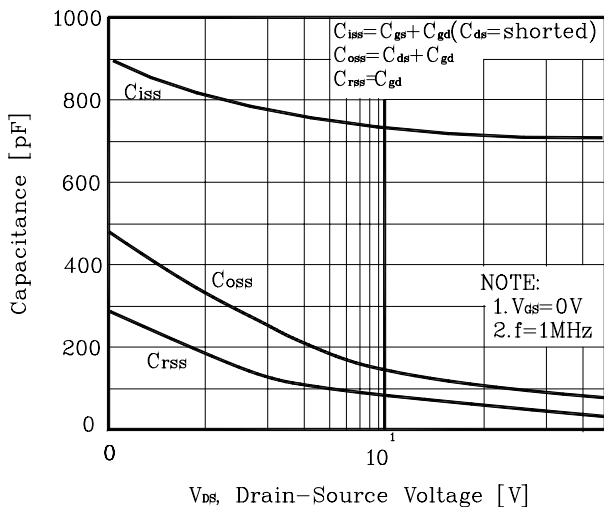
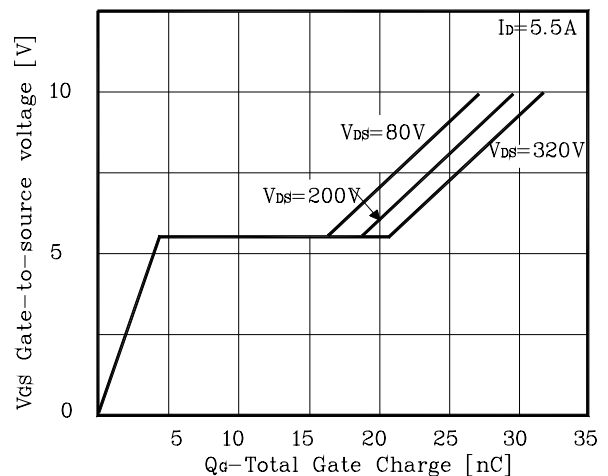
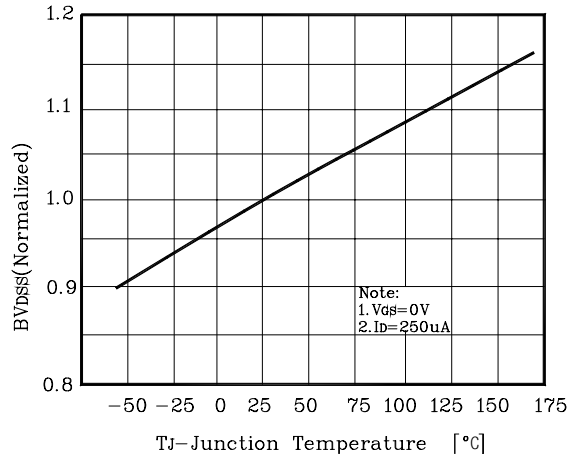


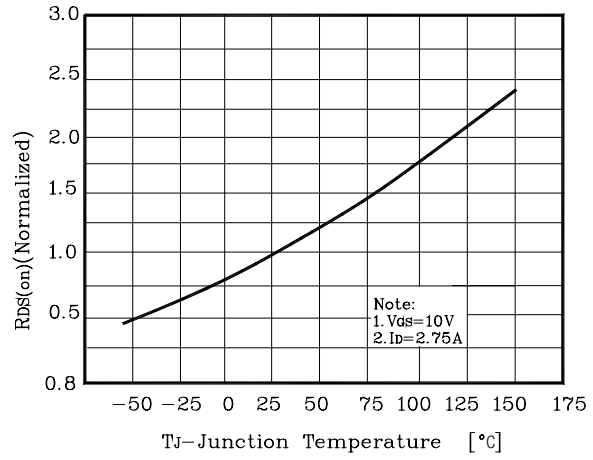
Fig. 6  $V_{GS} - Q_G$



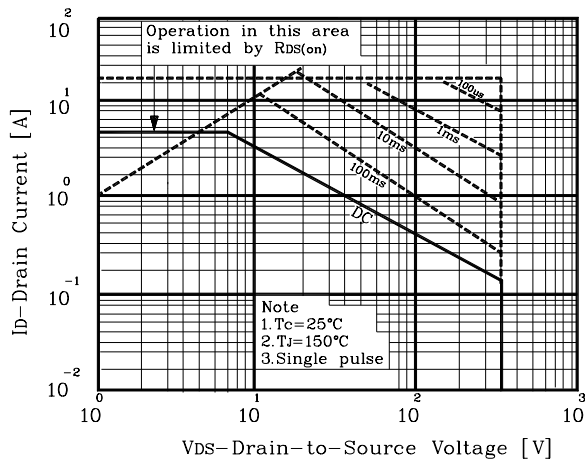
**Fig. 7  $BV_{DSS} - T_J$**



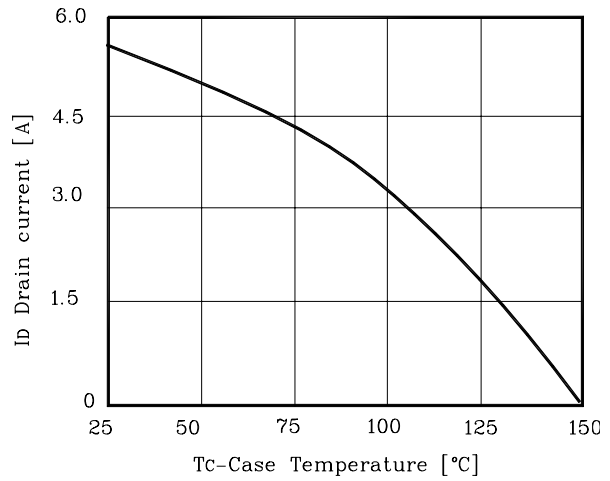
**Fig. 8  $R_{DS(on)} - T_J$**



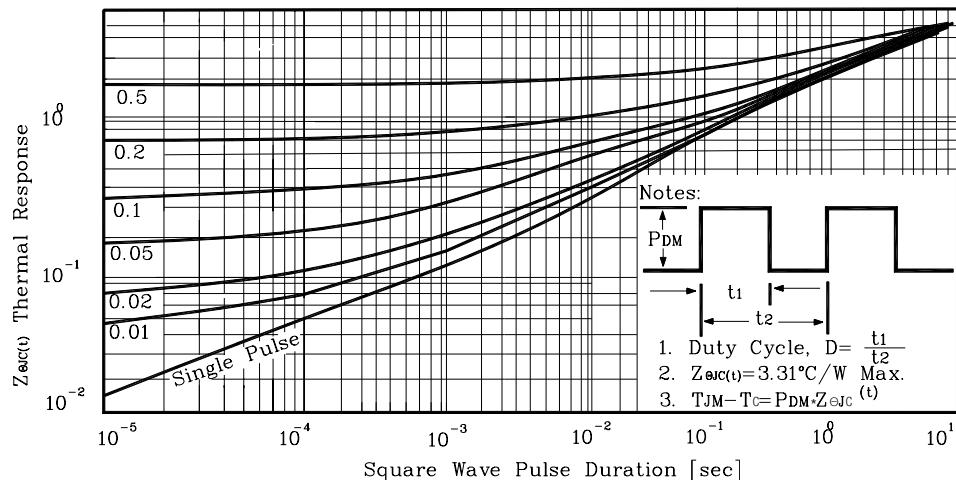
**Fig. 9 Safe operating Area**



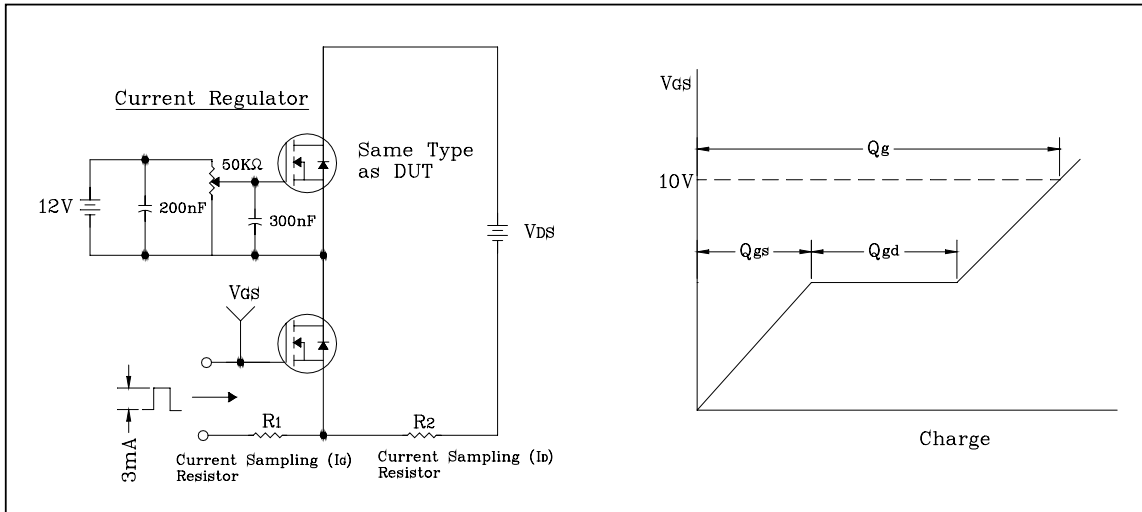
**Fig. 10  $I_D - T_C$**



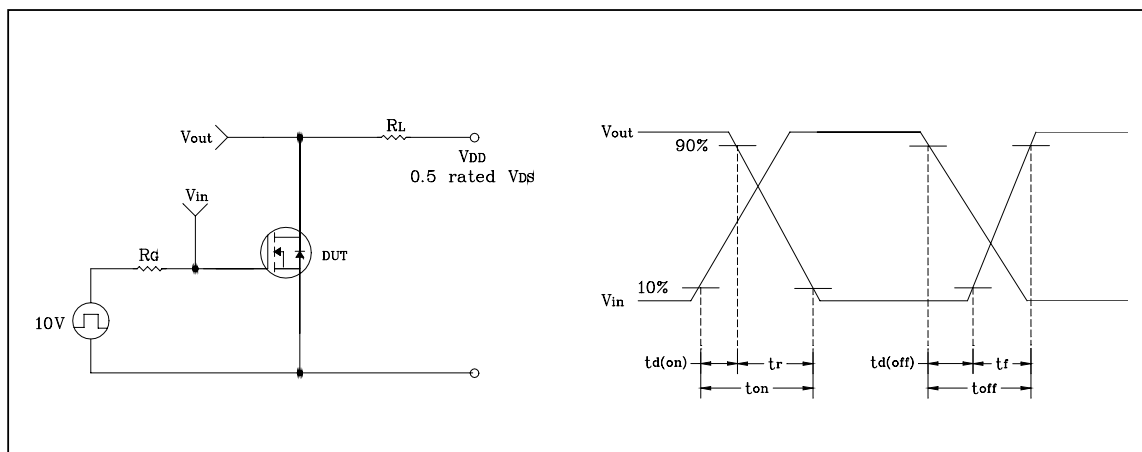
**Fig. 11 Thermal Response**



**Fig. 12 Gate Charge Test Circuit & Waveform**



**Fig. 13 Resistive Switching Test Circuit & Waveform**



**Fig. 14 Unclamped Inductive Switching Test Circuit & Waveform**

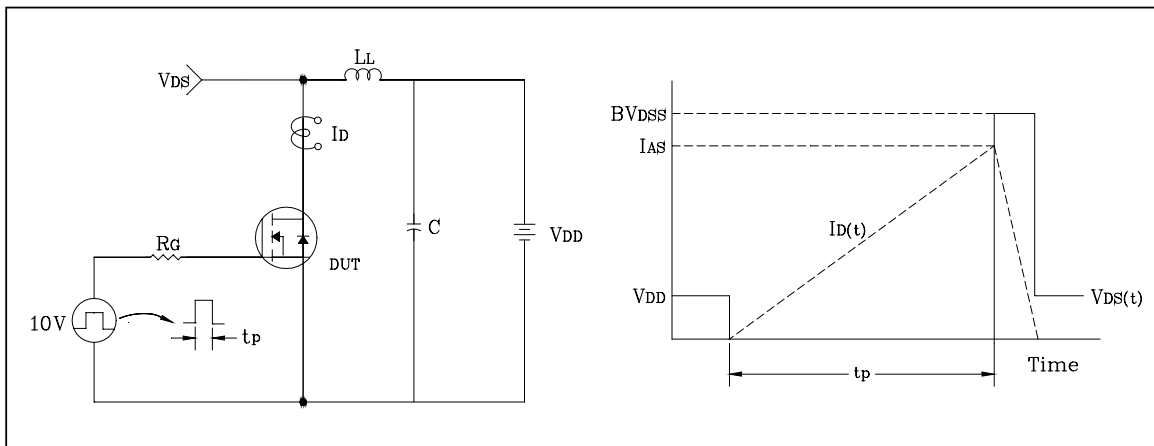
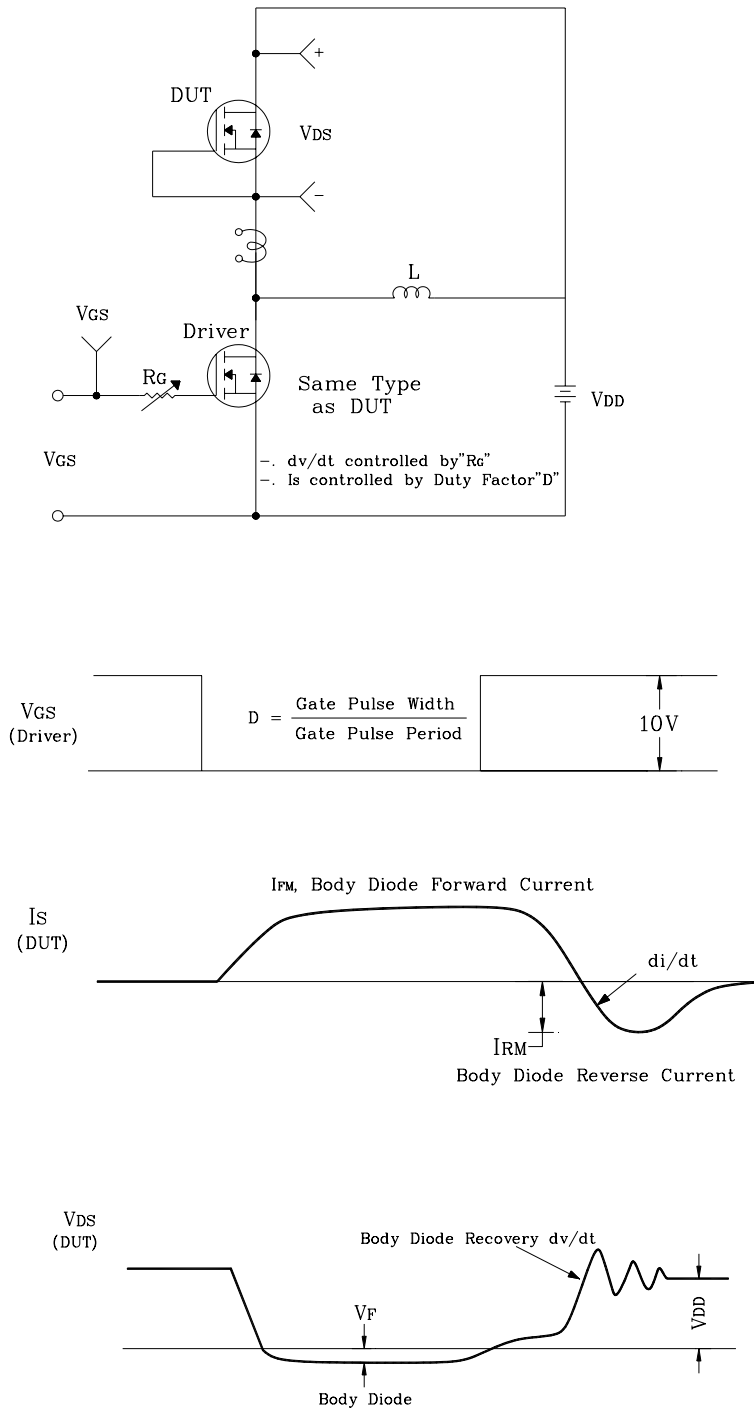


Fig. 15 Peak Diode Recovery dv/dt Test Circuit & Waveform



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