FAIRCHILD SEMICONDUCTOR™

April 1988
Revised September 2000

74F160A • 74F162A
Synchronous Presettable BCD Decade Counter

General Description

The 74F160A and 74F162A are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for applications in programmable dividers. There are two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The F160A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The F162A has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock. The F160A and F162A are high speed versions of the F160 and F162.

Features

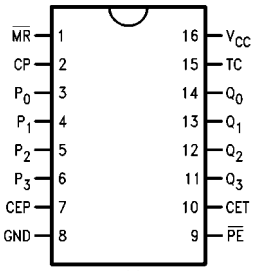
- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 120 MHz

Ordering Code:

Order Number	Package Number	Package Description
74F160ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F160ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F160APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74F162ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F162APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams



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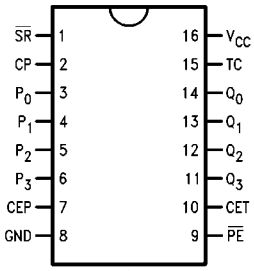

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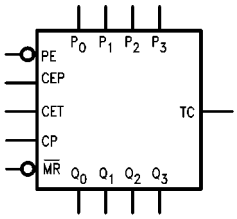
Logic Symbols



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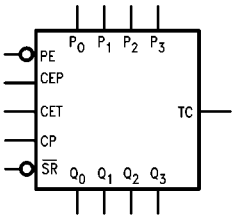

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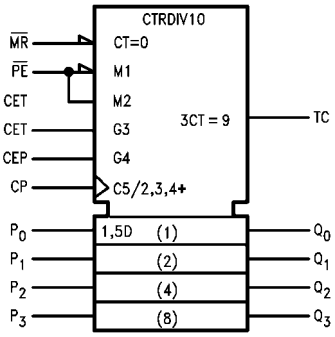
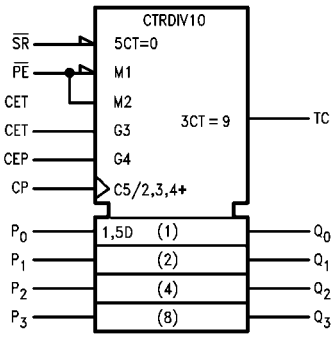
IEEE/IEC



74F160A



74F162A

Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CEP	Count Enable Parallel Input	1.0/1.0	20 µA/–0.6 mA
CET	Count Enable Trickle Input	1.0/2.0	20 µA/–1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
$\overline{MR}$ (74F160A)	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{SR}$ (74F162A)	Synchronous Reset Input (Active LOW)	1.0/2.0	20 µA/–1.2 mA
P_0–P_3	Parallel Data Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/2.0	20 µA/–1.2 mA
Q_0–Q_3	Flip-Flop Outputs	50/33.3	–1 mA/20 mA
TC	Terminal Count Output	50/33.3	–1 mA/20 mA

Functional Description

The 74F160A and 74F162A count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the (F160A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (F160A), synchronous reset (F162A), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, F160A), Synchronous Reset ($\overline{SR}$, F162A), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ (F160A) or $\overline{SR}$ (F162A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The F160A and F162A use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the F160A and F162A decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations:

$$\text{Count Enable} = CEP \times CET \times \overline{PE}$$

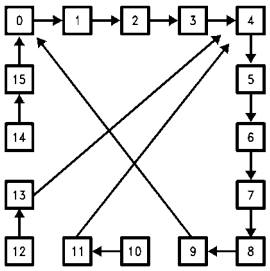
$$TC = Q_0 \times \overline{Q}_1 \times \overline{Q}_2 \times Q_3 \times CET$$

Mode Select Table

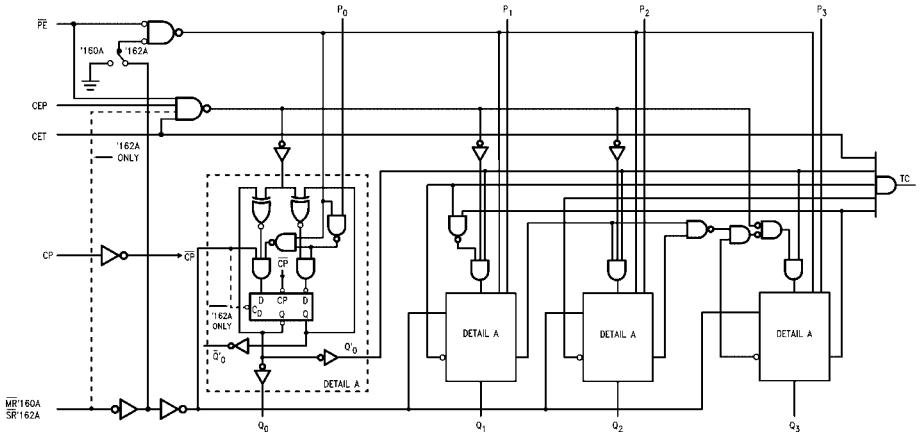
*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For 74'F162A only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
	Voltage 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW 10% V_{CC} Voltage			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current			5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current			3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW			−0.6	mA	Max	V_{IN} = 0.5V (CP, CEP,P_n, $\overline{MR}$ (F160A))
	Current			−1.2	mA	Max	V_{IN} = 0.5V (CET, $\overline{SR}$ (F162A), $\overline{PE}$)
I_{OS}	Output Short-Circuit Current	−60		−150	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current		37	55	mA	Max	V_O = HIGH

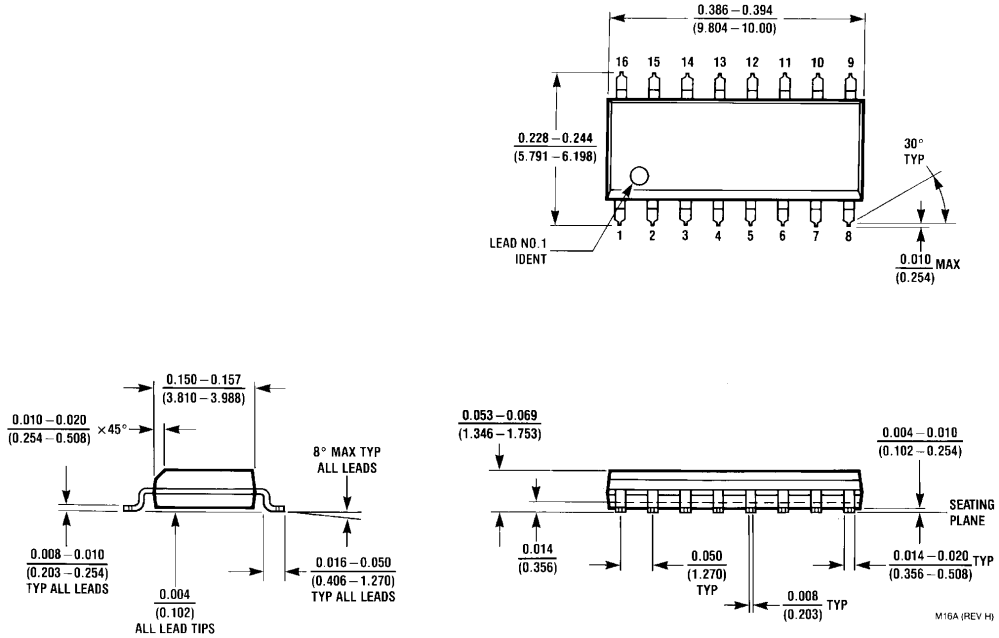
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Count Frequency	90	120		75		80		MHz
t_{PLH}	Propagation Delay, Count	3.5	5.5	7.5	3.5	9.0	3.5	8.5	ns
t_{PHL}	CP to Q_n ($\overline{PE}$ Input HIGH)	3.5	7.5	10.0	3.5	11.5	3.5	11.0	
t_{PLH}	Propagation Delay, Load	4.0	6.0	8.5	4.0	10.0	4.0	9.5	ns
t_{PHL}	CP to Q_n ($\overline{PE}$ Input LOW)	4.0	6.0	8.5	4.0	10.0	4.0	9.5	
t_{PLH}	Propagation Delay	5.0	10.0	14.0	5.0	16.5	5.0	15.0	ns
t_{PHL}	CP to TC	5.0	10.0	14.0	5.0	15.5	5.0	15.0	
t_{PLH}	Propagation Delay	2.5	4.5	7.5	2.5	9.0	2.5	8.5	ns
t_{PHL}	CET to TC	2.5	4.5	7.5	2.5	9.0	2.5	8.5	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n (74F160A)	5.5	9.0	12.0	5.5	14.0	5.5	13.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC (74F160A)	4.5	8.0	10.5	4.5	12.5	4.5	11.5	ns

AC Operating Requirements

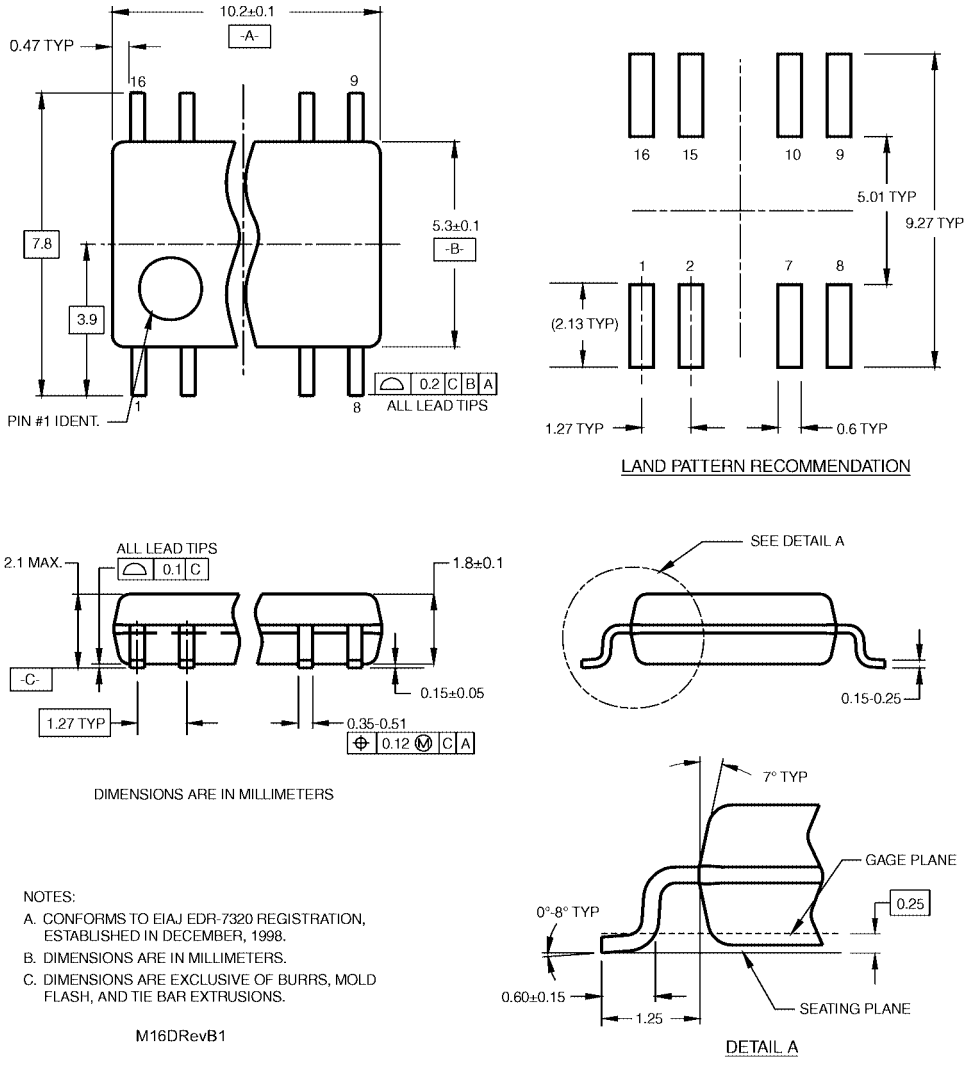
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	4.0		5.5		4.0		ns
$t_S(L)$	P_n to CP (74F160A)	5.0		5.5		5.0		
$t_S(H)$	Setup Time, HIGH or LOW	5.0				5.0		ns
$t_S(L)$	P_n to CP (74F162A)	5.0				5.0		
$t_H(H)$	Hold Time, HIGH or LOW	2.0		2.5		2.0		
$t_H(L)$	P_n to CP	2.0		2.5		2.0		
$t_S(H)$	Setup Time, HIGH or LOW	11.0		13.5		11.5		ns
$t_S(L)$	$\overline{PE}$ or $\overline{SR}$ to CP	8.5		10.5		9.5		
$t_H(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0		
$t_H(L)$	$\overline{PE}$ or $\overline{SR}$ to CP	0		0		0		
$t_S(H)$	Setup Time, HIGH or LOW	11.0		13.0		11.5		ns
$t_S(L)$	CEP or CET to CP	5.0		6.0		5.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		0		
$t_H(L)$	CEP or CET to CP	0		0		0		
$t_W(H)$	Clock Pulse Width (Load)	5.0		5.0		5.0		ns
$t_W(L)$	HIGH or LOW	5.0		5.0		5.0		
$t_W(H)$	Clock Pulse Width (Count)	4.0		5.0		4.0		ns
$t_W(L)$	HIGH or LOW	6.0		8.0		7.0		
$t_W(L)$	$\overline{MR}$ Pulse Width, LOW (74F160A)	5.0		5.0		5.0		
t_{REC}	Recovery Time $\overline{MR}$ to CP (74F160A)	6.0		6.0		6.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

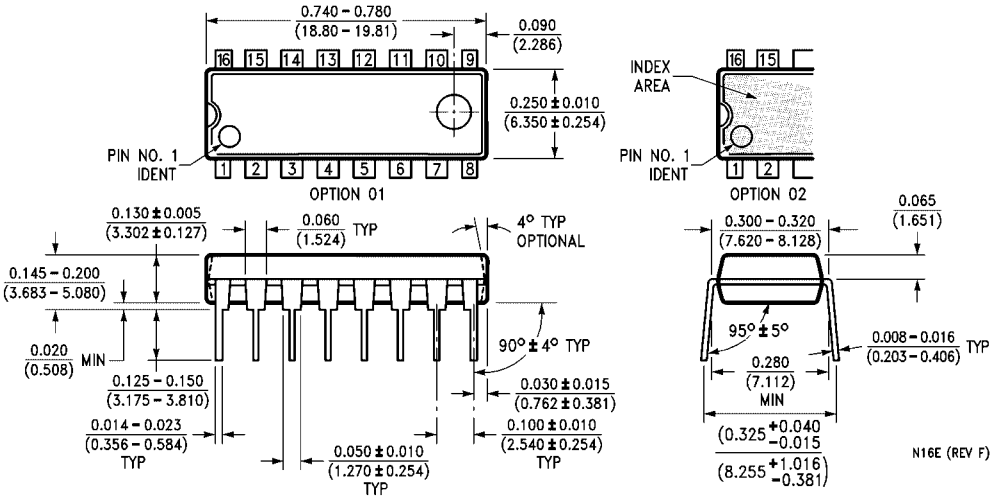
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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