Reset Circuits with Manual Reset Input

FEATURES

- Ultra-low supply current of 1µA (typ.)
- Guaranteed reset valid to Vcc=0.9V
- Available in two output yypes:
  - Push-pull active-low (SS811)
  - Push-pull active-high (SS812)
- Power-on reset pulse width minimum 140ms
- Internally fixed threshold 2.3V, 2.6V, 2.9V, 3.1V, 4.0V, 4.4V, and 4.6V
- Tight voltage threshold tolerance: 1.5%
- Low profile package: SOT-23-5

APPLICATIONS

- Notebook Computers
- Digital Still Cameras
- PDAs
- Critical Microprocessor Monitoring

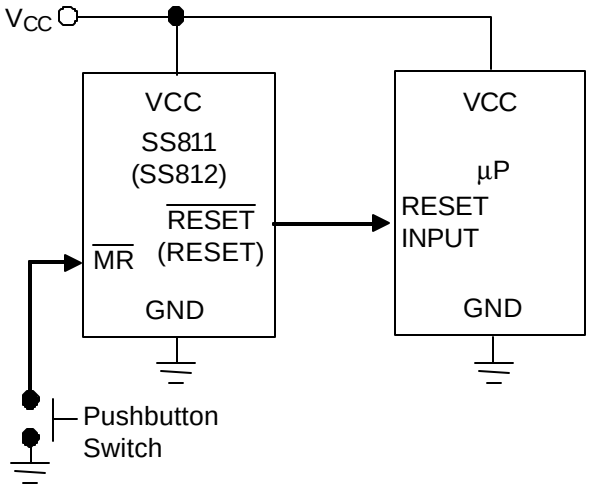
DESCRIPTION

The SS811 and SS812 are low-power microprocessor (µP) supervisory circuits used to monitor power supplies in µP and digital systems. They improve circuit reliability and reduce cost by eliminating external components. The SS811 and SS812 also offer a manual reset input.

These devices perform as valid singles in applications with Vcc ranging from 6.0V down to 0.9V. The reset signal lasts for a minimum period of 140ms whenever the V_{CC} supply voltage falls below a preset threshold. Both the SS811 and SS812 were designed with a reset comparator to help identify invalid signals lasting less than 140ms. The only difference between the SS811 and the SS812 is that one has an active-low $\overline{\text{RESET}}$ output and the other has an active-high RESET output.

A low supply current (1µA) makes the SS811 and SS812 ideal for portable equipment. The devices are available in a SOT-23-5 package.

TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION

SS811-XXCXXX
SS812-XXCXXX

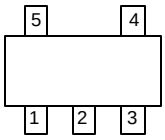
- Packing type
  TR: Tape and reel
- Package type
  V: SOT-23-5
- Reset Threshold Voltage
  23: 2.3V
  26: 2.6V
  29: 2.9V
  31: 3.1V
  40: 4.0V
  44: 4.4V
  46: 4.6V

(Additional voltage versions with a unit of 0.1V within the voltage range from 1.5V to 5.5V for this product line may be available on demand with prior consultation with SSC.)

Example: SS811-31CVTR
→ 3.1V version in SOT-23-5 package, shipped in tape and reel.

PIN CONFIGURATION

SOT-23-5
TOP VIEW
1: GND
2: NC
3: RESET (RESET)
4: MR
5: VCC



SOT-23-5 Marking

Part No.	Marking
SS811-23CV	BQ23
SS811-26CV	BQ26
SS811-29CV	BQ29
SS811-31CV	BQ31
SS811-40CV	BQ40
SS811-44CV	BQ44
SS811-46CV	BQ46

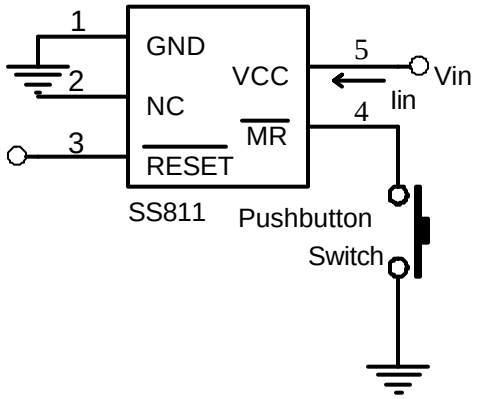
Part No.	Marking
SS812-23CV	BR23
SS812-26CV	BR26
SS812-29CV	BR29
SS812-31CV	BR31
SS812-40CV	BR40
SS812-44CV	BR44
SS812-46CV	BR46

ABSOLUTE MAXIMUM RATINGS

V_{CC}	-0.3V ~6.5V
RESET, $\overline{\text{RESET}}$	-0.3V ~ (VCC+0.3V)
Input Current (V_{CC}, $\overline{\text{MR}}$)	20mA
Output Current (RESET or $\overline{\text{RESET}}$)	20mA
Continuous Power Dissipation (T_A = +70°C)	320mW
Operating Junction Temperature Range	-40°C ~ 85°C
Storage Temperature Range	- 65°C ~ 150°C
Lead Temperature (Soldering) 10 sec	260°C

Note1: Any stress beyond the Absolute Maximum Ratings above may cause permanent damage to the device.

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

(Typical values are at T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Operating Voltage Range	V_{CC}			0.9		6	V
Supply Current	I_{CC}	V_{CC} = V_{TH} +0.1V			1	3	µA
Reset Threshold	V_{TH}	SS811-23	T_A=+25°C	2.265	2.3	2.335	V
			T_A= -40°C to +85°C	2.254		2.346	
		SS811-26	T_A=+25°C	2.561	2.6	2.639	
			T_A= -40°C to +85°C	2.548		2.652	
		SS811-29	T_A=+25°C	2.857	2.9	2.944	
			T_A= -40°C to +85°C	2.842		2.958	
		SS811-31	T_A=+25°C	3.054	3.1	3.147	
			T_A= -40°C to +85°C	3.038		3.162	
		SS811-40	T_A=+25°C	3.940	4.0	4.060	
			T_A= -40°C to +85°C	3.920		4.080	
		SS811-44	T_A=+25°C	4.334	4.4	4.466	
			T_A= -40°C to +85°C	4.312		4.488	
		SS811-46	T_A=+25°C	4.531	4.6	4.669	
			T_A=-40°C to +85°C	4.508		4.692	
V_{CC} to Reset Delay	T_{RD}	V_{CC}=V_{TH} to (V_{TH} –0.1V), V_{TH}=3.1V			20		µS
Reset Active Timeout Period	T_{RP}	V_{CC} = $V_{TH(MAX)}$	T_A=+25°C	140	230	560	mS
			T_A= -40°C to +85°C	100		1030	
$\overline{MR}$ to Reset Propagation Delay	T_{MD}	Vcc=6V			0.5		µS
$\overline{MR}$ Input Threshold	V_{IH}			0.7V_{CC}			V
	V_{IL}					0.25V_{CC}	
$\overline{MR}$ Pull-Up Resistance				10	20	30	KΩ
$\overline{RESET}$ Output Voltage	V_{OH}	V_{CC}=V_{TH}+0.1V, I_{SOURCE}=1mA		0.8V_{CC}			V
	V_{OL}	V_{CC}=V_{TH} - 0.1V, I_{SINK}=1mA				0.2Vcc	
RESET Output Voltage	V_{OH}	V_{CC}=V_{TH}+0.1V, I_{SOURCE}=1mA		0.8V_{CC}			V
	V_{OL}	V_{CC}=V_{TH} - 0.1V, I_{SINK}=1mA				0.2Vcc	

Note2: $\overline{RESET}$ output is for the SS811; RESET output is for the SS812.

Note3: Specifications for operating temperature ranges from -40°C to 85°C, are guaranteed by Statistical Quality Controls (SQC), with no production testing.

TYPICAL PERFORMANCE CHARACTERISTICS

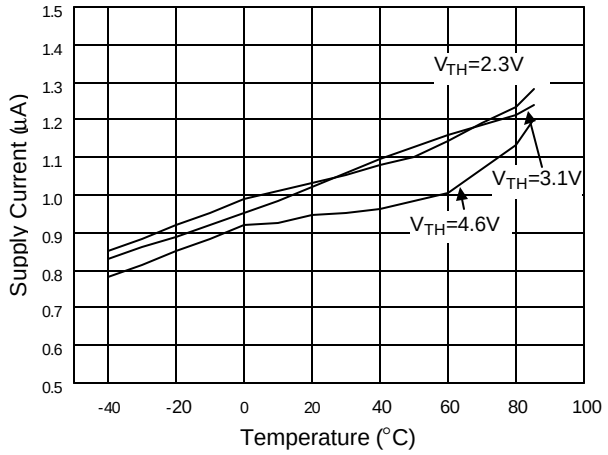


Fig 1 Supply Current vs. Temperature

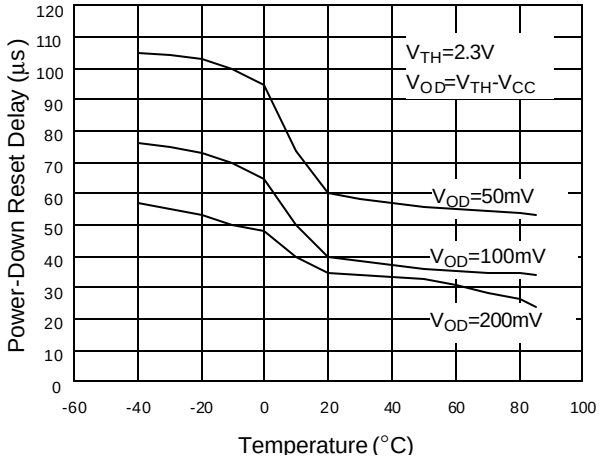


Fig 2 Power-Down Reset Delay vs. Temperature

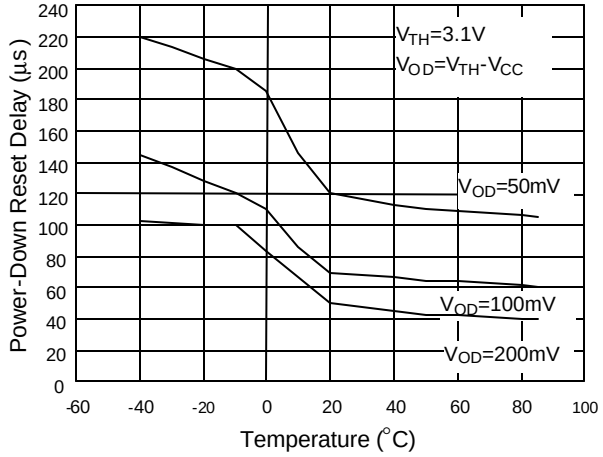


Fig 3 Power-Down Reset Delay vs. Temperature

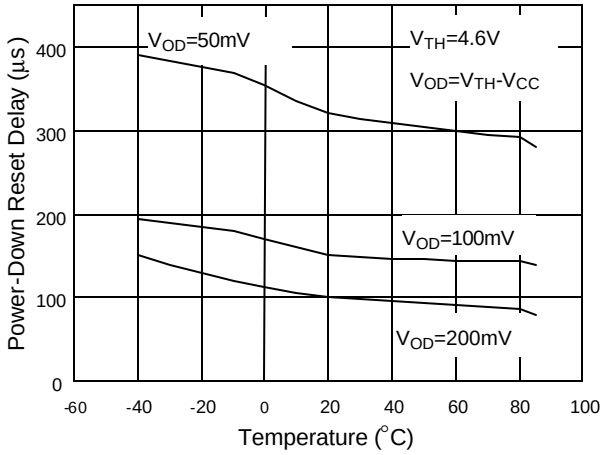


Fig 4 Power-Down Reset Delay vs. Temperature

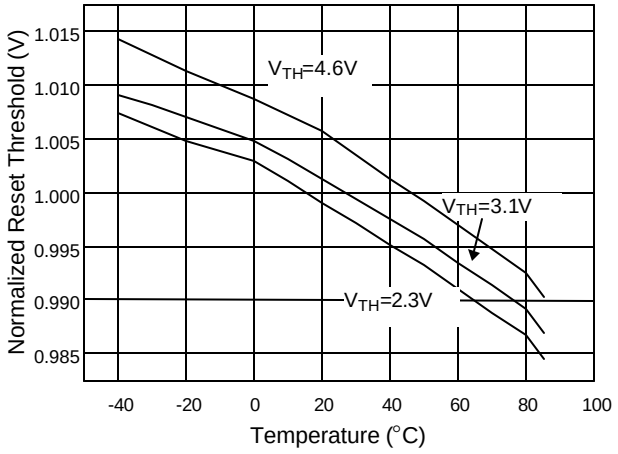


Fig 5 Normalized Reset Threshold vs. Temperature

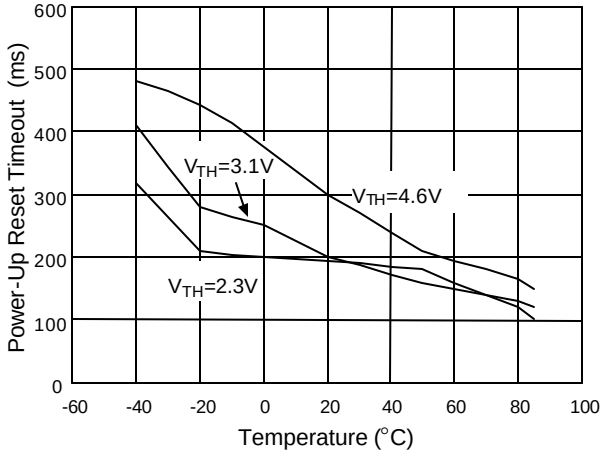
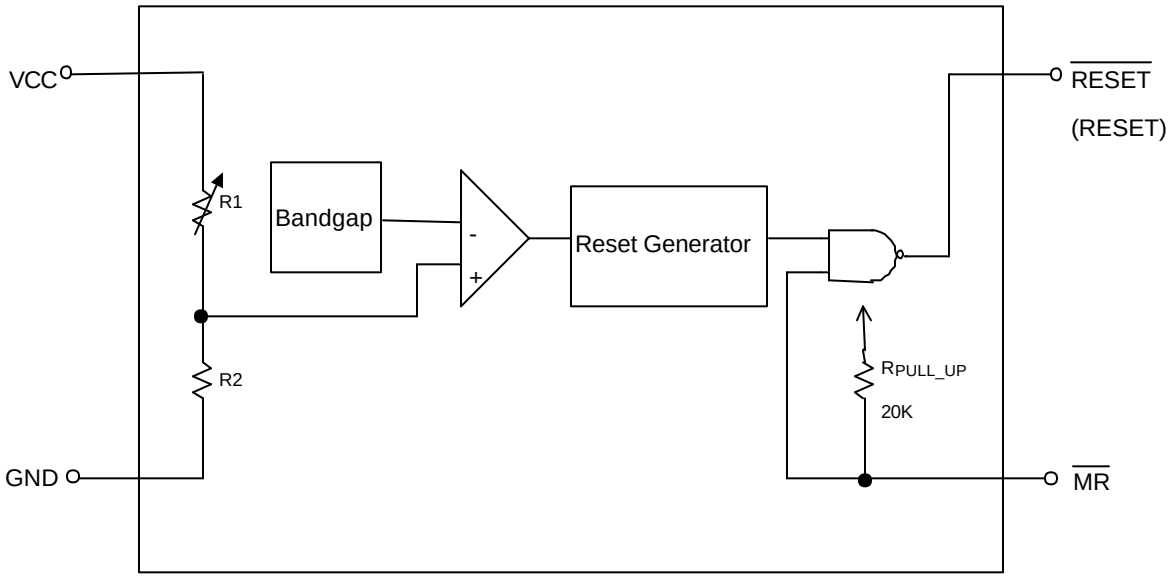


Fig 6 Power-Up Reset Timeout vs. Temperature

BLOCK DIAGRAM



PIN DESCRIPTIONS

GND Pin	:	Ground.
$\overline{\text{RESET}}$ Pin (SS811)	:	Active low output pin. $\overline{\text{RESET}}$ Output remains low while Vcc is below reset threshold.
RESET Pin (SS812)	:	Active high output pin. RESET output remains high while Vcc is below reset threshold.
$\overline{\text{MR}}$ Pin	:	Logic low manual reset input. This active-low input has an internal 20kΩ pull-up resistor. It can be driven by a TTL or CMOS, or shorted to ground with a switch. Leave open when unused.
Vcc Pin	:	Supply voltage.

DETAILED DESCRIPTIONS OF TECHNICAL TERMS

RESET OUTPUT

The microprocessor will be activated at a valid reset state. These µ P supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

$\overline{\text{RESET}}$ is guaranteed to be a logic low for V_{TH}>VCC>0.9V. Once VCC exceeds the reset threshold, an internal timer keeps $\overline{\text{RESET}}$ low for the reset timeout period; after this interval, $\overline{\text{RESET}}$ goes high.

If a brownout condition occurs (VCC drops below the reset threshold), $\overline{\text{RESET}}$ goes low. Any time VCC goes below the reset threshold, the internal timer resets to zero, and $\overline{\text{RESET}}$ goes low. The internal timer is activated after VCC returns above the reset threshold, and $\overline{\text{RESET}}$ remains low for the reset timeout period.

The manual reset input ($\overline{\text{MR}}$) can also initiate a reset. The SS812 has an active-high RESET output that is the inverse of the SS811's $\overline{\text{RESET}}$ output.

MANUAL RESET INPUT

Many microprocessor-based products require manual reset capability, allowing operators, test technicians, or external logic circuitry to initiate a reset. Logic low on $\overline{MR}$ asserts reset. Reset will remain asserted for the Reset Active Timeout Period (t_{RP}) after $\overline{MR}$ returns high. This input has an internal 20KΩ pull-up resistor, so it can be floating if it is not used. $\overline{MR}$ can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Another alternative is to connect a normal switch from $\overline{MR}$ to GND to create a manual reset function. Connecting a 0.1µF capacitor from $\overline{MR}$ to ground can provide noise immunity to prevent noise caused by long cables of $\overline{MR}$ or noisy environment.

BENEFITS OF HIGHLY ACCURATE RESET THRESHOLD

The SS811/812 with specified voltage as 5V±10% or 3V ±10% are ideal for systems using a 5V±5% or 3V±5% power supply. The reset is guaranteed to assert after the power supply falls out of regulation, but before power drops below the minimum specified operating voltage range of the system ICs. The pre-trimmed thresholds reduce the range over which an undesirable reset may occur.

APPLICATION INFORMATION

NEGATIVE-GOING VCC TRANSIENTS

In addition to issuing a reset to the microprocessor during power-up, power-down, and brownout conditions, the SS811 series are relatively resistant to short-duration negative-going VCC transient.

ENSURING A VALID RESET OUTPUT DOWN TO VCC=0

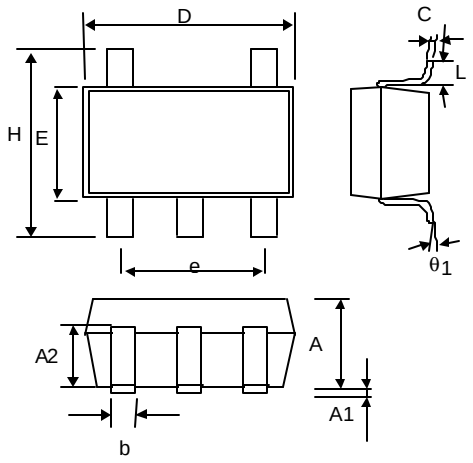
When VCC falls below 0.9V, the SS811 $\overline{RESET}$ output no longer sinks current; it becomes an open circuit. In this case, high-impedance CMOS logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. Therefore, the SS811/2 is perfect for most CMOS applications with VCC down to 0.9V. However in applications where $\overline{RESET}$ must be valid down to 0V, adding a pull-down resistor to $\overline{RESET}$ causes any leakage currents to flow to ground, holding $\overline{RESET}$ low.

INTERFACING TO MICROPROCESSORS WITH BIDIRECTIONAL RESET PINS

Microprocessors with bidirectional reset pins may have contention with the SS811/812 reset outputs. If the SS811 $\overline{RESET}$ output is asserted high and the microprocessor wants to pull it low, indeterminate logic levels may occur. To correct such cases, connect a resistor between the SS811 $\overline{RESET}$ (or SS812 RESET) output and the microprocessor reset I/O. Buffer the reset output to other system components.

PHYSICAL DIMENSIONS

SOT-23-5 (unit: mm)



SYMBOL	MIN	MAX
A	1.00	1.30
A1	—	0.10
A2	0.70	0.90
b	0.35	0.50
C	0.10	0.25
D	2.70	3.10
E	1.40	1.80
e	1.90 (TYP)	
H	2.60	3.00
L	0.37	—
θ1	1°	9°