

Microprocessor Voltage Monitor with Manual Reset

Features

Precision monitoring of +3V, +3.3V, and +5V power-supply voltages
Fully specified over temperature
Available in two output configurations

Push-pull RESET output (SS8039L) Push-pull RESET output (SS8039H)

Manual reset input

Power-on reset pulse width of 140ms min Supply current of 5µA Guaranteed reset valid to V_{CC} = +1V Power supply transient immunity No external components 4-Pin SOT-143 package

Applications

Computers
Controllers
Intelligent instruments
Critical µP and µC power monitoring
Portable / battery-powered equipment
Automotive

Compatible with the popular "811" series

General Description

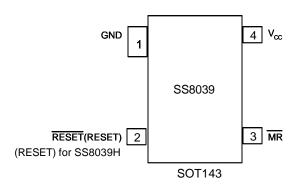
The SS8039 is a microprocessor (μ P) supervisory circuit used to monitor the power supplies in μ P and digital systems. It provides excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5V, +3.3V, +3.0V- powered circuits.

These circuits perform a single function: they assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. Reset thresholds suitable for operation with a variety of supply voltages are available.

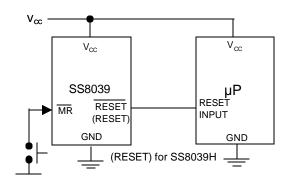
The SS8039 has a push-pull output stage. The SS8039L has an active-low $\overline{\text{RESET}}$ output, while the SS8039H has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC}, and the outputs are guaranteed to be in the correct logic state for V_{CC} down to 1V.

Low supply current makes the SS8039 ideal for use in portable equipment, and it is available in a 4-pin SOT-143 package.

Pin Configuration



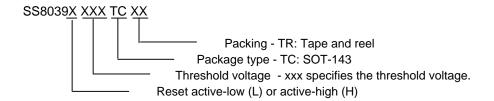
Typical Application





Ordering Information

Options are released to production as needed. Please check with Silicon Standard for availability.



Example: SS8039H263TCTR

SS8039 with push-pull active-high reset output at 2.63V in SOT-143 package supplied on tape and reel

Absolute Maximum Ratings

Terminal voltages with respect to GND	
V _{CC} 0.3V to +6.0V	Continuous Power Dissipation ($T_A = +70$ °C)
RESET, $\overline{\text{RESET}}$ (push-pull)0.3V to (V _{CC} + 0.3V	SOT-143 (derate 4mW/°C above +70°C)320mW
Input Current, V _{CC}	Operating Temperature Range40°C to +105°C Storage Temperature Range65°C to +150°C
	Lead Temperature (soldering 10s) +300°C

Electrical Characteristics

 $(V_{CC} = \text{full range}, T_A = -40^{\circ}\text{C} \text{ to } +105^{\circ}\text{C}, \text{ unless otherwise noted}. \text{ Typical values are at } T_A = +25^{\circ}\text{C}, V_{CC} = 5\text{V for } 463/438/400 \text{ versions}, V_{CC} = 3.3\text{V for } 308/293 \text{ versions}, \text{ and } V_{CC} = 3\text{V for } 263 \text{ version.})$ (Note 1)

PARAMETER	SYMBOL	CONDITION			ТҮР	MAX	UNITS
V Dongo		$T_A = 0^{\circ}C + 70^{\circ}C$		1.0		5.5	\/
V _{CC} Range		T _A = -40°C +105°C		1.2		5.5	V
Supply Current		$T_A = -40^{\circ}\text{C} + 105^{\circ}\text{C}$	V _{CC} <5.5V, SS8039x463/438/400		5.5	9	μA
	l _{CC}		V _{CC} <3.6V, SS8039x308/293/263		5	8	
		SS8039x463	T _A = +25°C	4.537	4.63	4.722	V
		SS8039x438	T _A = +25°C	4.292	4.38	4.467	
Reset Threshold		SS8039x400	T _A = +25°C	3.92	4.00	4.08	
	V_{TH}	SS8039x308	$T_A = +25$ °C	3.018	3.08	3.141	
		SS8039x293	$T_A = +25$ °C	2.871	2.93	2.988	
		SS8039x263	T _A = +25°C	2.577	2.63	2.682	



Electrical Characteristics (Continued)

(V_{CC} = full range, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = 5V for 463/438/400 versions, V_{CC} = 3.3V for 308/293 versions, and V_{CC} = 3V for 263 version.) (Note 1)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	
Reset Threshold Tempco				70		ppm/°C	
V _{CC} to Reset Delay (Note 2)		$V_{CC} = V_{TH}$ to $(V_{TH} - 100$ mV)		15			
Reset Active Timeout Period		V _{CC} = V _{TH} max, SS8039x463/438/400	250	510	720	ms	
		V _{CC} = V _{TH} max, SS8039x308/293/263	140	310	520		
MR Minimum Pulse Width	t _{MR}			10		μs	
MR Glitch Immunity (Note 3)				100		ns	
MR to Reset Propagation Delay (Note 2)	t _{MD}			0.5		μs	
MR Input Threshold	V _{IH}	$V_{CC} > V_{TH(max)}$	0.6 x V _∞		0.25 x V _∞	V	
MR Pull-up Resistance			10	20	30	ΚΩ	
RESET Output Current Low (push-pull active low ,SS8039L	la	V _{CC} = 2.5V, V RESET = 0.5V	8			mA	
RESET Output Current High (push-pull active low, SS8039L)	Юн	$V_{CC} = 5V$, $V_{RESET} = 4.5V$, SS8039L463/438/400 $V_{CC} = 3.3V$, $V_{RESET} = 2.8V$, SS8039L308/293 $V_{CC} = 3V$, $V_{RESET} = 2.5V$, SS8039L263	4.5 3 2			mA	
RESET Output Current Low (push-pull active high, SS8039H)	la	$V_{CC} = 5V$, $V_{RESET} = 0.5V$, SS8039H463/438/400 $V_{CC} = 3.3V$, $V_{RESET} = 0.5V$, SS8039H308/293 $V_{CC} = 3V$, $V_{RESET} = 0.5V$, SS8039H263	16 12 10			mA	
RESET Output Current High (push-pull active high, SS8039H)	l _{он}	$V_{CC} = 2.5V$, $V_{RESET} = 2V$	2			mA	

- Note 1: Production testing done at $T_A = +25$ °C; limits over temperature guaranteed by design.
- Note 2: RESET output is for SS8039L; RESET output is for SS8039H.
- Note 3: "Glitches" of 100ns or less typically will not generate a reset pulse.

Selection Guide and Part Marking

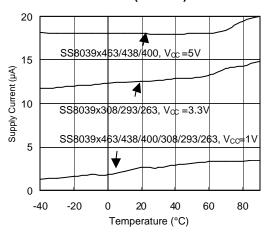
PART/SUFFIX	RESET THRESHOLD (V)	OUTPUT TYPE	TOP MARK
SS8039H463TC	4.63	Push-Pull RESET	692Lx
SS8039H438TC	4.38	Push-Pull RESET	692Kx
SS8039H400TC	4.00	Push-Pull RESET	692Jx
SS8039H308TC	3.08	Push-Pull RESET	692lx
SS8039H293TC	2.93	Push-Pull RESET	692Hx
SS8039H263TC	2.63	Push-Pull RESET	692Gx
SS8039L463TC	4.63	Push-Pull RESET	692Fx
SS8039L438TC	4.38	Push-Pull RESET	692Ex
SS8039L400TC	4.00	Push-Pull RESET	692Dx
SS8039L308TC	3.08	Push-Pull RESET	692Cx
SS8039L293TC	2.93	Push-Pull RESET	692Bx
SS8039L263TC	2.63	Push-Pull RESET	692Ax



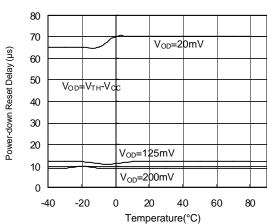
Typical Operating Characteristics

 $(V_{CC} = \text{full range}, T_A = -40^{\circ}\text{C} \text{ to } +105^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $T_A = +25^{\circ}\text{C}, V_{CC} = 5\text{V}$ for 463/438/400 versions, $V_{CC} = 3.3\text{V}$ for 308/293 versions, and $V_{CC} = 3.7\text{V}$ for 263 version.)

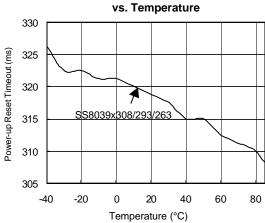
Supply Current vs.Temperature (No Load)



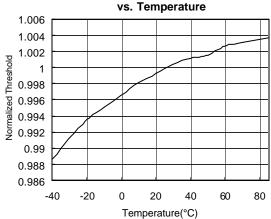
Power-down Reset Delay vs. Temperature (\$\$8039x308/293/263)



Power-up Reset Timeout



Normalized Reset Threshold





Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	RESET (SS8039L)	RESET Output remains low while V_{CC} is below the reset threshold, and for at least 140ms after V_{CC} rises above the reset threshold.
_	RESET (SS8039H)	RESET Output remains high while V_{CC} is below the reset threshold, and for at least 140ms after V_{CC} rises above the reset threshold.
3	MR	Manual Reset Input. A logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted as long as $\overline{\text{MR}}$ is low and for at least 140ms after $\overline{\text{MR}}$ returns high, This active-low input has an internal 20k Ω pull- up resistor. It can be driven from a TTL or CMOS-logic line, or shorted to ground with a switch. Leave open if unused.
4	V _{cc}	Supply Voltage (+5V, +3.3V, +3.0V)

Detailed Description

A microprocessor's (μ P's) reset input starts the μ P in a known state. The SS8039L and SS8039H assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions. They assert a reset signal whenever the $V_{\rm CC}$ supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after $V_{\rm CC}$ has risen above the reset threshold.

The SS8039L/SS8039H <u>have</u> a push-pull output stage. The manual reset input (MR) can also initiate a reset. See the Manual Reset Input Section.

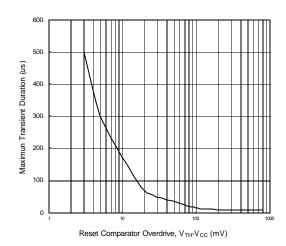


Fig.1 Maximum Transient Duration Without Causing a Reset Pulse vs. Reset Comparator Overdrive

Manual Reset Input

Many μP -based products require manual reset capability allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on \overline{MR} asserts reset. Reset remains asserted while \overline{MR} is low, and for the Reset Active Timeout Period (t_{RP}) after \overline{MR} returns high. This input has an internal $20k\Omega$ pull-up resistor, so it can be left open if it is not used. \overline{MR} can be driven with TTL or CMOS-logic levels, or with open-drain / collector outputs. Connect a normally open momentary switch from \overline{MR} to GND to create a manual-reset function; external debounce circuitry is not required. If \overline{MR} is driven from long cables or if the device is used in a noisy environment, connecting a $0.1\mu F$ capacitor from \overline{MR} to ground provides additional noise immunity.

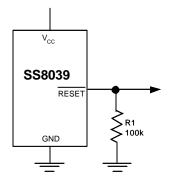


Figure 2. RESET Valid to V_{cc} = Ground Circuit



Applications Information

Negative-Going V_{CC} Transients

In addition to issuing a reset to the μP during power-up, power-down, and brownout conditions, the SS8039H and SS8039L are relatively immune to short-duration negative-going $V_{\rm CC}$ transients (glitches).

Figure1 shows typical transient durations, vs. the reset comparator overdrive, for which both the SS8039H and SS8039L do not generate a reset pulse. The graph was generated using a negative-going pulse applied to V_{CC} , starting 0.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width a negative-going V_{cc} transient can have without causing a reset pulse. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. For the SS8039x463 and SS8039x438, a V_{CC} transient that goes 100mV below the reset threshold and lasts 15µs or less will not typically cause a reset pulse. A 0.1µF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

Ensuring a Valid Reset Output Down to Vcc = 0

When $V_{\rm CC}$ falls below 1V, the SS8039 RESET output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to RESET can drift to undetermined voltages. This presents no problem in most applications since most μP and other circuitry is inoperative with VCC below 1V. However, in applications where RESET must be valid down to 0V, adding a pull-down resistor to RESET causes any stray leakage currents to flow to ground, holding RESET low (Figure 2). R1's value is not critical; $100 \text{k}\Omega$ is large enough not to load RESET and small enough to pull RESET to ground.

Benefits of Highly Accurate Reset Threshold

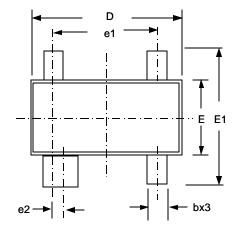
Most μP supervisor ICs have reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when the supply is 10% below nominal.

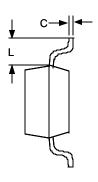
When using ICs rated at only the nominal supply $\pm 5\%$, this leaves a zone of uncertainty where the supply is between 5% and 10% low, and where the reset may or may not be asserted.

The SS8039x uses highly accurate circuitry to ensure that reset is asserted close to the 5% limit, and long before the supply has declined to 10% below nominal.

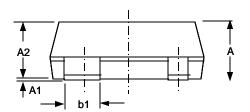


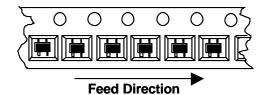
Physical Dimensions





Package Orientation





SOT 143 Package

SYMBOL	DIMENSION	IN MILIMETERS	DIMENSION IN INCHS		
STWIBOL	MIN.	MAX.	MIN.	MAX.	
Α	0.95	1.20	0.037	0.047	
A1	0.05	0.10	0.002	0.004	
A2	0.90	1.10	0.035	0.043	
b	0.37	0.46	0.145	0.018	
b1	0.76	0.89	0.030	0.035	
С	0.10	0.18	0.004	0.007	
D	2.80	3.04	0.110	0.120	
E	1.20	1.40	0.047	0.055	
E1	2.30	2.50	0.091	0.098	
e1	1.9	92 BSC.	0.75 BSC.		
e2	0.2	20 BSC.	0.078 BSC.		
L	0.	69 REF.	0.27 REF.		

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