

SM5610

IC for Quartz Crystal Oscillating
Module

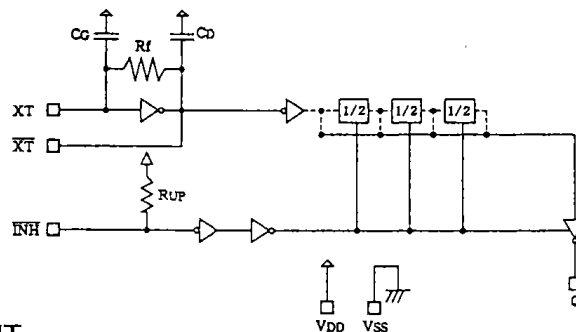
OVERVIEW

SM5610 series are C-MOS ICs for quartz crystal oscillating module. Each IC has a high frequency oscillating circuit and dividers with low current consumption.
 Many kinds of type, capacitor for oscillation on chip or not, output frequency: f_0 (fundamental), $f_0/2$, $f_0/4$, or $f_0/8$, and I/O level TTL or CMOS (Refer to the SERIES TABLE).

FEATURES

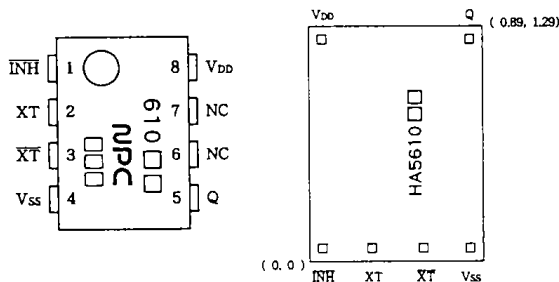
- Operating voltage (4V - 6V)
- On-chip in feed back resistance of oscillation circuit
- Gate function
- Low current consumption
- Chip form, 8-pin SOP
- Niobium gate C-MOS
- Fundamental wave use

■ BLOCK DIAGRAM



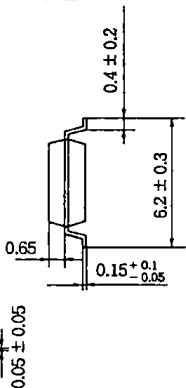
■ PIN OUT

• 8-pin SOP (TOP VIEW)

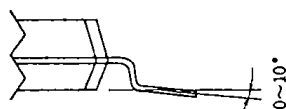


CHIP SIZE: 0.89 × 1.29mm
 CHIP THICKNESS: 400 ± 30 μm

PACKAGE DIMENSION



COORDINATES



SM5610

Frequency	Output duty level	Output current
	TTL	16mA
2	TTL	16mA
4	TTL	16mA
8	TTL	16mA
	CMOS	4mA
2	CMOS	4mA
4	CMOS	4mA
8	CMOS	4mA
	CMOS	16mA
2	CMOS	16mA
4	CMOS	16mA
8	CMOS	16mA

SOP package is named SM5610 □ □ S.

MAXIMUM RATING ($V_{SS}=0V$)

PARAMETER	CONDITIONS	UNIT
V_{DD}	-0.5 to +7.0	V
V_{IN}	-0.5 to $V_{DD}+0.5$	V
V_{OUT}	-0.5 to $V_{DD}+0.5$	V
T_{STG1}	-65 to +150 (chip)	°C
T_{STG2}	-40 to +125 (SOP)	
I_{OUT}	N, K series 25 H series 10	mA
P_W	200	mW
T_{SLD}	255	°C
t_{SLD}	10	S

Note: * mark is useful at SOP package

SM5610

TERISTICS

(V_{SS}=0V, T_a=-40 to 85°C, unless otherwise noted)

CONDITIONS			LIMITS			UNIT
			MIN	TYP	MAX	
SM5610K, N	Q pin, Fig. 1	V _{DD} =4.5V, I _{OH} =16.0mA	3.9	4.2		V
		V _{DD} =4.0V, I _{OH} =14.4mA	3.4	3.7		
SM5610H		V _{DD} =4.5V, I _{OL} =4.0mA	3.9	4.2		
		V _{DD} =4.0V, I _{OL} =3.6mA	3.4	3.7		
SM5610K, N	Q pin, Fig. 1	V _{DD} =4.5V, I _{OH} =16.0mA		0.3	0.4	V
		V _{DD} =4.0V, I _{OH} =14.4mA		0.3	0.4	
SM5610H		V _{DD} =4.5V, I _{OL} =4.0mA		0.3	0.5	
		V _{DD} =4.0V, I _{OL} =3.6mA		0.3	0.5	
Q pin, Fig. 1, I _{NH} ="L", V _{DD} =6.0V		V _{OH} =V _{DD}			10	μA
		V _{OL} =V _{SS}			10	
I _{NH} pin		V _{DD} =5±0.5V	2.0			V
		V _{DD} =5±1.0V	2.2			
I _{NH} pin		V _{DD} =5±1.0V			0.8	V
Load circuit 1 (SM5610N, H)		V _{DD} =5V, T _a =25°C		15	20	mA
Load circuit 2 (SM5610K), Fig. 2, I _{NH} =OPEN, C _L =15pF		V _{DD} =5.5V			30	
		V _{DD} =6.0V			35	
Load circuit 1 (SM5610N, H)		V _{DD} =5V, T _a =25°C		21	26	
Load circuit 2 (SM5610K), Fig. 2, I _{NH} =OPEN, C _L =50pF		V _{DD} =5.5V			36	
		V _{DD} =6.0V			41	
Fig. 3			50		250	kΩ
Fig. 4		V _{DD} =5±0.5V	1.0		5.0	MΩ
		V _{DD} =5±1.0V	0.9		5.5	
Design value			19	27	35	pF
			19	27	35	

TERISTICS

V_{SS} = 0V, T_a = -40 to +85°C unless otherwise noted.

OL	CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
	Load circuit 2, Fig. 2, C _L =15pF, V _{DD} =5±0.5V		1.5	3.0	ns

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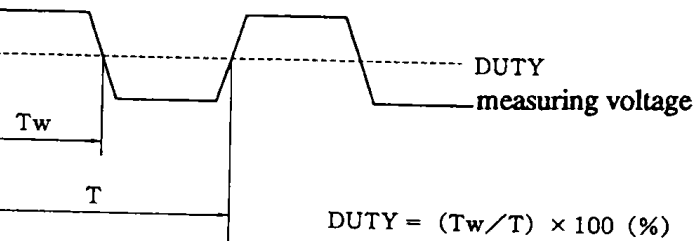
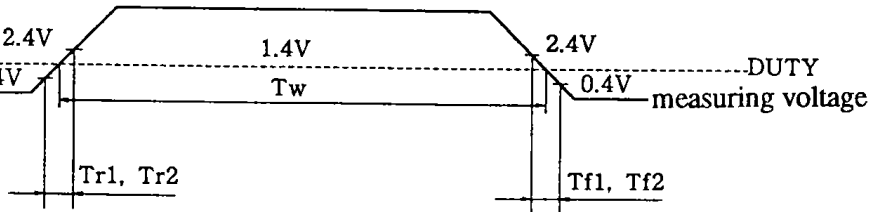
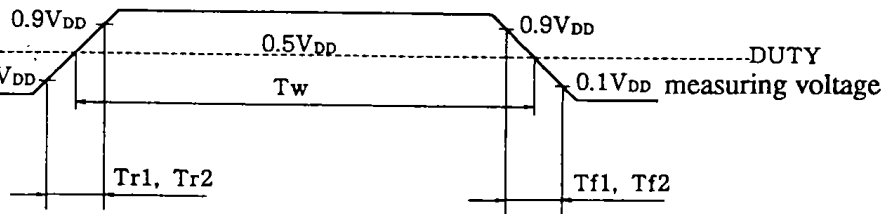
V_{SS} = 0V, T_a = -40 to +85°C unless otherwise noted.

SYMBOL	CONDITIONS			LIMITS			UNIT
				MIN	TYP	MAX	
T _{ri}	Load circuit 1, Fig. 2 0.1V _{DD} to 0.9V _{DD}	C _L =15pF	V _{DD} =5±0.5V	5.0	10	ns	
			V _{DD} =5±1.0V		12		
T _{r2}		C _L =50pF	V _{DD} =5±0.5V	13	26		
			V _{DD} =5±1.0V		30		
T _{fi}	Load circuit 1, Fig. 2 0.9V _{DD} to 0.1V _{DD}	C _L =15pF	V _{DD} =5±0.5V	5.0	10	ns	
			V _{DD} =5±1.0V		12		
T _{f2}		C _L =50pF	V _{DD} =5±0.5V	13	26		
			V _{DD} =5±1.0V		30		
DUTY	Load circuit 1, Fig. 2, C _L =15pF, T _a =25°C, V _{DD} =5.0V			45		55	%
T _{PLZ}	Fig. 2, T _a =25°C, V _{DD} =5±1.0V, Load C _L ≤50pF					100	ns
T _{PZL}						100	
f _{MAX}	Load circuit 1, Fig. 2, V _{DD} =5±1.0V			30			MHz

V_{SS} = 0V, T_a = -40 to +85°C unless otherwise noted.

SYMBOL	CONDITIONS			LIMITS			UNIT
				MIN	TYP	MAX	
T _{ri}	Load circuit 1, Fig. 2 0.1V _{DD} to 0.9V _{DD}	C _L =15pF	V _{DD} =5±0.5V		1.5	3.0	ns
			V _{DD} =5±1.0V			3.5	
T _{r2}		C _L =50pF	V _{DD} =5±0.5V		3.0	6.0	
			V _{DD} =5±1.0V			7.0	
T _{fi}	Load circuit 1, Fig. 2 0.9V _{DD} to 0.1V _{DD}	C _L =15pF	V _{DD} =5±0.5V		1.5	3.0	ns
			V _{DD} =5±1.0V			3.5	
T _{f2}		C _L =50pF	V _{DD} =5±0.5V		3.0	6.0	
			V _{DD} =5±1.0V			7.0	
DUTY	Load circuit 1, Fig. 2, C _L =50pF, T _a =25°C, V _{DD} =5.0V			45		55	%
T _{PLZ}	Fig. 2, T _a =25°C, V _{DD} =5±1.0V, Load C _L ≤50pF					100	ns
T _{PZL}						100	
f _{MAX}	Load circuit 1, Fig. 2, C _L =50pF, V _{DD} =5±1.0V			30			MHz

SWITCHING TIME



SM5610

terminal
Q
$f_0/2; f_0/4$ or $f_0/8$)
balance

frequency