Document Title

16M x 8 Bit NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial issue.	May 28'th 2001	Advance
0.1	K9F2808U0B(3.3V device)'s qualification is finished	Jun. 30th 2001	
0.2	K9F2808Q0B (1.8V device) - Changed typical read operation current (Icc1) from 8mA to 5mA - Changed typical program operation current (Icc2) from 8mA to 5mA - Changed typical erase operation current (Icc3) from 8mA to 5mA - Changed typical program time(tPROG) from 200us to 300us - Changed ALE to $\overline{RE}$ Delay (ID read, tAR1) from 100ns to 20ns - Changed CLE hold time(tCLH) from 10ns to 15ns - Changed $\overline{CE}$ hold time(tCH) from 10ns to 15ns - Changed ALE hold time(tALH) from 10ns to 15ns - Changed Data hold time(tDH) from 10ns to 15ns - Changed $\overline{CE}$ Access time(tCEA) from 45ns to 60ns - Changed Read cycle time(tRC) from 50ns to 70ns - Changed Write Cycle time(tWC) from 50ns to 70ns - Changed $\overline{RE}$ Access time(tREA) from 35ns to 40ns - Changed $\overline{RE}$ High Hold time(tREH) from 15ns to 20ns - Changed $\overline{WE}$ High Hold time(tWH) from 15ns to 20ns	Jul. 30th 2001	K9F2808Q0B : Preliminary
0.3	1. Device Code is changed - TBGA package information : 'B' --> 'D' ex) K9F2808Q0B-BCB0 ,BIB0 --> K9F2808Q0B-DCB0,DIB0 K9F2808U0B-BCB0 ,BIB0 --> K9F2808Q0B-DCB0,DIB0 2. V_{IH} ,V_{IL} of K9F2808Q0B(1.8 device) is changed	Aug. 23th 2001	

(before revision)

Input High Voltage	V_{IH}	I/O pins	VccQ-0.4		VccQ
		Except I/O pins	V_{CC}-0.4	-	VCC
Input Low Voltage, All inputs	V_{IL}	-	0	-	0.4

(after revision)

Input High Voltage	V_{IH}	I/O pins	VccQ-0.4		VccQ +0.3
		Except I/O pins	V_{CC}-0.4	-	VCC +0.3
Input Low Voltage, All inputs	V_{IL}	-	-0.3	-	0.4

Note : For more detailed features and specifications including FAQ, please refer to Samsung's Flash web site.
http://www.intl.samsungsemi.com/Memory/Flash/datasheets.html

Revision History

Revision No.	History	Draft Date	Remark
0.4	1. I_{OL}($R/\overline{B}$) of 1.8V device is changed. -min. Value: 7mA -->3mA -typ. Value: 8mA -->4mA 2. AC parameter is changed. tRP(min.) : 30ns --> 25ns	Nov 5th 2001	Preliminary
0.5	1. Parameters are changed in 1.8V part(K9F2808Q0B) . - tCH is changed from 15ns to 20ns - tCLH is changed from 15ns to 20ns - tALH is changed from 15ns to 20ns - tDH is changed from 15ns to 20ns	Feb 15th 2002	
0.6	1. Parameters are changed in 1.8V part(K9F2808Q0B) . - tRP is changed from 25ns to 35ns - tWB is changed from 100ns to 150ns - tREA is changed from 40ns to 45ns	May 3rd 2002	

Note : For more detailed features and specifications including FAQ, please refer to Samsung's Flash web site.
http://www.intl.samsungsemi.com/Memory/Flash/datasheets.html

16M x 8 Bit Bit NAND Flash Memory

PRODUCT LIST

Part Number	Vcc Range	Organization	PKG Type
K9F2808Q0B-D	1.7 ~ 1.9V	X8	TBGA
K9F2808U0B-Y	2.7 ~ 3.6V		TSOP1
K9F2808U0B-D			TBGA
K9F2808U0B-V			WSOP1

FEATURES

- Voltage Supply
  - K9F2808Q0B : 1.7~1.9V
  - K9F2808U0B : 2.7 ~ 3.6 V
- Organization
  - Memory Cell Array : (16M + 512K)bit x 8bit
  - Data Register : (512 + 16)bit x8bit
- Automatic Program and Erase
  - Page Program : (512 + 16)Byte
  - Block Erase : (16K + 512)Byte
- 528-Byte Page Read Operation
  - Random Access : 10µs(Max.)
  - Serial Page Access
    - K9F2808Q0B : 70ns
    - K9F2808U0B : 50ns
- Fast Write Cycle Time
  - Program Time
    - K9F2808Q0B : 300µs(Typ.)
    - K9F2808U0B : 200µs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Package
  - K9F2808U0B-YCB0/YIB0 :
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9F2808X0B-DCB0/DIB0
    63- Ball TBGA (9 x 11 /0.8mm pitch , Width 1.0 mm)
  - K9F2808U0B-VCB0/VIB0
    48 - Pin WSOP I (12X17X0.7mm)
    * K9F2808U0B-V(WSOPI) is the same device as K9F2808U0B-Y(TSOP1) except package type.

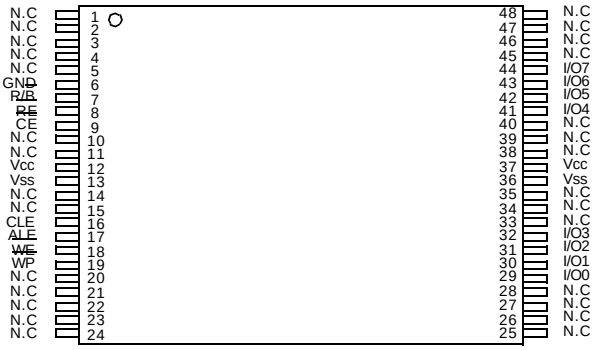
GENERAL DESCRIPTION

The K9F2808X0B is a 16M(16,777,216)x8bit NAND Flash Memory with a spare 512K(524,288)x8bit. The device is offered in 1.8V or 3.3V Vcc. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation programs the 528-byte page in typical 200µs and an erase operation can be performed in typical 2ms on a 16K-byte block. Data in a page can be read out at 70ns/50ns(K9F2808Q0B:70ns, K9F2808U0B:50ns) cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even write-intensive systems can take advantage of the K9F2808X0B's extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.

The K9F2808X0B is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption.

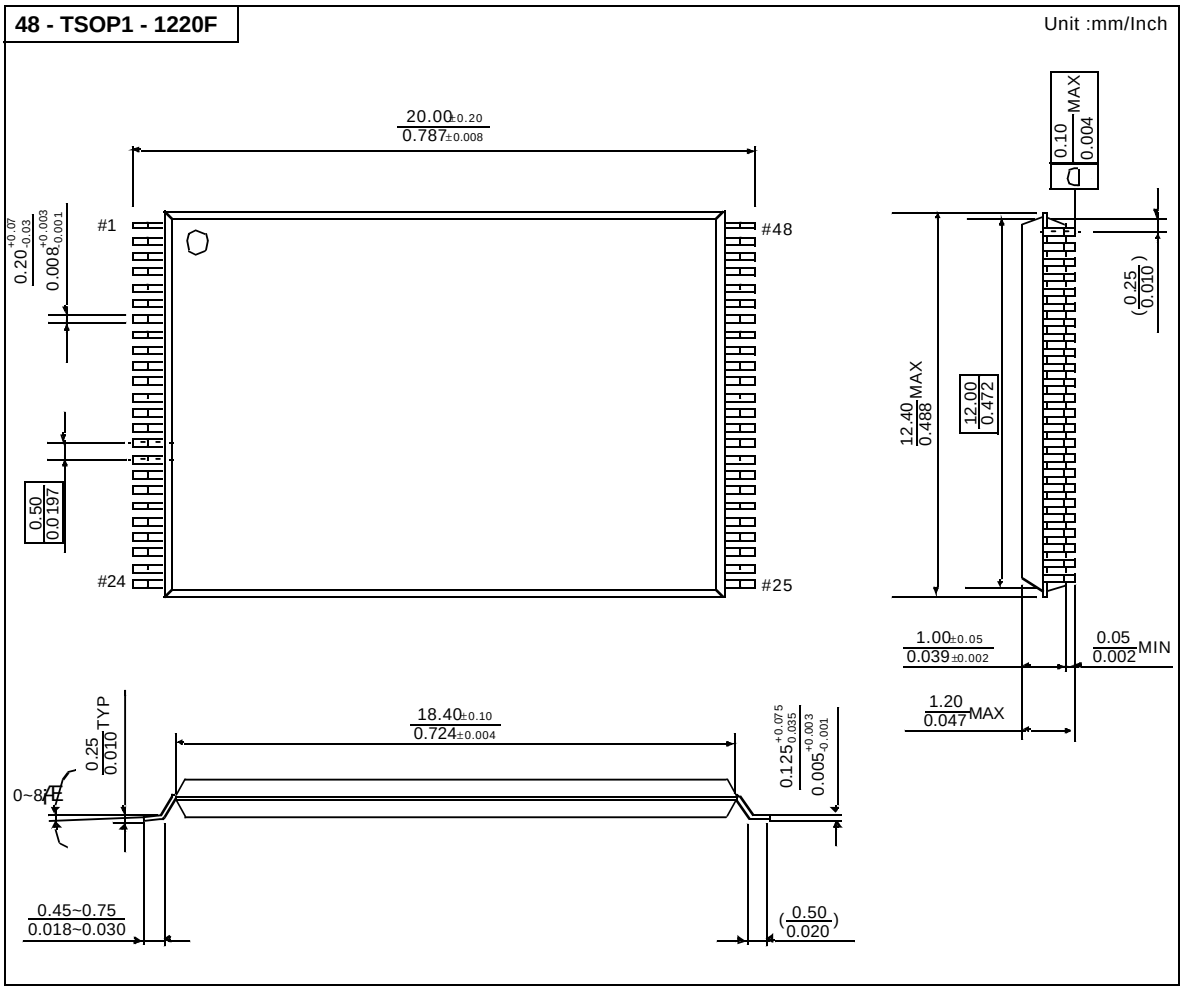
PIN CONFIGURATION (TSOP1)

K9F2808U0B-YCB0/YIB0



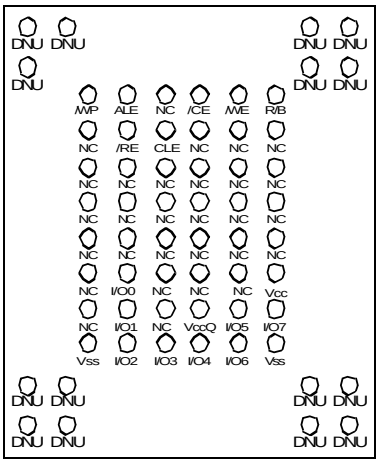
PACKAGE DIMENSIONS

48-PIN LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)



PIN CONFIGURATION (TBGA)

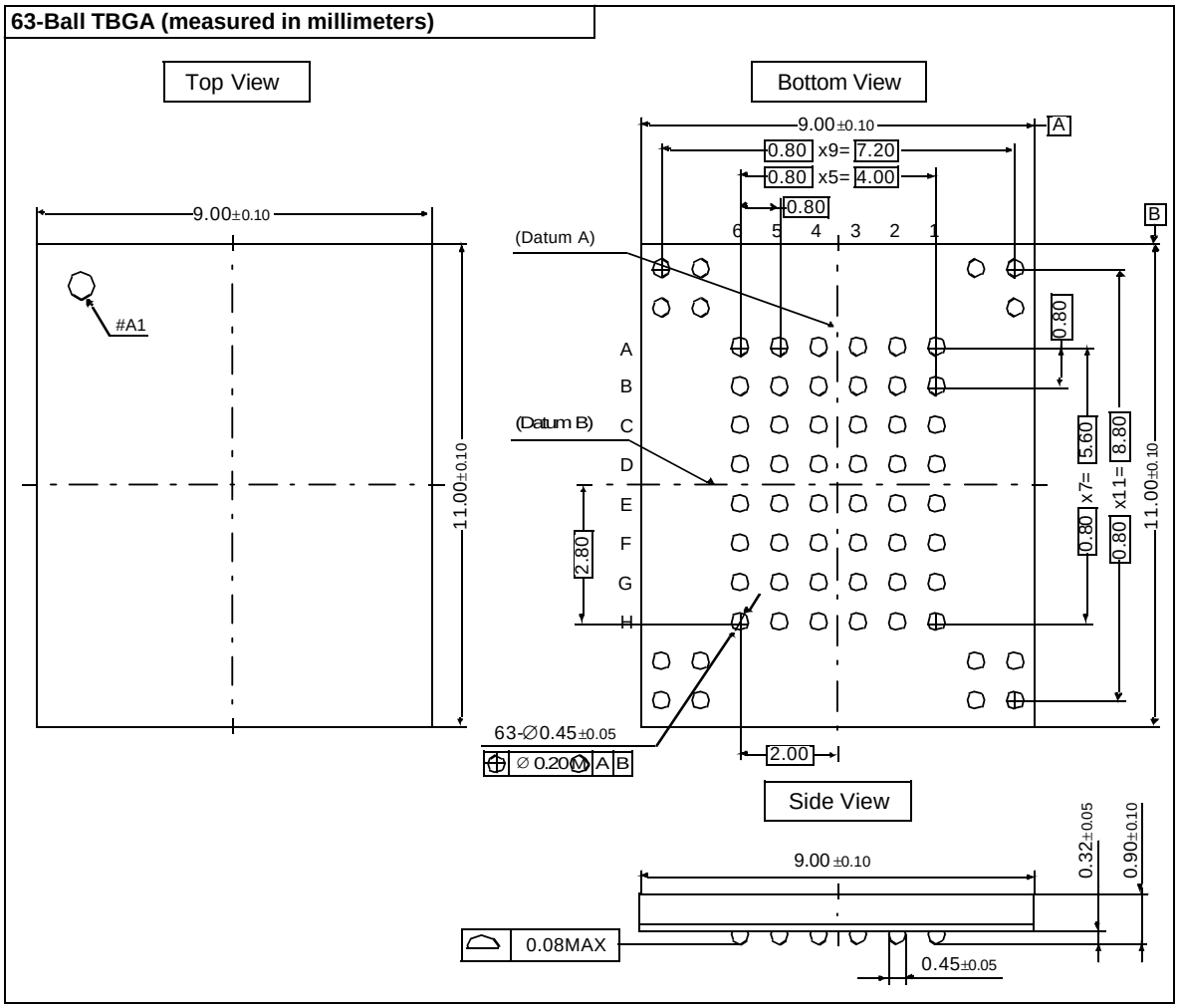
K9F2808X0B-DCB0/DIB0



(Top View)

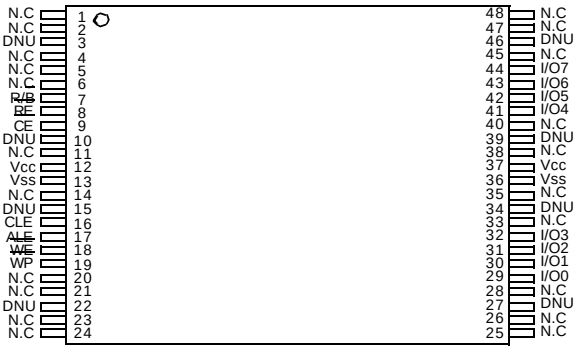
PACKAGE DIMENSIONS

63-Ball TBGA (measured in millimeters)



PIN CONFIGURATION (WSOP1)

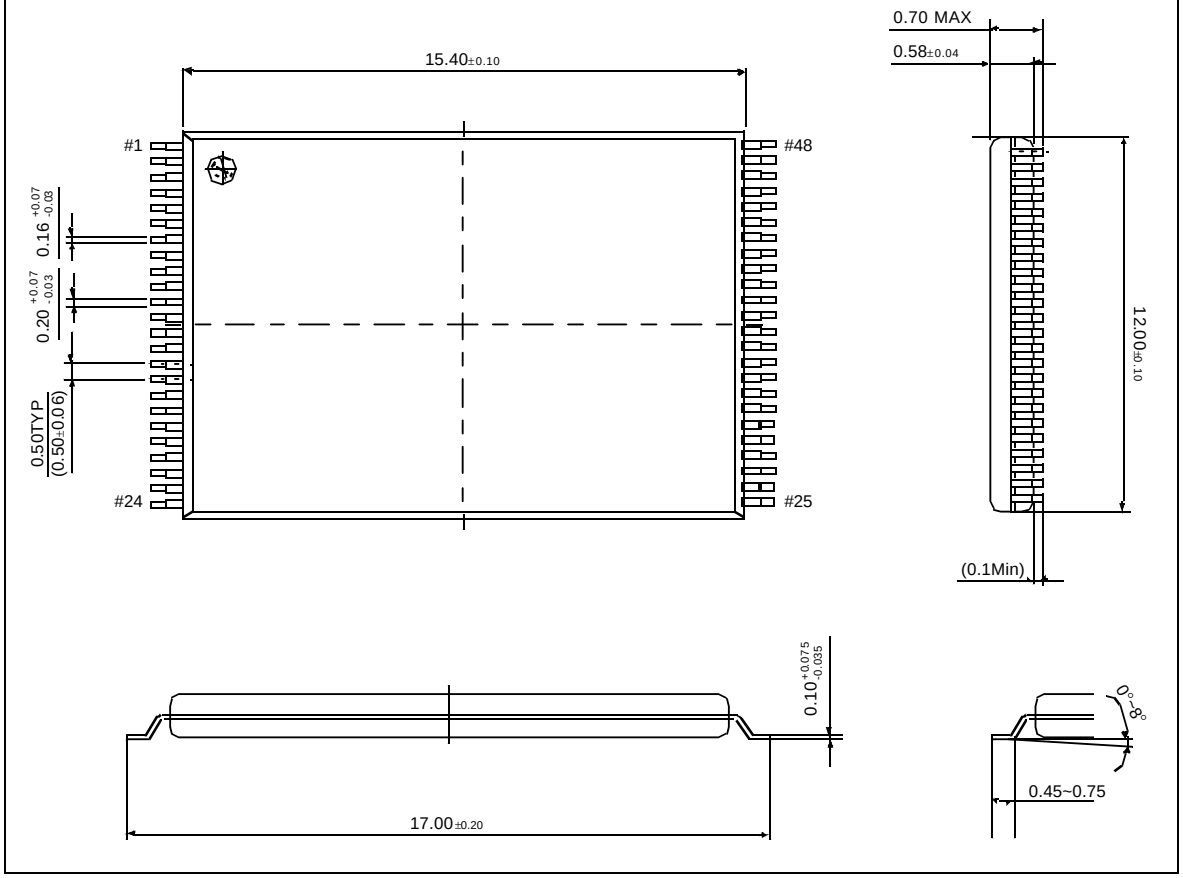
K9F2808U0B-VCB0/VIB0



PACKAGE DIMENSIONS

48-PIN LEAD PLASTIC VERY VERY THIN SMALL OUT-LINE PACKAGE TYPE (I)

48 - WSOP1 - 1217F Unit :mm



PIN DESCRIPTION

Pin Name	Pin Function
$I/O_0 \sim I/O_7$	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase opertion. Regarding $\overline{CE}$ control during read operation, refer to 'Page read' section of Device operation.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
$R/\overline{B}$	**READY/BUSY OUTPUT** The $R/\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VccQ	**OUTPUT BUFFER POWER** VccQ is the power supply for Output Buffer. VccQ is internally connected to Vcc, thus should be biased to Vcc.
Vcc	**POWER** Vcc is the power supply for device.
Vss	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.
GND	**GND INPUT FOR ENABLING SPARE AREA** To do sequential read mode including spare area , connect this input pin to Vss or set to static low state or to do sequential read mode excluding spare area , connect this input pin to Vcc or set to static high state.
DNU	**DO NOT USE** Leave it disconnected.

NOTE: Connect all Vcc and Vss pins of each device to common power supply outputs.

Figure 1. FUNCTIONAL BLOCK DIAGRAM

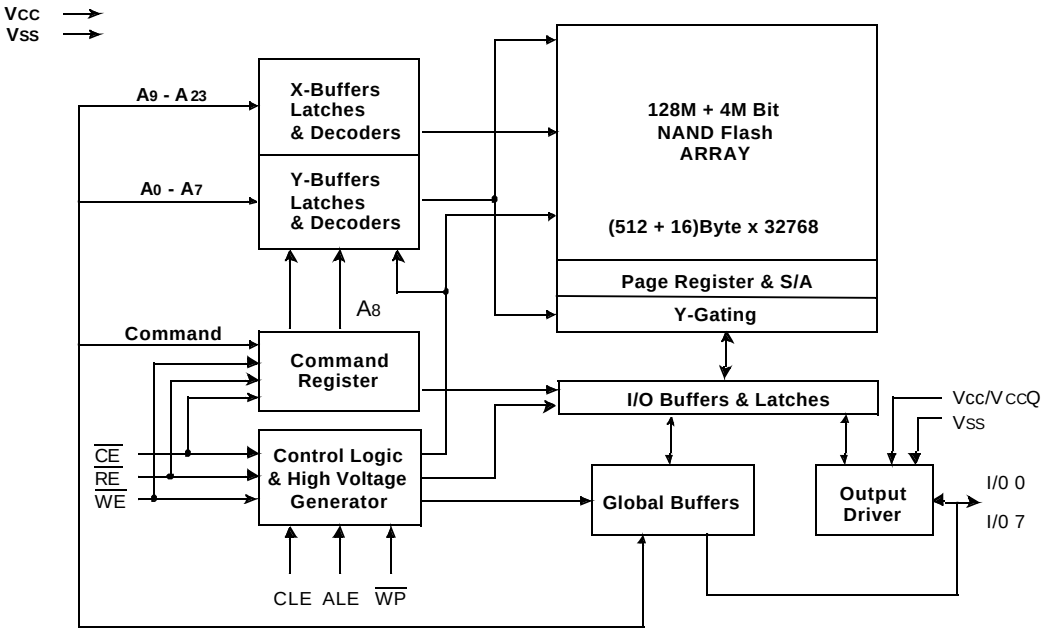
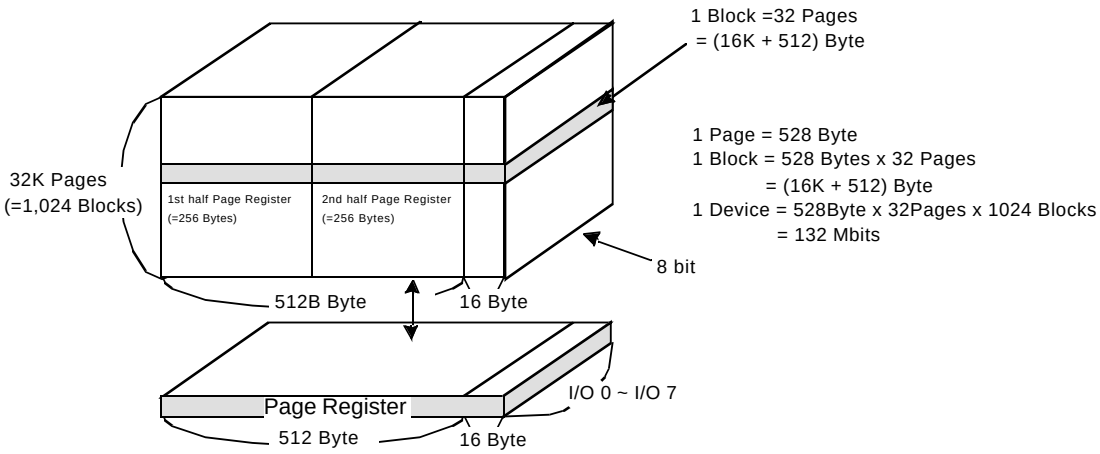


Figure 2. ARRAY ORGANIZATION



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16	Row Address (Page Address)
3rd Cycle	A17	A18	A19	A20	A21	A22	A23	*L	

NOTE : Column Address : Starting Address of the Register.

00h Command(Read) : Defines the starting address of the 1st half of the register.

01h Command(Read) : Defines the starting address of the 2nd half of the register.

* A8 is set to "Low" or "High" by the 00h or 01h Command.

* L must be set to "Low".

* The device ignores any additional input of address cycles than reguired.

PRODUCT INTRODUCTION

The K9F2808X0B is a 132Mbit(138,412,032 bit) memory organized as 32,768 rows(pages) by 528 columns. Spare 16 columns are located in 512 to 527 column address. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected like NAND structure. Each of the 16 cells resides in a different page. A block consists of the 32 pages formed by one NAND structures, totaling 8448 NAND structures of 16 cells. The array organization is shown in Figure 2. Program and read operations are executed on a page basis, while erase operation is executed on a block basis. The memory array consists of 1024 blocks, and a block is separately erasable by 16K-byte unit. It indicates that the bit by bit erase operation is prohibited on the K9F2808X0B.

The K9F2808X0B has addresses multiplexed with 8 I/O′s. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O′s by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except Page Program command and Block Erase command which require two cycles: one cycle for setup and another for execution. The 16M byte physical space requires 24 addresses, thereby requiring three cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following required command input. In Block Erase operation, however, only two row address cycles are used. Device operations are selected by writing specific commands into command register. Table 1 defines the specific commands of the K9F2808X0B.

Table 1. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read 1	00h/01h(1)	-	
Read 2	50h	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Block Erase	60h	D0h	
Read Status	70h	-	O

NOTE: 1. The 00h command defines starting address of the 1st half of registers.
The 01h command defines starting address of the 2nd half of registers.
After data access on 2nd half of register by the 01h command, start pointer is automatically moved to 1st half register(00h) on the next cycle.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			K9F2808Q0B(1.8V)	K9F2808U0B(3.3V)	
Voltage on any pin relative to V_{SS}		$V_{IN/OUT}$	-0.6 to + 2.45	-0.6 to + 4.6	V
		V_{CC}	-0.2 to + 2.45	-0.6 to + 4.6	V
		V_{CCQ}	-0.2 to + 2.45	-0.6 to + 4.6	V
Temperature Under Bias	K9F2808X0B-YCB0,DCB0	T_{BIAS}	-10 to + 125		°C
	K9F2808X0B-YIB0,DIB0		-40 to + 125		
Storage Temperature		T_{STG}	-65 to + 150		°C

NOTE:
1. Minimum DC voltage is -0.6V on input/output pins and -0.2V on Vcc and VccQ pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CCQ}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, K9F2808X0B-YCB0,DCB0:T_A=0 to 70°C, K9F2808X0B-YIB0,DIB0:T_A=-40 to 85°C)

Parameter	Symbol	K9F2808Q0B(1.8V)			K9F2808U0B(3.3V)			Unit
		Min	Typ.	Max	Min	Typ.	Max	
Supply Voltage	V_{CC}	1.7	1.8	1.9	2.7	3.3	3.6	V
Supply Voltage	V_{CCQ}	1.7	1.8	1.9	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	0	0	0	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	K9F2808Q0B(1.8V)			K9F2808U0B(3.3V)			Unit
				Min	Typ	Max	Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	$\overline{CE}$=V_{IL}, I_{OUT}=0mA K9F2808Q0B: tRC=70ns K9F2808U0B: tRC=50ns	-	5	15	-	10	20	mA
	Program	I_{CC2}	-	-	5	15	-	10	20	
	Erase	I_{CC3}	-	-	5	15	-	10	20	
Stand-by Current(TTL)		I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	-	-	1	
Stand-by Current(CMOS)		I_{SB2}	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	10	50	-	10	50	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±10	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	-	-	±10	
Input High Voltage		V_{IH}	I/O pins	VccQ-0.4		VccQ+0.3	2.0	-	VccQ+0.3	V
			Except I/O pins	V_{CC}-0.4	-	VCC +0.3	2.0	-	V_{CC}+0.3	
Input Low Voltage, All inputs		V_{IL}	-	-0.3	-	0.4	-0.3	-	0.8	
Output High Voltage Level		V_{OH}	K9F2808Q0B :I_{OH}=-100µA K9F2808U0B :I_{OH}=-400µA	VccQ-0.1	-	-	2.4	-	-	
Output Low Voltage Level		V_{OL}	K9F2808Q0B :I_{OL}=100uA K9F2808U0B :I_{OL}=2.1mA	-	-	0.1	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL} (R/$\overline{B}$)	K9F2808Q0B :V_{OL}=0.1V K9F2808U0B :V_{OL}=0.4V	3	4	-	8	10	-	mA

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	1004	-	1024	Blocks

NOTE:
1. The K9F2808X0B may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

AC TEST CONDITION

(K9F2808X0B-YCB0, DCB0 :TA=0 to 70°C, K9F2808X0B-YIB0,DIB0:TA=-40 to 85°C

K9F2808Q0B : Vcc=1.7V~1.9V , K9F2808U0B : Vcc=2.7V~3.6V unless otherwise noted)

Parameter	K9F2808Q0B	K9F2808U0B
Input Pulse Levels	0V to VccQ	0.4V to 2.4V
Input Rise and Fall Times	5ns	5ns
Input and Output Timing Levels	VccQ/2	1.5V
K9F2808Q0B:Output Load (VccQ:1.8V +/-10%) K9F2808U0B:Output Load (VccQ:3.0V +/-10%)	1 TTL GATE and CL=30pF	1 TTL GATE and CL=50pF
K9F2808U0B:Output Load (VccQ:3.3V +/-10%)	-	1 TTL GATE and CL=100pF

CAPACITANCE (T_A=25°C, V_{CC}=1.8V/3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L		H	X	Read Mode	Command Input
L	H	L		H	X		Address Input(3clock)
H	L	L		H	H	Write Mode	Command Input
L	H	L		H	H		Address Input(3clock)
L	L	L		H	H	Data Input	
L	L	L	H		X	Data Output	
L	L	L	H	H	X	During Read(Busy) on K9F2808U0B_Y or K9F2808U0B_V	
X	X	X	X	H	X	During Read(Busy) on the devices except K9F2808U0B_Y and K9F2808U0B_V	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program/Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	K9F2808Q0B:300 K9F2808U0B:200	500	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	2	cycles
	Spare Array		-	-	3	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	K9F2808Q0B		K9F2808U0B		Unit
		Min	Max	Min	Max	
CLE Set-up Time	tCLS	0	-	0	-	ns
CLE Hold Time	tCLH	20	-	10	-	ns
$\overline{CE}$ Setup Time	tCS	0	-	0	-	ns
$\overline{CE}$ Hold Time	tCH	20	-	10	-	ns
$\overline{WE}$ Pulse Width	tWP	25 (1)	-	25	-	ns
ALE Setup Time	tALS	0	-	0	-	ns
ALE Hold Time	tALH	20	-	10	-	ns
Data Setup Time	tDS	20	-	20	-	ns
Data Hold Time	tDH	20	-	10	-	ns
Write Cycle Time	tWC	70	-	50	-	ns
$\overline{WE}$ High Hold Time	tWH	20	-	15	-	ns

NOTE :
1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

AC Characteristics for Operation

Parameter		Symbol	K9F2808Q0B		K9F2808U0B		Unit
			Min	Max	Min	Max	
Data Transfer from Cell to Register		tR	-	10	-	10	µs
ALE to $\overline{RE}$ Delay(ID read)		tAR1	20	-	20	-	ns
ALE to $\overline{RE}$ Delay(Read cycle)		tAR2	50	-	50	-	ns
CLE to $\overline{RE}$ Delay		tCLR	50	-	50	-	ns
Ready to $\overline{RE}$ Low		tRR	20	-	20	-	ns
$\overline{RE}$ Pulse Width		tRP	35	-	25	-	ns
$\overline{WE}$ High to Busy		tWB	-	150	-	100	ns
Read Cycle Time		tRC	70	-	50	-	ns
$\overline{CE}$ Access Time		tCEA	-	60	-	45	ns
$\overline{RE}$ Access Time		tREA	-	45	-	35	ns
$\overline{RE}$ High to Output Hi-Z		tRHZ	15	30	15	30	ns
$\overline{CE}$ High to Output Hi-Z		tCHZ	-	20	-	20	ns
$\overline{RE}$ High Hold Time		tREH	20	-	15	-	ns
Output Hi-Z to $\overline{RE}$ Low		tIR	0	-	0	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low		tWHR	60	-	60	-	ns
Device Resetting Time(Read/Program/Erase)		tRST	-	5/10/500(1)	-	5/10/500 (1)	µs
K9F2808U0B-Y only	Last RE High to Busy (at sequential read)	tRB	-	100	-	100	ns
	$\overline{CE}$ High to Ready(in case of inter-ception by $\overline{CE}$ at read)	tCRY	-	50 +tr(R/$\overline{B}$)(3)	-	50 +tr(R/$\overline{B}$)(3)	ns
	$\overline{CE}$ High Hold Time(at the last serial read)(2)	tCEH	100	-	100	-	ns

NOTE :
1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. To break the sequential read cycle, $\overline{CE}$ must be held high for longer time than tCEH.
3. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.

NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding invalid block(s) is so called as the invalid block information. Devices ,regardless of having invalid block(s), have the same quality level because all valid blocks have same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it's bit line and common source line is isolated by a select transistor. The system design must be able to mask out invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 6th byte in the spare area. Samsung makes sure that either 1st or 2nd page of every invalid bbck has non-FFh data at the column address of 517. Since invalid block information is also erasable in most cases, it is impossible to recover the information once it was erased. Therefore, system must be able to recognize the invalid block(s) based on the original invalid block information and create invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the original invalid block information is prohibited.

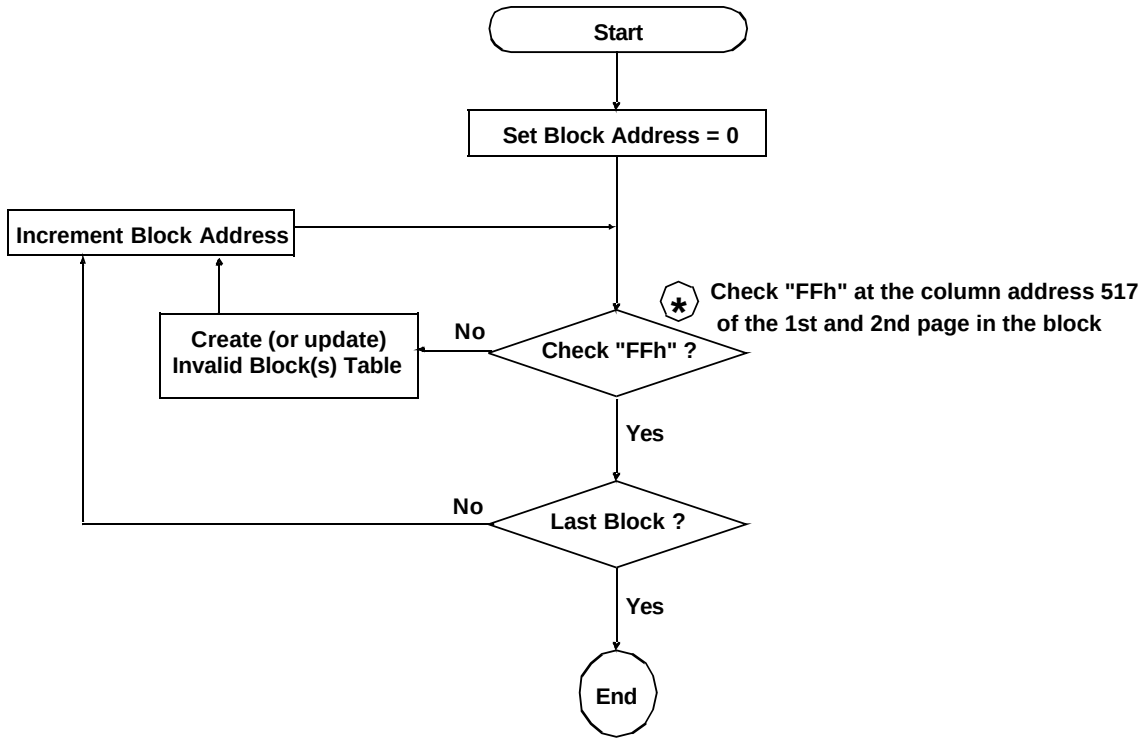


Figure 3. Flow chart to create invalid block table.

NAND Flash Technical Notes (Continued)

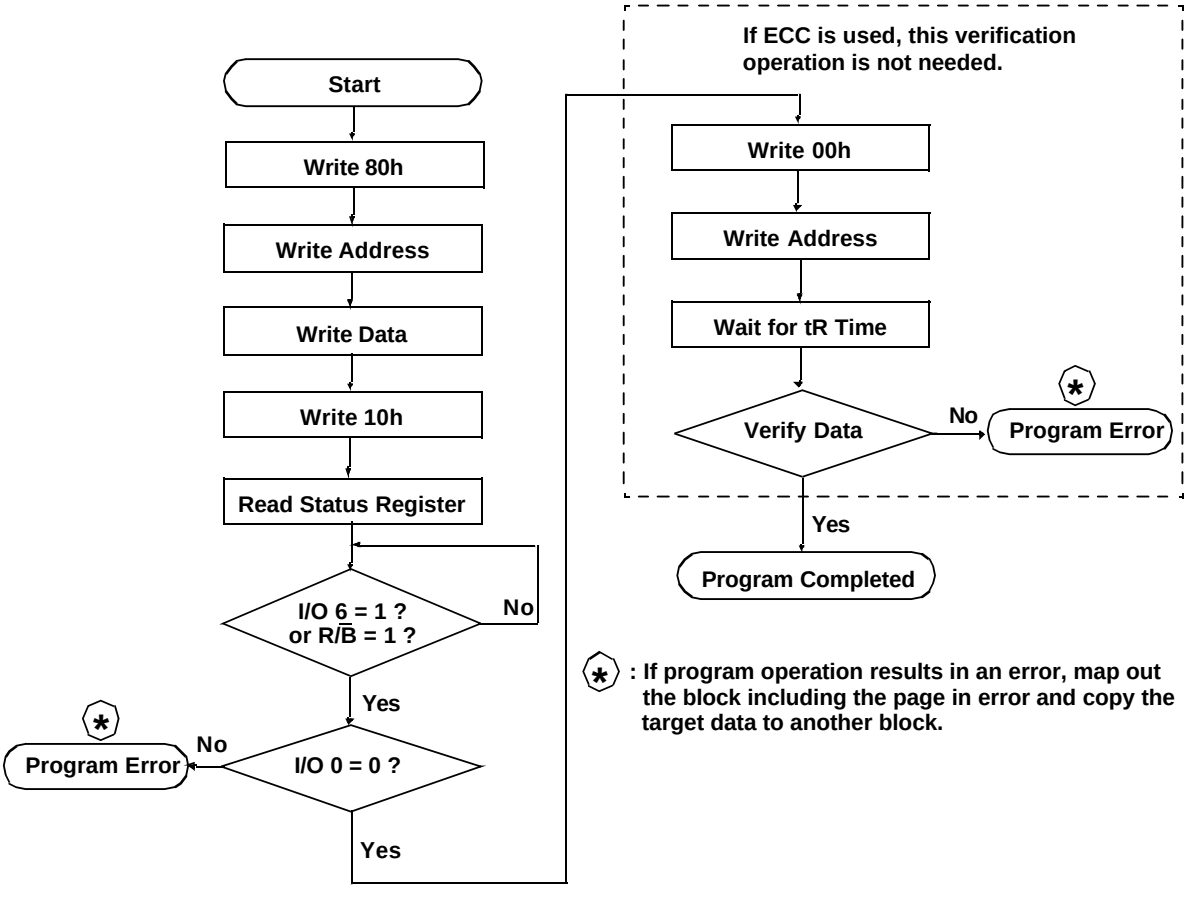
Error in write or read operation

Within its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. To improve the efficiency of memory space, we recommend using ECC without any block replacement in read or verification failure due to single bit error case. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> ECC Correction

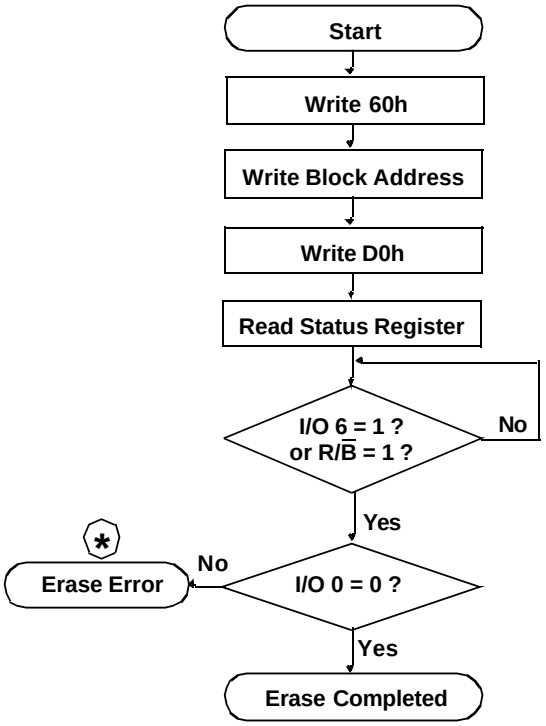
ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Program Flow Chart

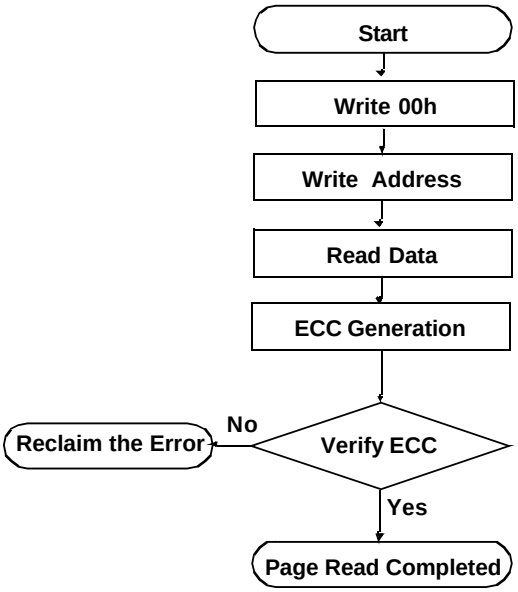


NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

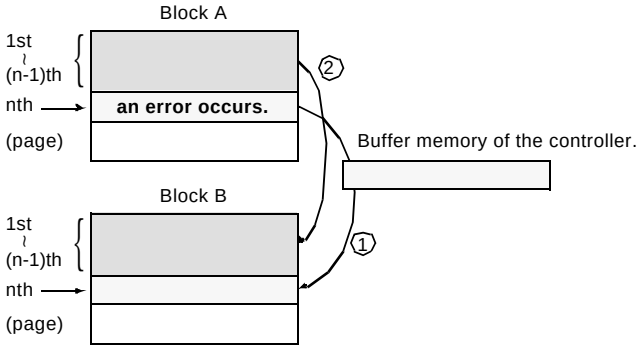


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement



* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block. (Block 'B')
* Step3
Then, copy the data in the 1st ~ (n-1)th page to the same location of the Block 'B'.
* Step4
Do not further erase Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

Pointer Operation of K9F2808X0B

Samsung NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. '00h' command sets the pointer to 'A' area(0~255byte), '01h' command sets the pointer to 'B' area(256~511byte), and '50h' command sets the pointer to 'C' area(512~527byte). With these commands, starting column address can be set to somewhere of a whole page(0~527byte). '00h' or '50h' is sustained until another address pointer command is entered. But, '01h' command is effective only for one time operation. After any operation of Read, Program, Erase, Reset, Power_Up following '01h' command, the address pointer returns to 'A' area by itself. To program data starting from 'A' or 'C' area, '00h' or '50h' command must be entered before '80h' command is written. A complete read operation prior to '80h' command is not necessary. To program data starting from 'B' area, '01h' command must be entered right before '80h' command is written.

Table 2. Destination of the pointer

Command	Pointer position	Area
00h	0 ~ 255 byte	1st half array(A)
01h	256 ~ 511 byte	2nd half array(B)
50h	512 ~ 527 byte	spare array(C)

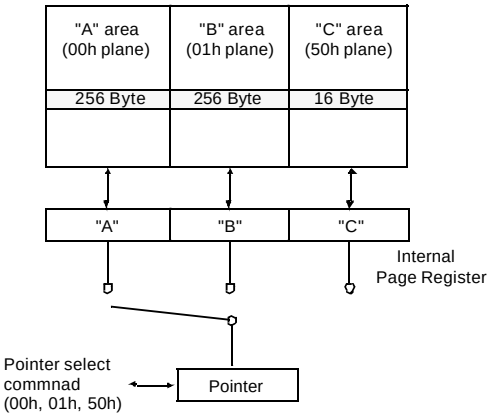
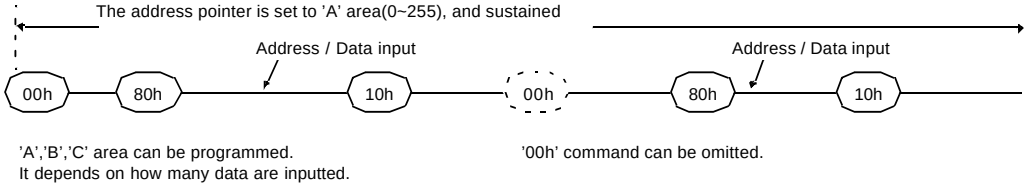
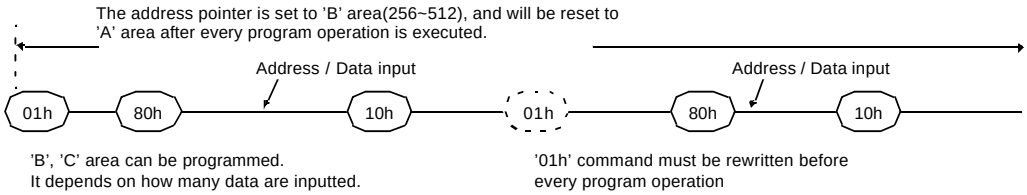


Figure 4. Block Diagram of Pointer Operation

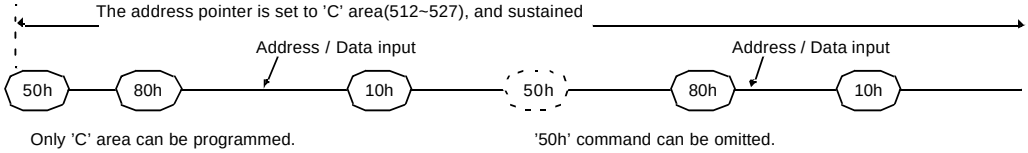
(1) Command input sequence for programming 'A' area



(2) Command input sequence for programming 'B' area



(3) Command input sequence for programming 'C' area



System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during data-loading or sequential data-reading as shown below. The internal 528byte page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant saving in power consumption.

Figure 5. Program Operation with $\overline{CE}$ don't-care.

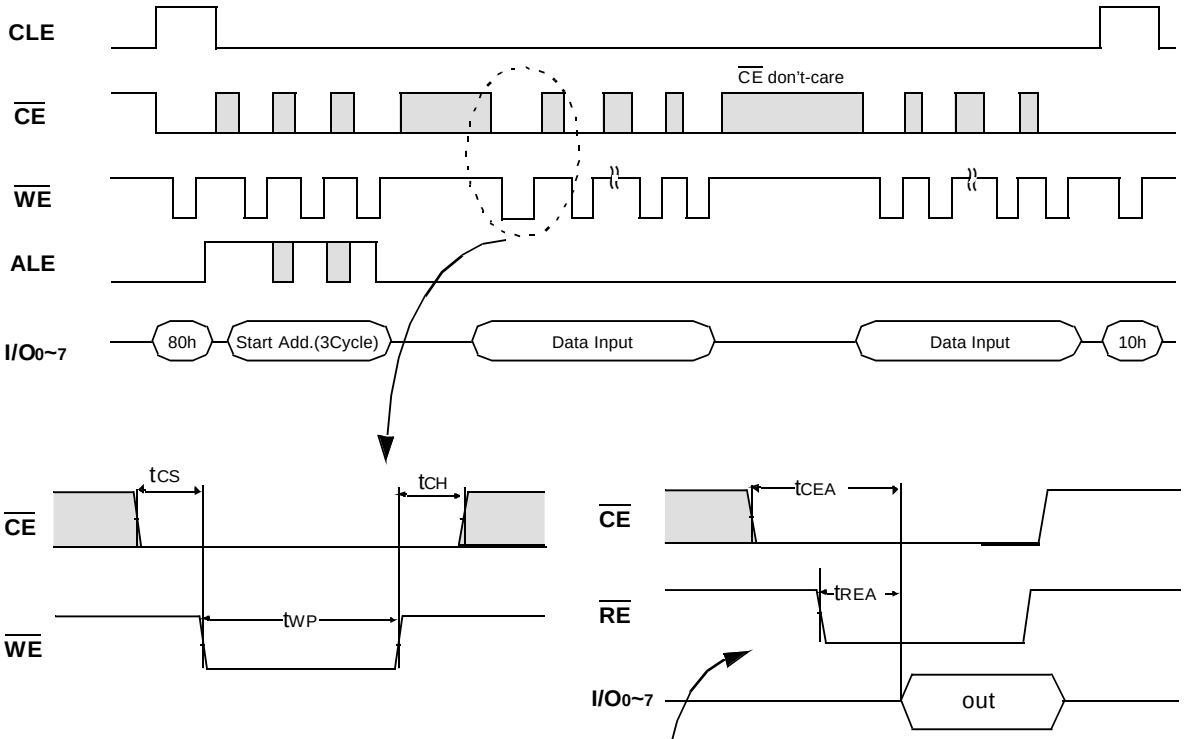
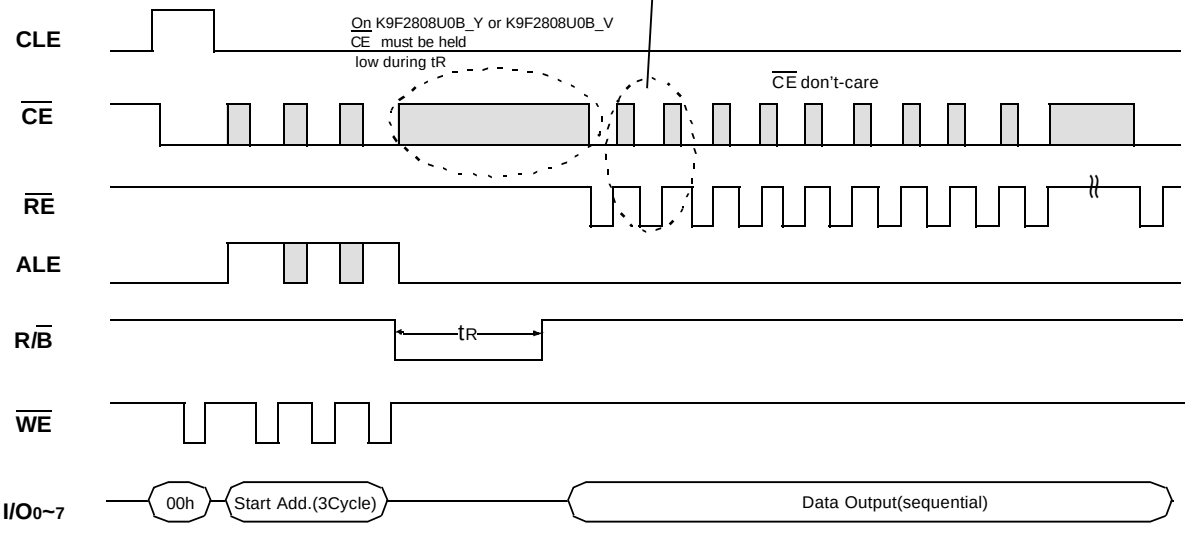
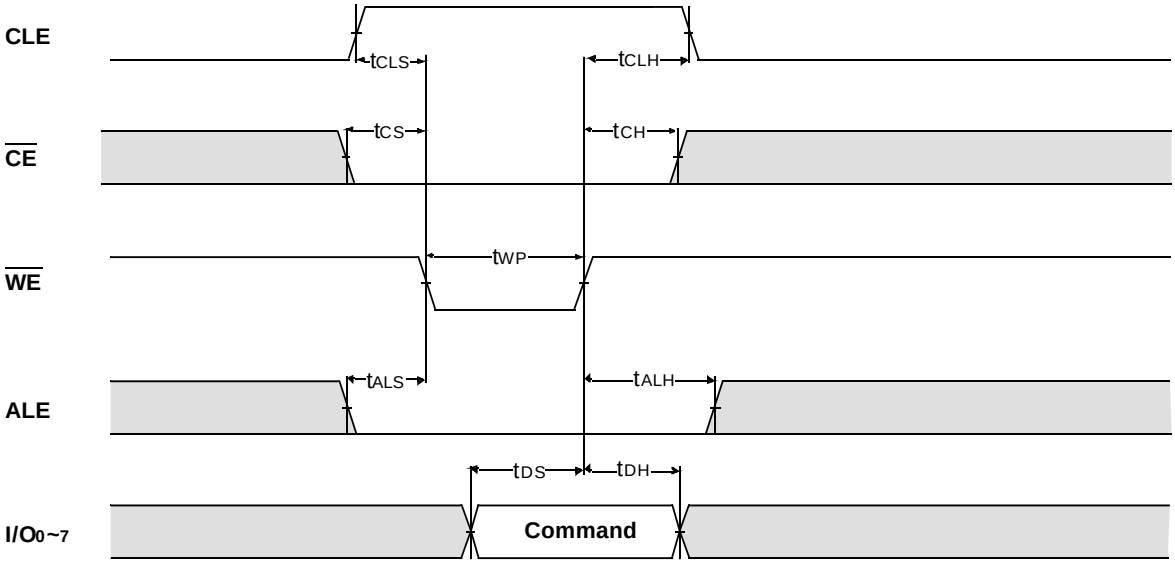


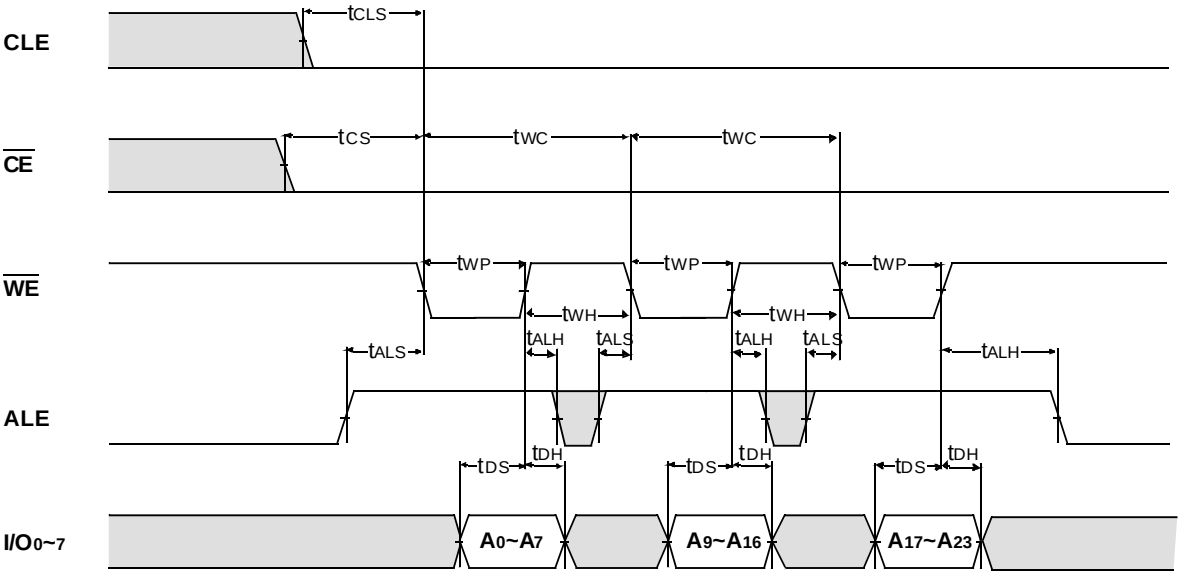
Figure 6. Read Operation with $\overline{CE}$ don't-care.



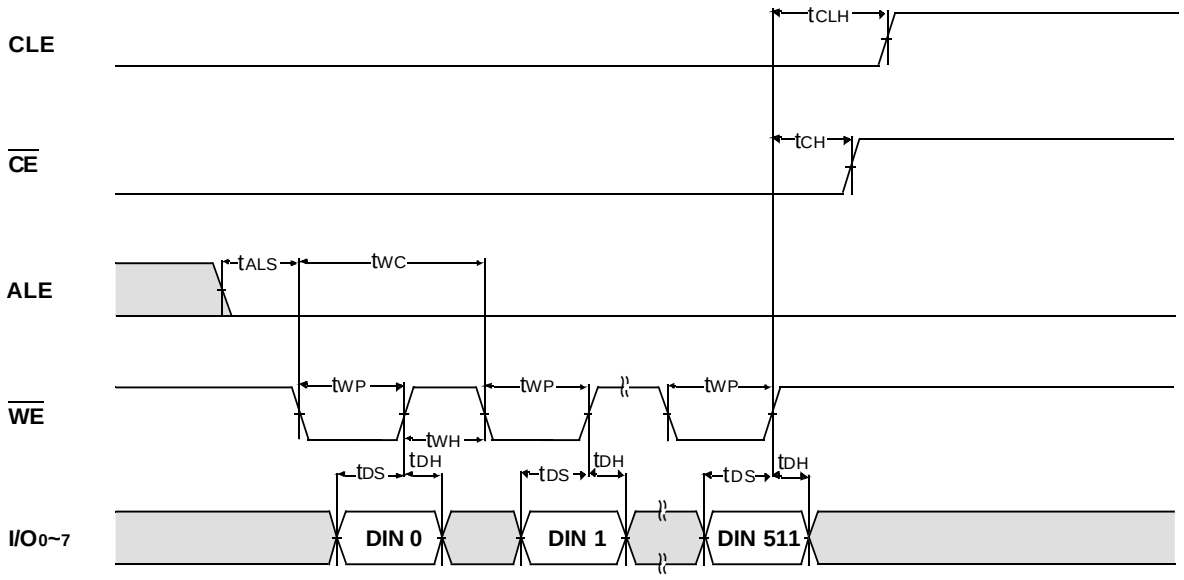
*** Command Latch Cycle**



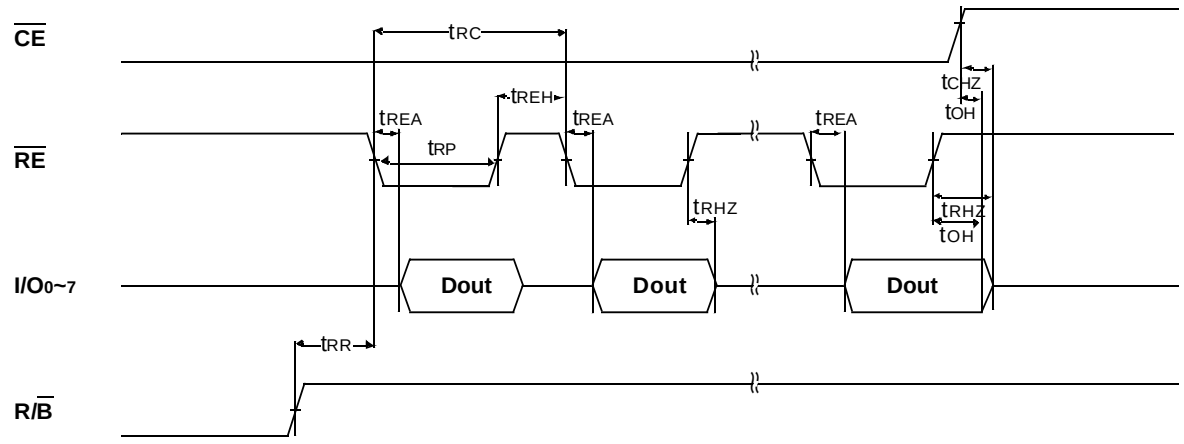
*** Address Latch Cycle**



*** Input Data Latch Cycle**

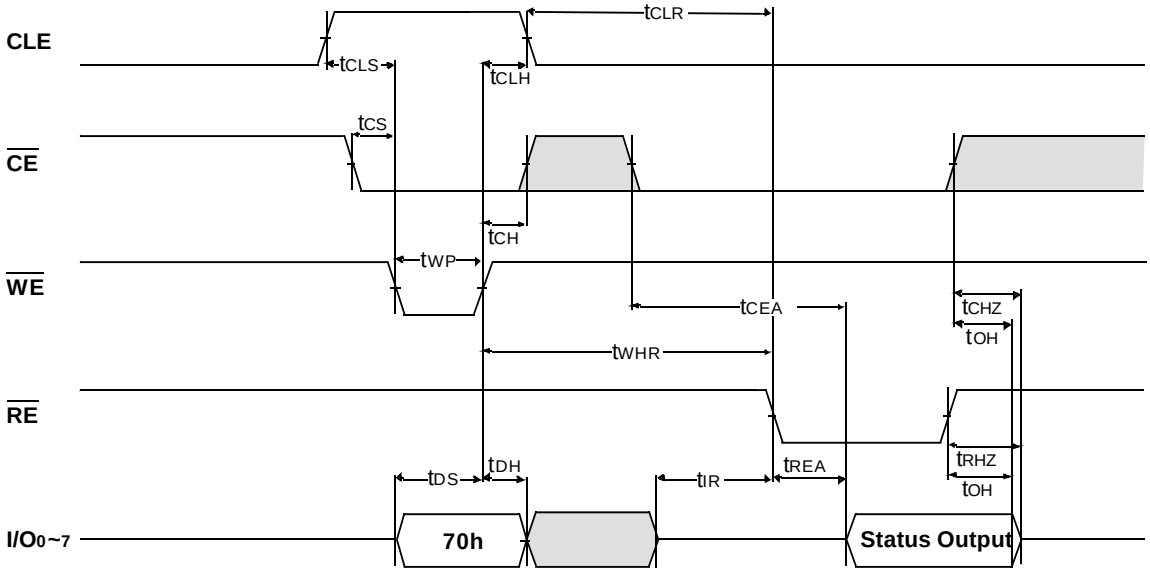


*** Serial Access Cycle after Read**(CLE=L, $\overline{WE}$=H, ALE=L)

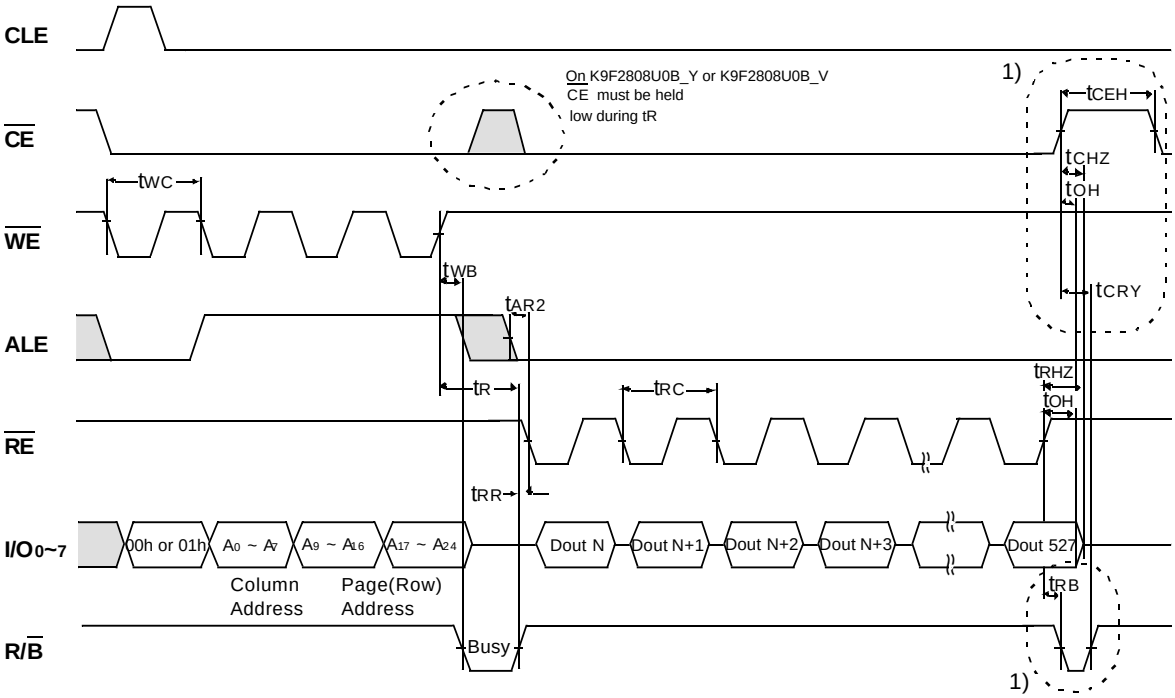


NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

*** Status Read Cycle**

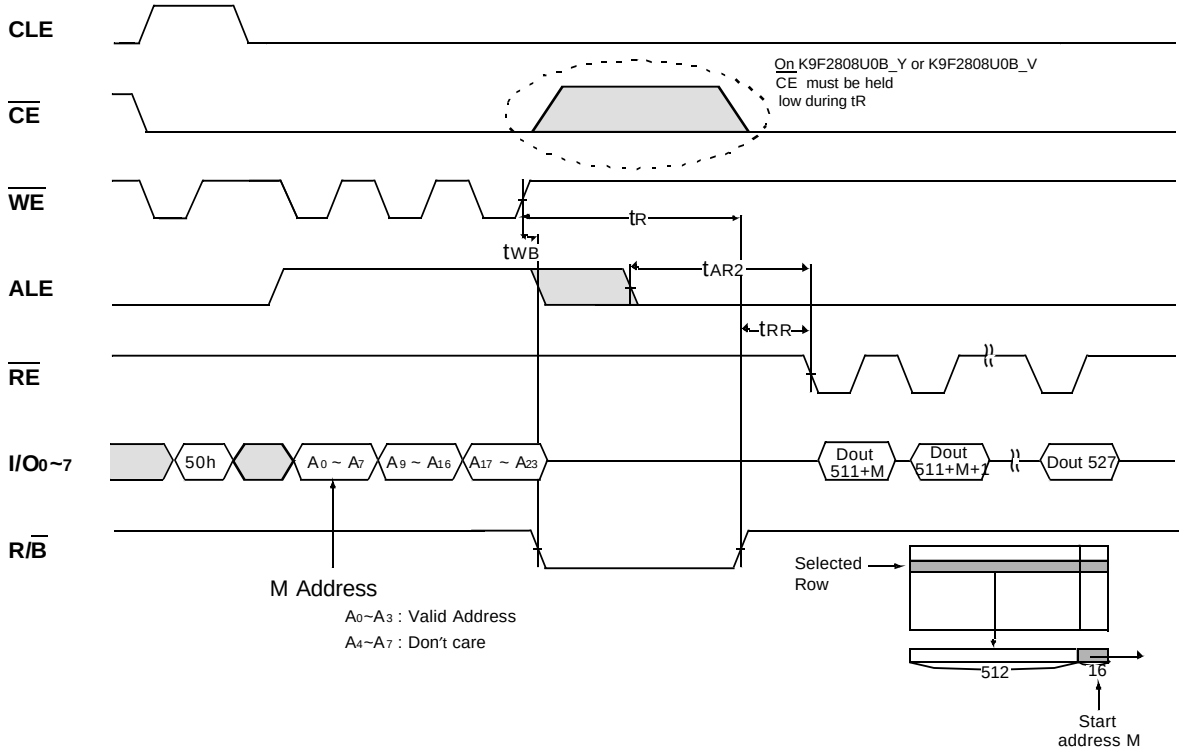


READ1 OPERATION(READ ONE PAGE)

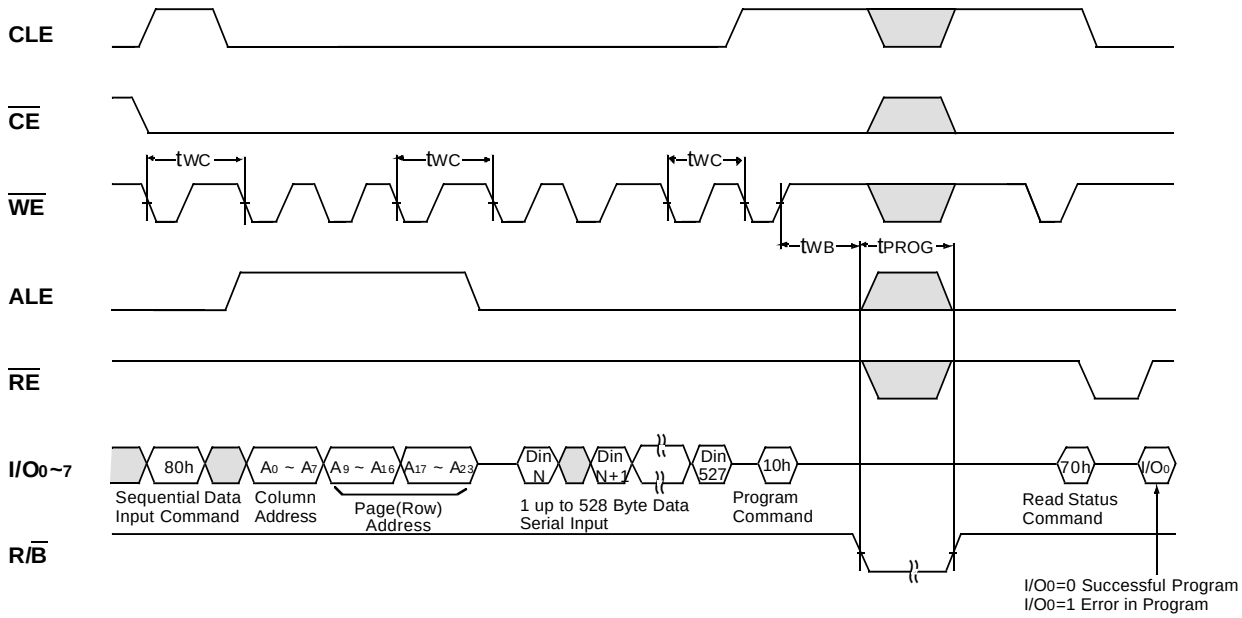


NOTE : 1) is only valid on K9F2808U0B_Y or K9F2808U0B_V

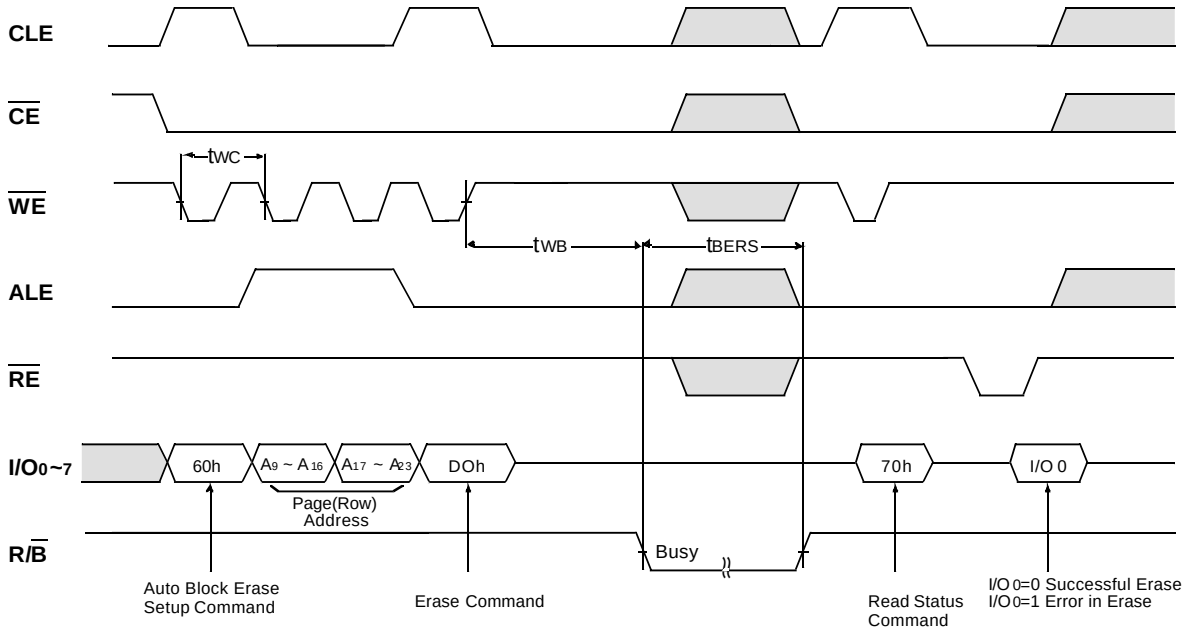
READ2 OPERATION (READ ONE PAGE)



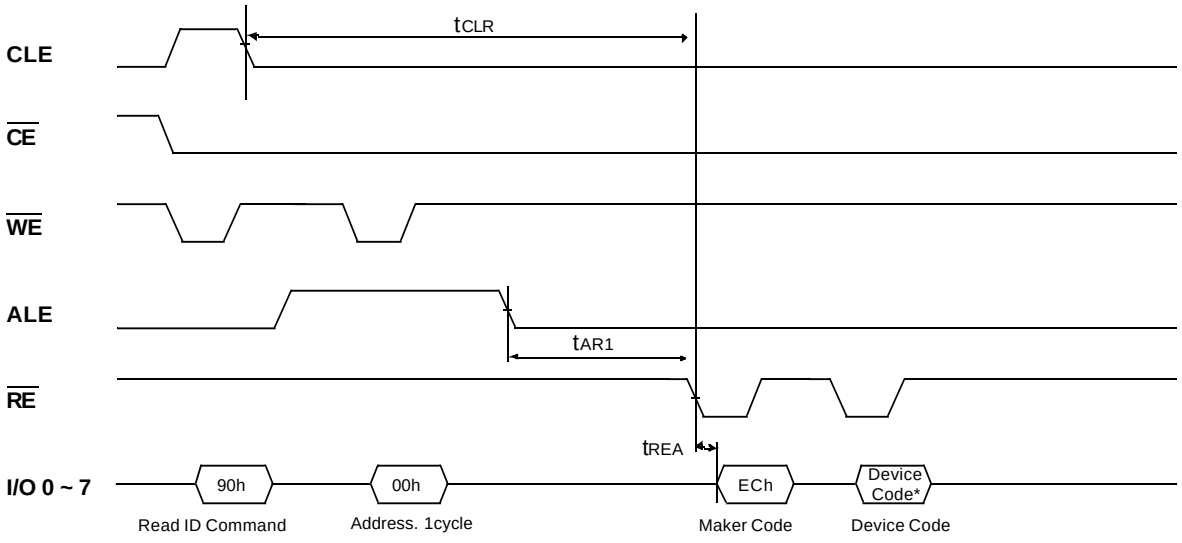
PAGE PROGRAM OPERATION



BLOCK ERASE OPERATION(ERASE ONE BLOCK)



MANUFACTURE & DEVICE ID READ OPERATION



Device	Device Code*
K9F2808Q0B	33h
K9F2808U0B	73h

DEVICE OPERATION

PAGE READ

Upon initial device power up, the device status is initially Read1 command(00h) latched. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Two types of operation are available : random read, serial page read. The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 10μs(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the registers, they may be read out by sequential $\overline{RE}$ pulse of 70ns/50n(K9F2808Q0B:70ns, K9F2808U0B:50ns) period cycle. High to low transitions of the $\overline{RE}$ clock take out the data from the selected column address up to the last column address.

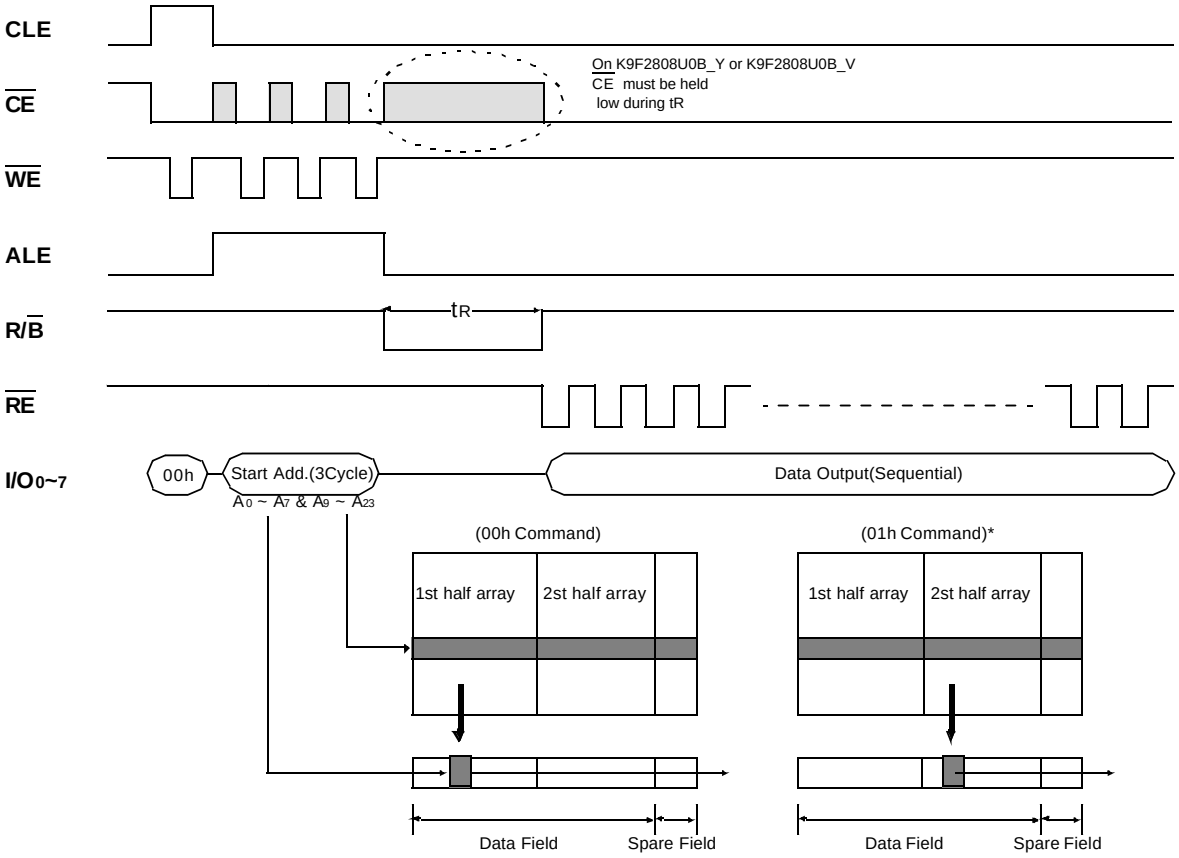
Read1 and Read2 commands determine pointer which selects either main area or spare area. The spare area(512 to 527 bytes) may be selectively accessed by writing the Read2 command. Addresses A_0 to A_3 set the starting address of spare area while addresses A_4 to A_7 are ignored. To move the pointer back to the main area, Read1 command(00h/01h) is needed. Figures 7 through 8 show typical sequence and timing for each read operation.

Figure 7,8 details the sequence.

Sequential Row Read is available only on K9F2808U0B_Y or K9F2808U0B_V :

After the data of last column address is clocked out, the next page is automatically selected for sequential row read. Waiting 10μs again allows reading the selected page. The sequential row read operation is terminated by bringing $\overline{CE}$ high. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Sequential Read 1 and 2 operation is allowed only within a block and after the last page of a block is readout, the sequential read operation must be terminated by bringing $\overline{CE}$ high. When the page address moves onto the next block, read command and address must be given. Figures 7-1, 8-1 show typical sequence and timings for sequential row read operation.

Figure 7. Read1 Operation



* After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

Figure 8. Read2 Operation

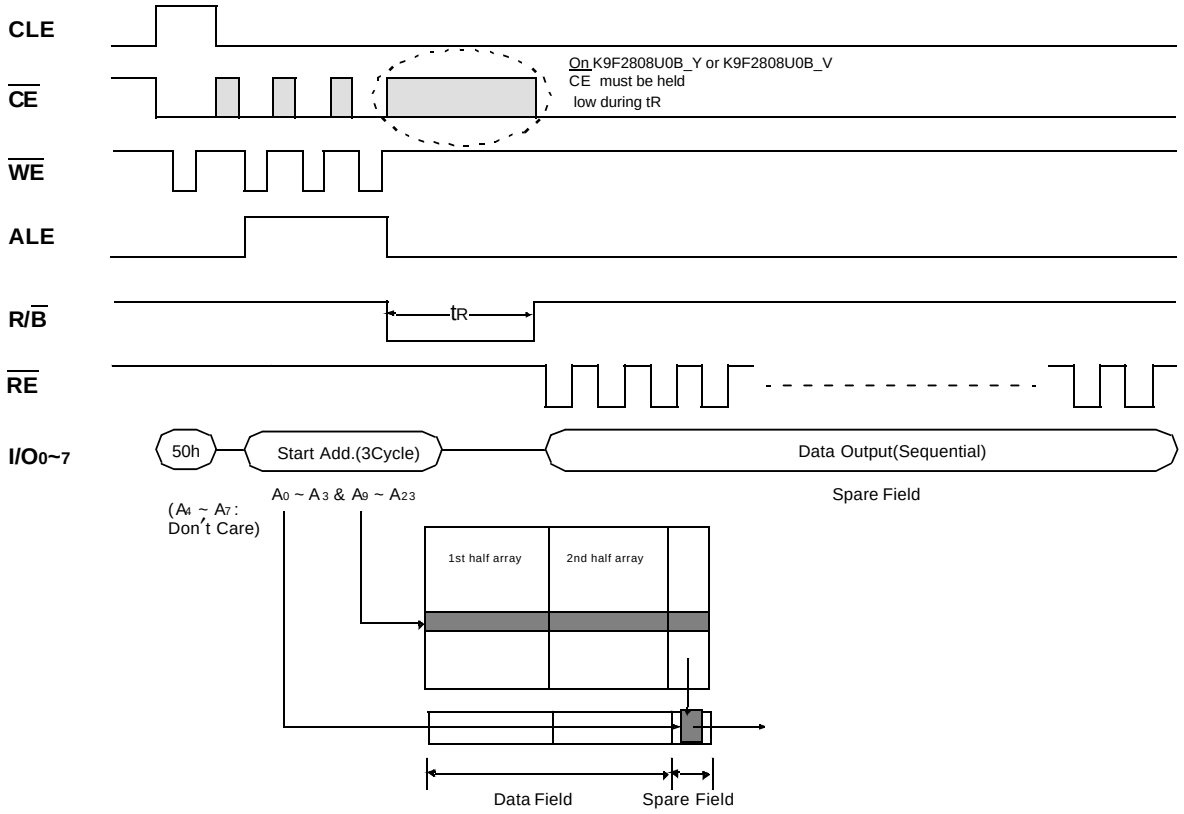


Figure 7-1. Sequential Row Read1 Operation (only for K9F2808U0B-Y and K9F2808U0B-V, valid within a block)

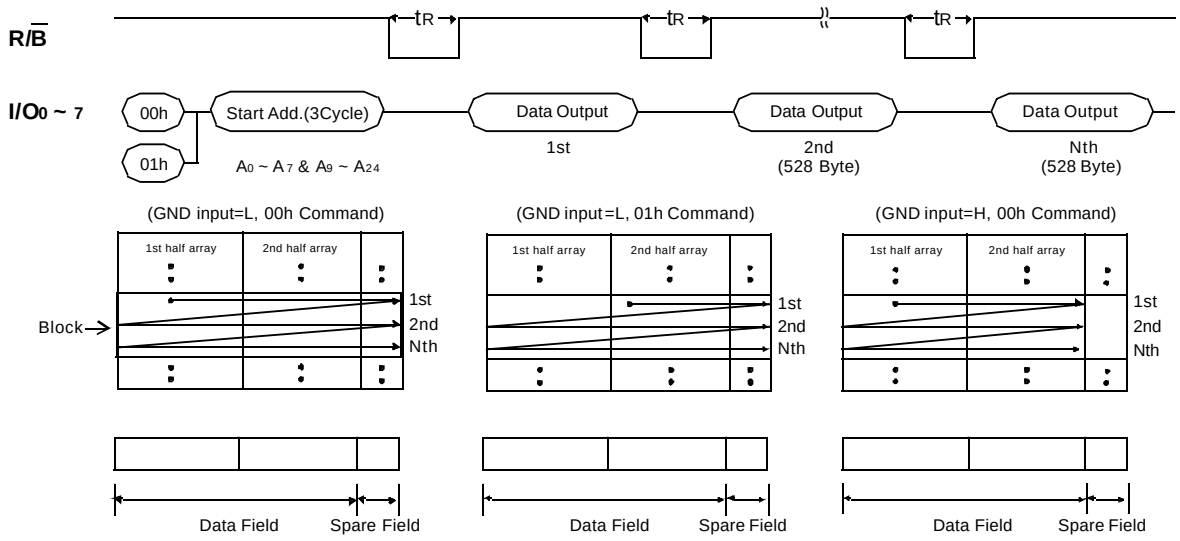
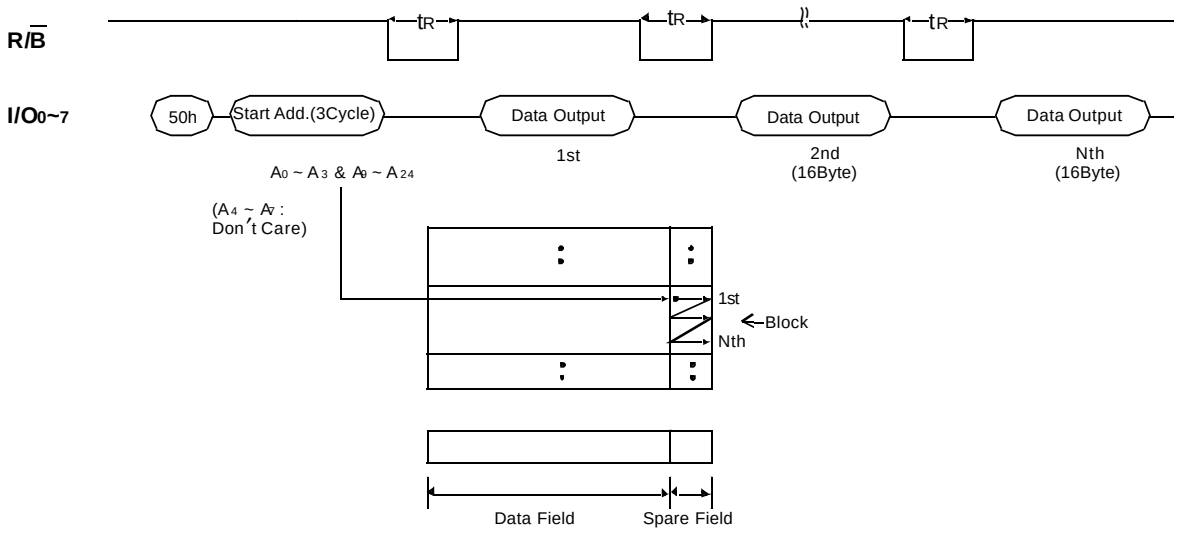


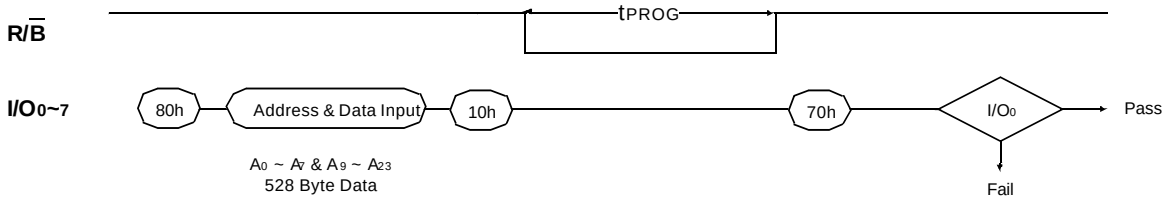
Figure 8-1. Sequential Row Read2 Operation (GND Input=Fixed Low)
(only for K9F2808U0B-Y and K9F2808U0B-V, valid within a block)



PAGE PROGRAM

The device is programmed basically on a page basis, but it allows multiple partial page program of one byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page program operation within the same page without intervening erase operation should not exceed 2 for main array and 3 for spare array. The addressing may be done in any random order in a block. Page program cycle consists of a serial data loading(up to 528 bytes of data) into the page register, and prog ram of loaded data into the appropriate cell. Serial data loading can start in 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes. Serial data loading is executed by entering the Serial Data Input command(80h) and three cycle address input and then serial data loading. The bytes except those to be programmed need not to be loaded. The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering 80h will not initiate program process. The internal write controller automatically executes the algorithms and timings necessary for program and verification, thereby freeing the CPU for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The CPU can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is completed, the Write Status Bit(I/O 0) may be checked(Figure 9). The internal write verification detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.
Figure 9 details the sequence.

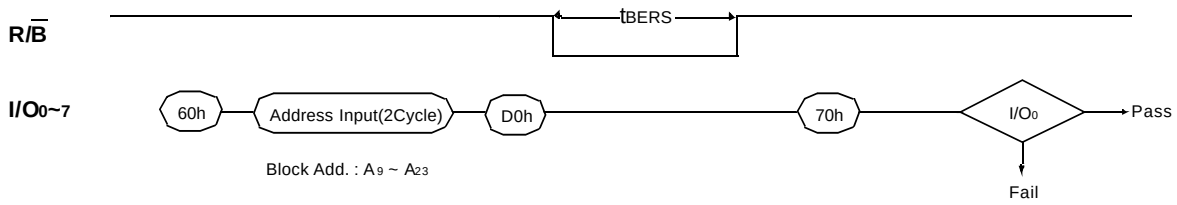
Figure 9. Program & Read Status Operation



BLOCK ERASE

The Erase operation is done on a block(16K Bytes) basis. Block Erase is executed by entering Erase Setup command(60h) and 2 cycle block addresses and Erase Confirm command(D0h). Only address A14 to A23 is valid while A9 to A13 is ignored. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise condition. At the rising edge of $\overline{WE}$ after erase confirm command input, internal write controller handles erase and erase-verification. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked.
Figure 10 details the sequence.

Figure 10. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to command register, a read cycle takes out the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 3 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

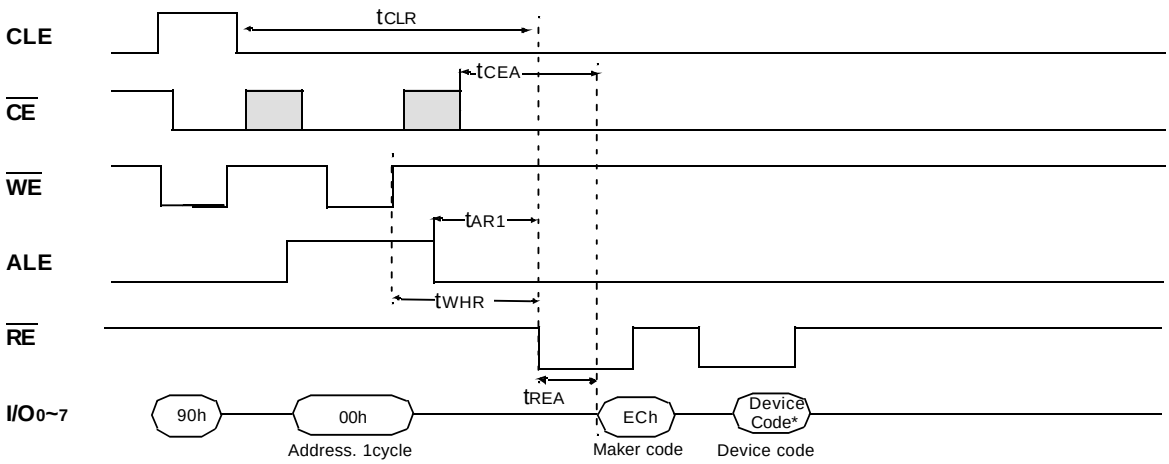
Table3. Read Status Register Definition

I/O #	Status	Definition
I/O 0	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
I/O 1	Reserved for Future Use	"0"
I/O 2		"0"
I/O 3		"0"
I/O 4		"0"
I/O 5		"0"
I/O 6	Device Operation	"0" : Busy "1" : Ready
I/O 7	Write Protect	"0" : Protected "1" : Not Protected

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code (73h) respectively. The command register remains in Read ID mode until further commands are issued to it.
Figure 11 shows the operation sequence.

Figure 11. Read ID Operation



Device	Device Code*
K9F2808Q0B	33h
K9F2808U0B	73h

RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 4 for device status after reset operation. If the device is already in reset state, new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Reset command is not necessary for normal operation. Refer to Figure 12 below.

Figure 12. RESET Operation

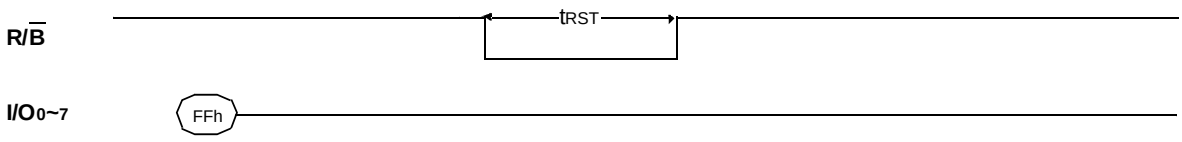


Table4. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 13). Its value can be determined by the following guidance.

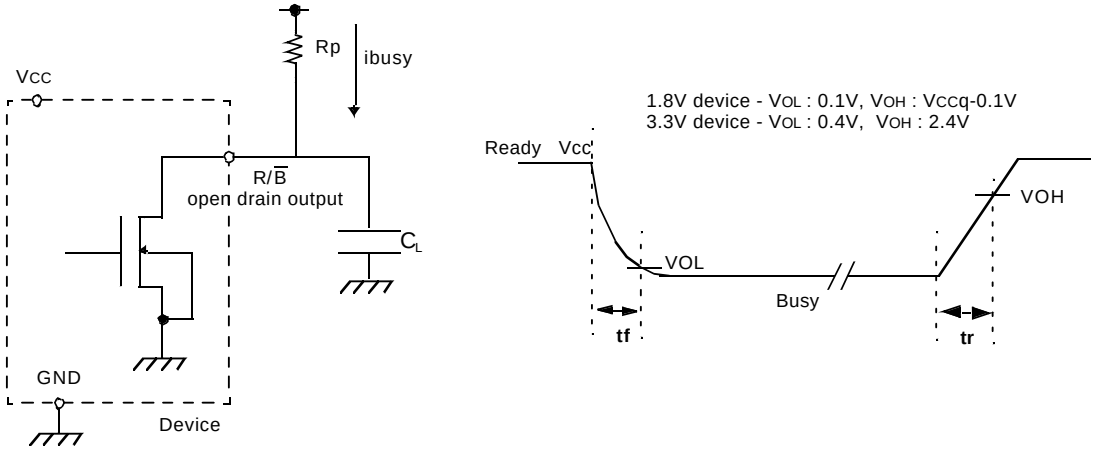
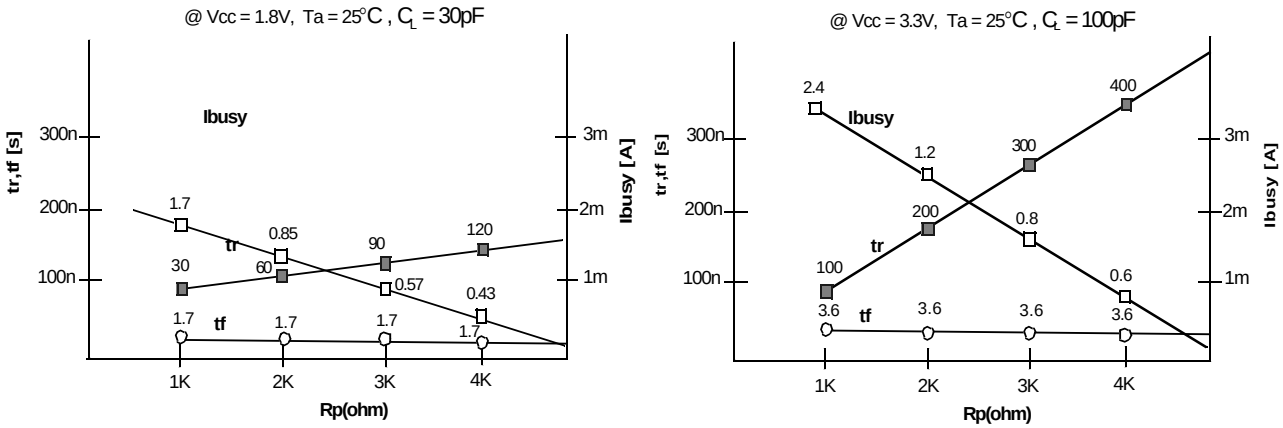


Fig 13 Rp vs tr ,tf & Rp vs ibusy



Rp value guidance

$$Rp(min, 1.8V part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

$$Rp(min, 3.3V part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Data Protection & Powerup sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.1V/2V(K9F2808Q0B:1.1V, K9F2808U0B:2V). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down and recovery time of minimum 1µs is required before internal circuit gets ready for any command sequences as shown in Figure 14. The two step command sequence for program/erase provides additional software protection.

Figure 14. AC Waveforms for Power Transition