

M62260FP

CS / BS CONVERTER DRIVER IC

DESCRIPTION

M62260FP is developed to be a 2-channel HEMT driver.

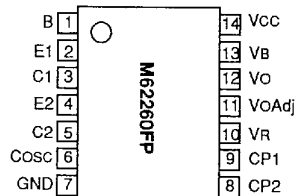
Capable of simplifying the peripheral circuits, this IC permits compact unitized design.

Incorporating in itself two power sources, +8V with high stability and great current capacity and -3.2V with simple construction, and the protective circuit designed to be actuated in the event of output overload or short, the IC has no restrictions to its applications.

FEATURES

- Sole connection of small-capacity power transistors permits the construction of a power source system, and therefore it is possible to produce low-cost sets with a small number of parts.
- The "L" shape protective circuit used as the over-current limiting circuit prevents heat generation and destruction in the event of output short.
- Since the high-precision +8V power source is arranged as pre-drive, sole connection of external transistors permits current output in the magnitude of hFE times 30 mA.
(when $hFE=50$, the resulting maximum current is 1.5 A.)
Since the power source can serve as a low dropout power source as well, even low line voltage such as a minimum of $V_o + 0.5V$ provides normal operation.
- The package is small with 14 pins.
- The use of voltage adjustment terminals permits external adjustment of output voltage.

PIN CONFIGURATION (TOP VIEW)

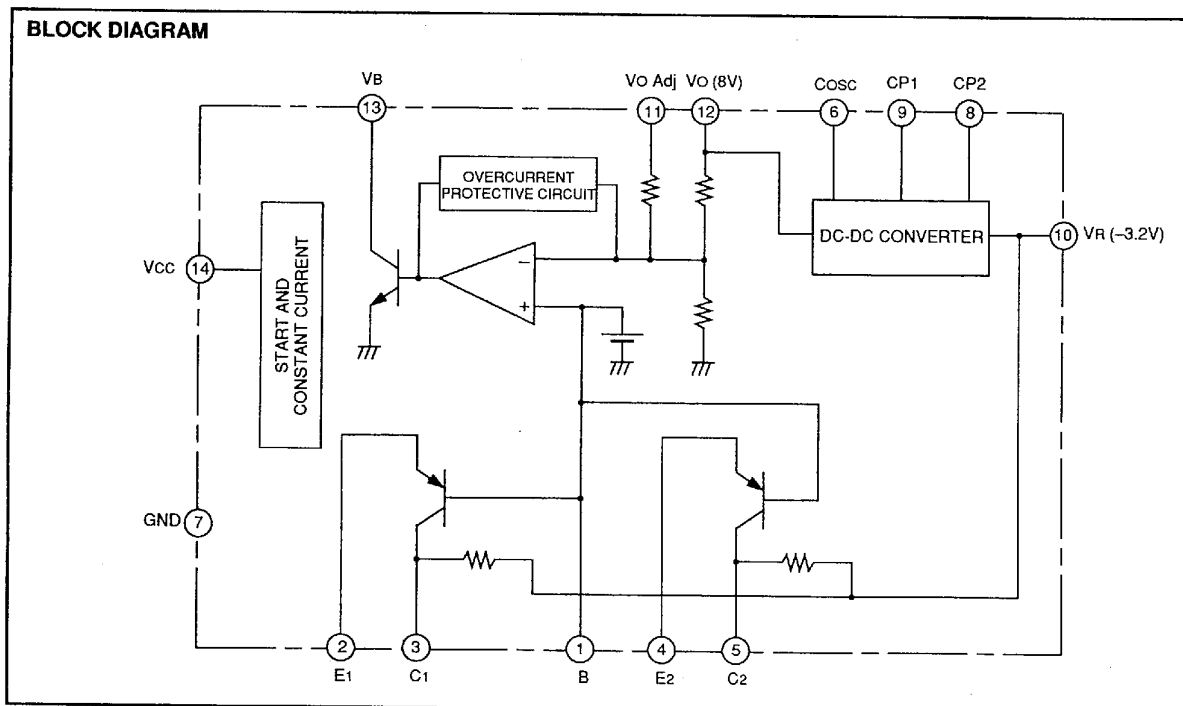


Outline 14P2P-A

APPLICATION

CS and BS converters and the like

BLOCK DIAGRAM



EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
①	B	HEMT driving PNP transistor base output(reference voltage output)
②	E1	HEMT driving PNP transistor emitter output 1
③	C1	HEMT driving gate bias output 1
④	E2	HEMT driving PNP transistor emitter output 2
⑤	C2	HEMT driving gate bias output 2
⑥	Cosc	DC-DC converter oscillation circuit capacitor connection terminal
⑦	GND	GND terminal
⑧	CP2	Charge pump capacitor connection terminal
⑨	CP1	Charge pump capacitor connection terminal
⑩	VR	Negative output voltage terminal
⑪	VOADJ	Positive and negative output voltage adjustment terminal
⑫	VO	Positive output voltage terminal
⑬	VB	External transistor base drive terminal
⑭	Vcc	Power supply terminal

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		23	V
Pd	Power dissipation		550	mW
Kθ	Thermal derating	Ta>=25°C	5.5	mW/°C
Topr	Operating temperature		-30~+85	°C
Tstg	Storage temperature		-55~+125	°C

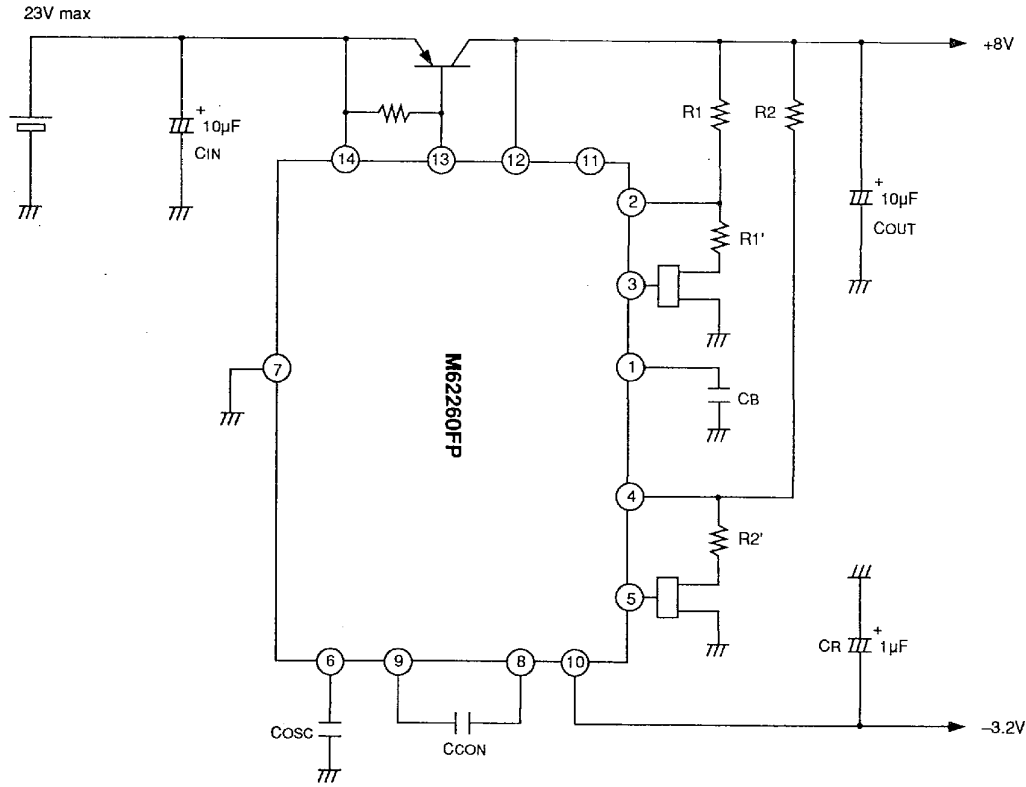
ELECTRICAL CHARACTERISTICS (Vcc = 12 V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Vcc	Supply voltage		Vo+0.5		22	V
Icc	Circuit current			10	15	mA
IBmax	MAXIMUM Bias current		10	30		mA
Vo	Positive output voltage	In steady state (VOAdj : open)	7.6	8.0	8.4	V
		VOAdj-Vo terminal short	4.75	5.0	5.25	
VR	Negative output voltage	In steady state (VOAdj : open)	-4.0	-3.2	-2.4	V
		VOAdj-Vo terminal short	-2.5	-2.0	-1.5	
V1	Reference voltage		2.38	2.5	2.62	V
I BSC	Positive output short bias current			1		mA
Reg-in	Positive output input regulation	Vcc=8.5V~22V		0.02		%/V
Reg-lo	Positive output load regulation	Io=10mA~100mA		20		mV
VoN	Positive output noise voltage	BPF:10Hz~100kHz, Io=100mA		170	300	μVrms
R.R	Positive output ripple removal ratio		40	60		dBm
ΔVo/ΔT	Positive output voltage temperature coefficient			0.02		%/T
⊖ Reg-lo	Negative output load regulation	IR=-0.5mA~-3mA		0.6	0.9	V
ΔVR/ΔT	Negative output voltage temperature coefficient			0.02		%/T
ΔVR	Negative output ripple voltage	IR=0		20	30	mV
ΔVo	Positive output clock leak voltage	IL=0		10	20	mV

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APPLICATION EXAMPLE

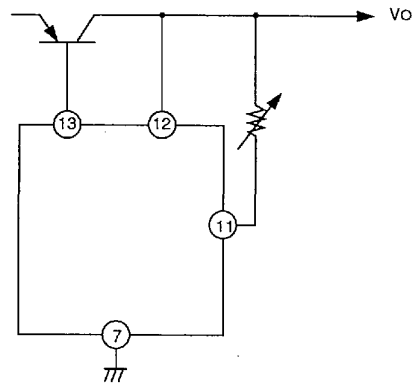


* R1' and R2' are required for VDS adjustment.

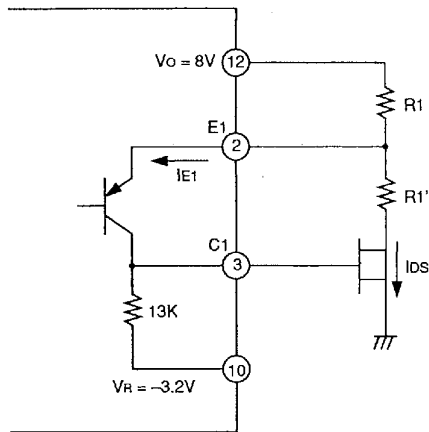
VoAdj terminal (pin ⑪)

This terminal is the adjustment terminal for Vo, VR.
 Insertion of an adjustment resistor between pins ⑪, ⑫, as shown in the diagram at right, permits adjustment in the range of $5V \leq V_o \leq 8V$.

(When pins ⑪, ⑫ are shorted, $V_o = 5V$)
 VR changes according to Vo setting.
 $V_R = -0.4V_o (V)$

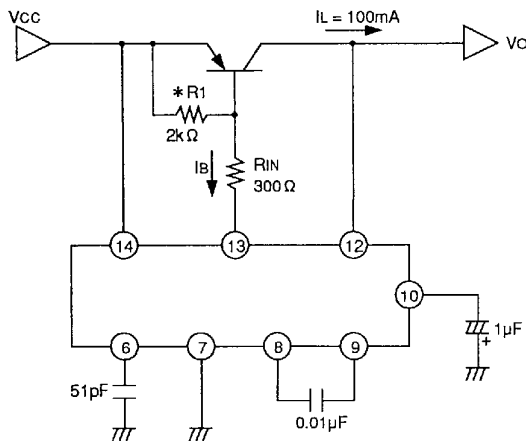


HEMT BIAS CIRCUIT



- $R1 = (V_o - V_B + V_{BE}) / (I_{DS} + I_{E1})$, $R1' = (V_B + V_{BE} - V_{DS}) / I_{DS}$
 $(V_o = 8V, V_B = 2.5V, V_{BE} = 0.7V, I_{DS} = 10mA, V_{DS} = 2V, I_{E1} = 0.23mA)$
 $R1 = (8V - 2.5V + 0.7V) / (10mA + 0.23mA)$
 $= 4.8V / 10.23mA$
 $R1 \approx 470\Omega$
- $R1' = (2.5V + 0.7V - 2V) / 10mA$
 $= 1.2V / 10mA$
 $R1' \approx 120\Omega$
- $V_{GS} = I_{E1} \cdot 13K - 3.2V$
 $= 2.99V - 3.2V$
 $V_{GS} = -0.21V$
 $R1 \approx 470\Omega, R1' \approx 120\Omega, V_{GS} = -0.21V$

Example application to limit the maximum bias current.



* R1 should be between 700Ω ~ 6kΩ

When the input voltage (Vcc) is lower than the set output voltage (Vo), approx. 30 ~ 45mA bias current flows through pin ⑬ of the IC (see the bias current-line voltage characteristics diagram).

Insertion of a resistor, Rin, as needed such as when the bias current need be limited, permits limiting the bias current (see Fig. 1 for the line voltage dependence of the input resistance, Rin and the limited current.)

In this applied circuit, the current flowing through pin ⑬ is limited to approx. 20 mA when the line voltage (Vo) is 8V.

Fig. 2 presents the bias current vs. line voltage characteristics of this applied circuit.

MAXIMUM BIAS CURRENT LIMITING (I_{BM})

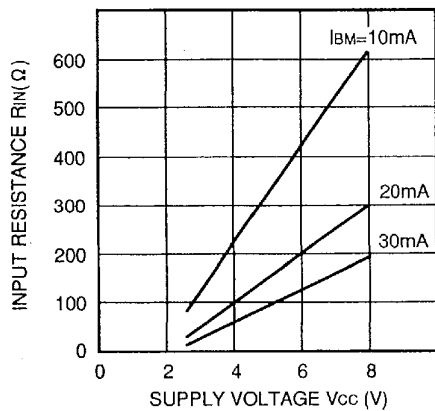


Fig. 1

BIAS CURRENT VS. LINE VOLTAGE

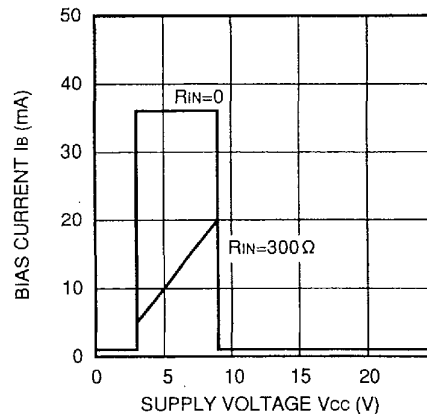


Fig. 2

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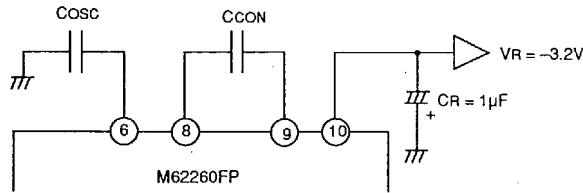
- DC-DC converter oscillation frequency setting equation.

$$f = \frac{1}{26 \times 10^3 \cdot C_{osc} + 1 \times 10^{-6}} \text{ [Hz]}$$

<Example C_{osc}-C_{con} ratio>

C _{osc} (PF)	C _{con} (μF)	f (kHz)
500	0.1	90
100	0.022	333
50	0.01	500

- Setting on the capacitors (C_{osc}, C_{con}) to produce negative power source (V_R).



SET THE C_{osc}-C_{con} RATIO TO 1: 200 OR GREATER.

TYPICAL CHARACTERISTICS

