

OVERVIEW

The SM5003 Series is quartz crystal oscillator ICs fabricated in NPC's Molybdenum-gate CMOS. They comprise low-voltage low-current consumption oscillator circuits

and output buffers. They incorporate built-in oscillation capacitance with superior frequency response to realize without any external components.

FEATURES

- Oscillation frequency up to 70MHz
- 3rd overtone oscillation
- 4.5 to 5.5 V supply voltage
- Inverter amplifier feedback resistance built-in (R_f)
- Oscillation capacitance built-in (C_G and C_D)
- Output drive capability : 8 mA ($V_{DD}=4.5V$)
- Output frequency : f_o (Oscillation frequency)
- Output duty level
SM5003A×H : CMOS
SM5003B×H : TTL
- Input level : TTL
- 3 state function
- Chip form (CF5003××)
- 6 pin SOT (SM5003××H)

DEVICE LIST

Device	Recommended frequency range (MHz)	gm (relative value)	Output duty level	Output (standby)	Internal capacitance		Rf (kΩ)
					C _G (pF)	C _D (pF)	
SM5003AAH	22 to 30	1.0	CMOS	Hi-Z	8	15	6.1
SM5003ABH	30 to 43	1.0	CMOS	Hi-Z	8	15	3.3
SM5003ACH	43 to 55	2.0	CMOS	Hi-Z	8	15	3.9
SM5003ADH	55 to 70	3.0	CMOS	Hi-Z	8	15	2.7
SM5003BAH	22 to 30	1.0	TTL	Hi-Z	8	15	6.1
SM5003BBH	30 to 43	1.0	TTL	Hi-Z	8	15	3.3
SM5003BCH	43 to 55	2.0	TTL	Hi-Z	8	15	3.9
SM5003BDH	55 to 70	3.0	TTL	Hi-Z	8	15	2.7

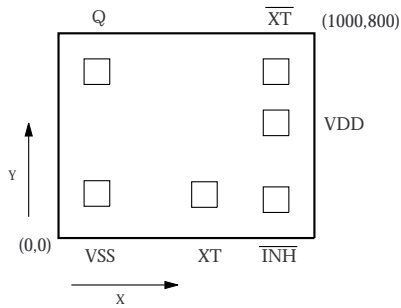
Notes :

CF5003×× is Chip form.

SM5003××H is 6 pin SOT.

SM5003 Series

PAD DIMENSIONS

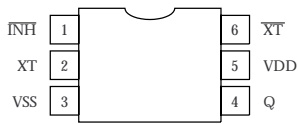


PAD COORDINATES

Name	Coordinates (μm)	
	X	Y
VSS	150	174
XT	570	170
$\overline{\text{INH}}$	850	150
VDD	850	450
$\overline{\text{XT}}$	850	650
Q	150	650

Chip size : 1.00x0.80mm
 Chip thickness : 250±30μm
 Chip reverse side : VDD level

PIN CONFIGURATION (Top View)

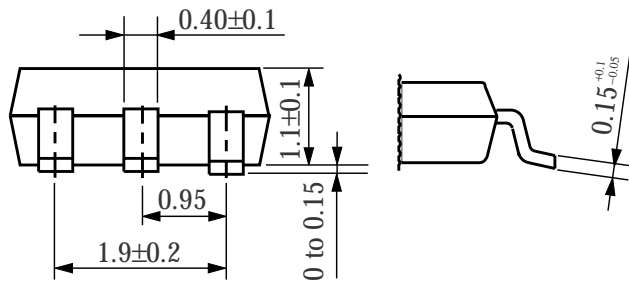
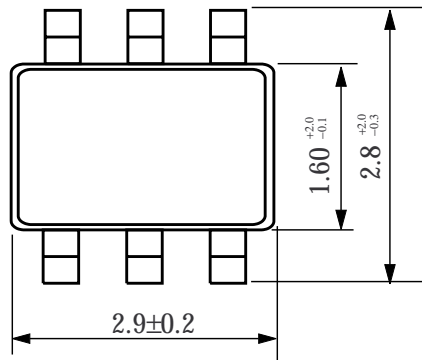


TERMINAL DESCRIPTIONS

Name	Descriptions
XT	Oscillator input pin
$\overline{\text{XT}}$	Oscillator output pin
$\overline{\text{INH}}$	Output state control input pin (with built-in pull-up resistance)
VDD	Supply voltage
VSS	Ground
Q	Output pin (fo:Oscillator frequency output XT pin)

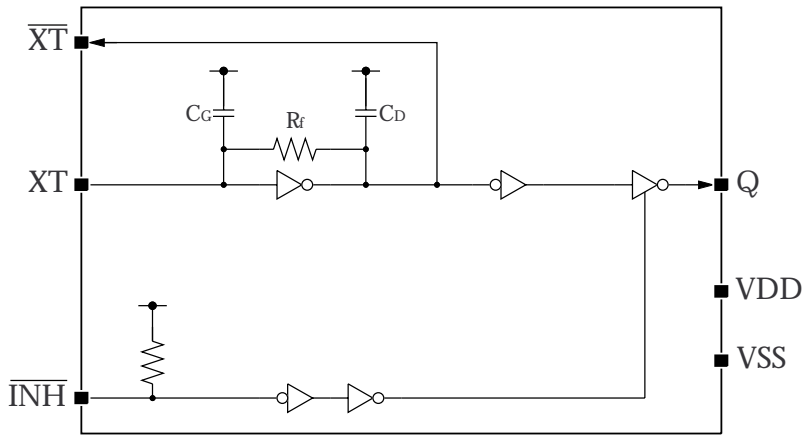
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PACKAGE DIMENSIONS (6 pin SOT)

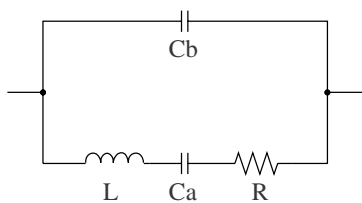


(Unit:mm)

BLOCK DIAGRAM



Current consumption and Output waveform with NPC's standard crystal.



f (MHz)	R (Ω)	L (mH)	C_a (pF)	C_b (pF)
30	18.62	16.24	1.733	5.337
40	20.53	11.34	1.396	3.989
50	22.17	7.40	1.370	4.105
60	22.20	5.05	1.388	4.226
70	25.42	4.18	1.254	5.170

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SPECIFICATIONS

Absolute Maximum Ratings

(V_{SS} = 0V unless otherwise noted)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V _{DD}		-0.5 to 7.0	V
Input voltage range	V _{IN}		-0.5 to V _{DD} + 0.5	V
Output voltage range	V _{OUT}		-0.5 to V _{DD} + 0.5	V
Storage temperature ranges	T _{STG}	Chip form	-65 to 150	°C
		6 pin SOT	-55 to 125	°C
Power dissipation	P _w	6 pin SOT	250	mW
Output current	I _{OUT}		13	mA
Soldering temperature	T _{SLD}	6 pin SOT	255	°C
Soldering time	t _{SLD}	6 pin SOT	10	sec

Recommended Operating Conditions

(V_{SS} = 0V unless otherwise noted)

Parameter	Symbol	Condition	Limit			Unit
			MIN	TYP	MAX	
Supply Voltage	V _{DD}		4.5		5.5	V
Input voltage	V _{IN}		V _{SS}		V _{DD}	V
Operating temperature	T _{OPR}		-20		+80	°C

Electrical Characteristics

(V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, T_a = -20 to 80°C, unless otherwise noted)

Parameter	Symbol	Condition	Limit			Unit
			MIN	TYP	MAX	
HIGH-level output voltage	V _{OH}	Q pin, test circuit 1, V _{DD} = 4.5V, I _{OH} = 8mA	3.9	4.2		V
LOW-level output voltage	V _{OL}	Q pin, test circuit 2, V _{DD} = 4.5V, I _{OL} = 8mA		0.3	0.4	V
Output leakage current	I _Z	Q pin, test circuit 2, V _{OH} = V _{DD}			10	μA
		$\overline{\text{INH}}$ = Low, V _{DD} = 5.5V, V _{OL} = V _{SS}			10	μA
HIGH-level input voltage	V _{IH}	$\overline{\text{INH}}$ pin	2.0			V
LOW-level input voltage	V _{IL}	$\overline{\text{INH}}$ pin			0.8	V
Current consumption	I _{DD}	$\overline{\text{INH}}$ = OPEN, test circuit 3, C _L = 15pF, f = 70MHz		28	45	mA
		SM5003A×H load circuit 1 SM5003B×H load circuit 2		28	45	mA
Pull-up resistance	R _{UP}	$\overline{\text{INH}}$ pin, test circuit 4	25	100	250	kΩ
AC feedback resistance	R _f	test circuit 5				
		SM5003×AH	5.4	6.1	6.7	kΩ
		SM5003×BH	2.9	3.3	3.7	kΩ
		SM5003×CH	3.5	3.9	4.3	kΩ
Internal capacitance	C _G C _D	Design value, determined by the internal wafer pattern	7.2	8	8.8	pF
			13.5	15	16.5	pF

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Switching Characteristics

Duty level CMOS (SM5003A×H)

(V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, T_a = -20 to 80°C, unless otherwise noted)

Parameter	Symbol	Conditions	Limit			Unit
			MIN	TYP	MAX	
Output rise time	tr	Test circuit 6, load circuit 1, C_L = 15pF 0.1V _{DD} to 0.9V _{DD}		3.5	7	ns
Output fall time	tr	Test circuit 6, load circuit 1, C_L = 15pF 0.9V _{DD} to 0.1V _{DD}		3.5	7	ns
Output duty cycle	DUTY	Test circuit 6, T_a = 25°C, V_{DD} =5.0V load circuit 1, C_L = 15pF, f= 70MHz (*1)	45		55	%
Output disable delay time	tPLZ	Test circuit 6, T_a = 25°C, V_{DD} = 5.0V load circuit 1, C_L = 15pF			100	ns
Output enable delay time	tPZL				100	ns

Duty level TTL (SM5003B×H)

(V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, T_a = -20 to 80°C, unless otherwise noted)

Parameter	Symbol	Condition	Limit			Unit
			MIN	TYP	MAX	
Output rise time	tr	Test circuit 6, load circuit 2, C_L = 15pF 0.4V _{DD} to 2.4V _{DD}		2.5	7	ns
Output fall time	tr	Test circuit 6, load circuit 2, C_L = 15pF 2.4V _{DD} to 0.4V _{DD}		2.5	7	ns
Output duty cycle	DUTY	Test circuit 6, T_a = 25°C, V_{DD} =5.0V load circuit 2, C_L = 15pF, f= 70MHz (*1)	45		55	%
Output disable delay time	tPLZ	Test circuit 6, T_a = 25°C, V_{DD} = 5.0V load circuit 2, C_L = 15pF			100	ns
Output enable delay time	tPZL				100	ns

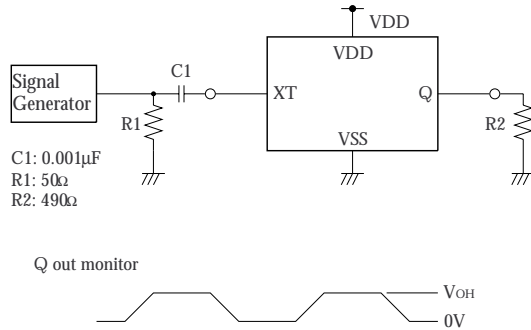
Note:

(*1) Determined by the lot. monitor.

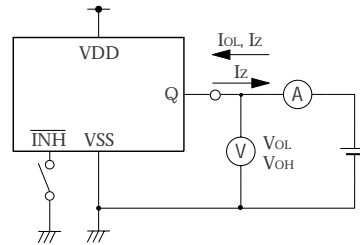
TEST CIRCUITS

Test Circuit 1

3.5 V_{P-P}, 10MHz sine wave input signal

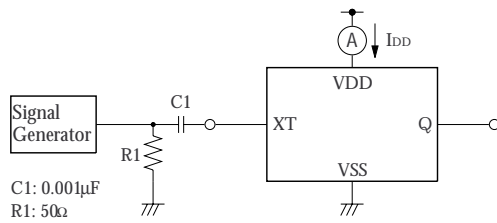


Test Circuit 2

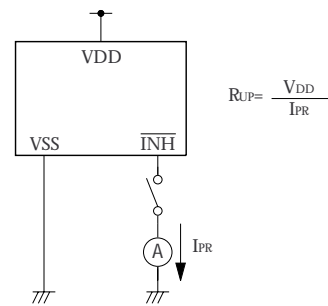


Test Circuit 3

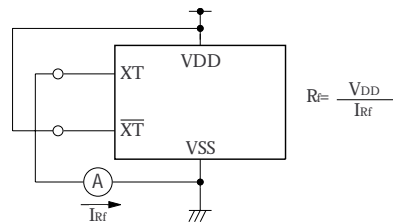
3.5 V_{P-P}, 70MHz sine wave input signal



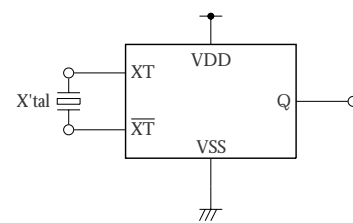
Test Circuit 4



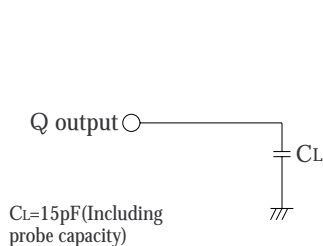
Test Circuit 5



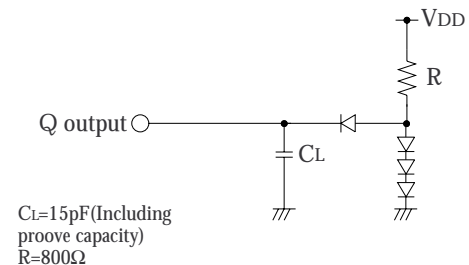
Test Circuit 6



Load Circuit 1



Load Circuit 2

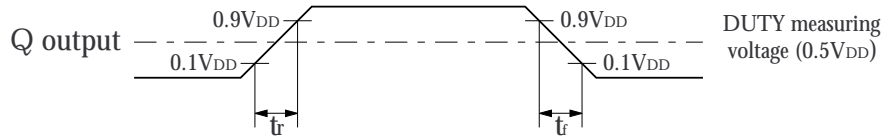


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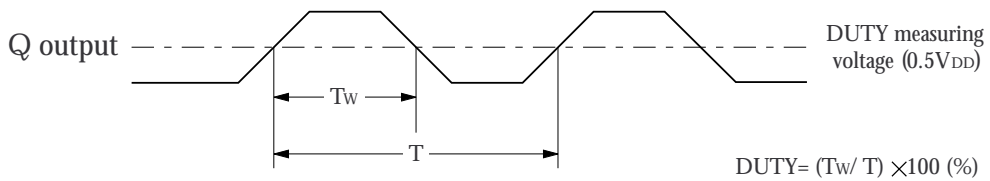
Switching Time Test Waveforms

Duty level CMOS (SM5003A×H)

tr,tf DUTY

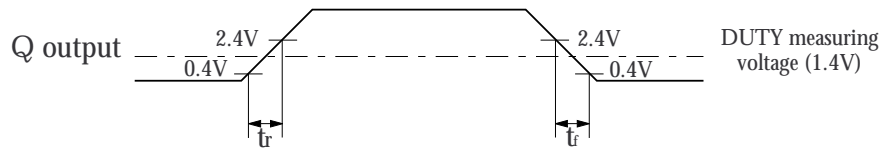


Output duty cycle time

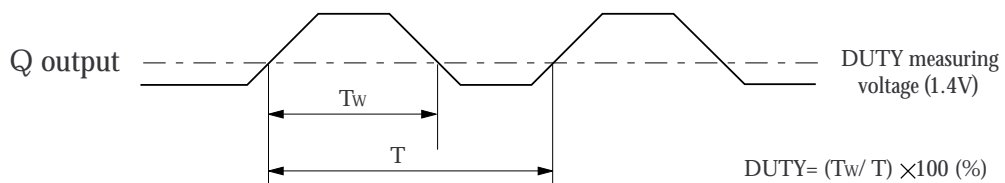


Duty level TTL (SM5003B×H)

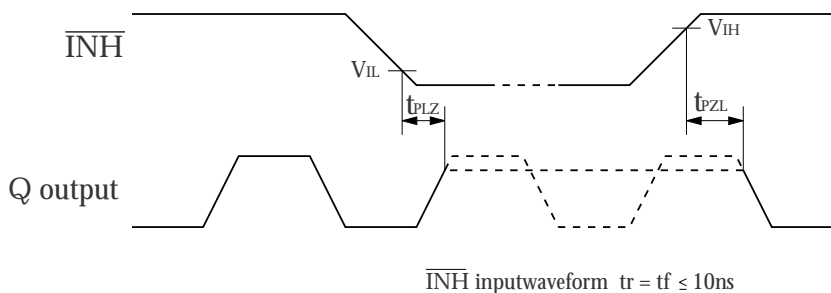
tr,tf DUTY



Output duty cycle time



Output Disable/Enable Delay Times



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