Features

- Core
  - ARM® Cortex®-M3 revision 2.0 running at up to 96 MHz
  - Memory Protection Unit (MPU)
  - Thumb®-2 instruction set
- Memories
  - From 64 to 256 Kbytes embedded Flash, 128-bit wide access, memory accelerator, dual bank
  - From 16 to 48 Kbytes embedded SRAM with dual banks
  - 16 Kbytes ROM with embedded bootloader routines (UART, USB) and IAP routines
  - Static Memory Controller (SMC): SRAM, NOR, NAND support. NAND Flash controller with 4 Kbytes RAM buffer and ECC
- System
  - Embedded voltage regulator for single supply operation
  - POR, BOD and Watchdog for safe reset
  - Quartz or resonator oscillators: 3 to 20 MHz main and optional low power 32.768 kHz for RTC or device clock.
  - High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz Default Frequency for fast device startup
  - Slow Clock Internal RC oscillator as permanent clock for device clock in low power mode
  - One PLL for device clock and one dedicated PLL for USB 2.0 High Speed Device
  - Up to 17 peripheral DMA (PDC) channels and 4-channel central DMA
- Low Power Modes
  - Sleep and Backup modes, down to 2.5 µA in Backup mode
  - Backup domain: VDDBU pin, RTC, 32 backup registers
  - Ultra low power RTC: 0.6 µA
- Peripherals
  - USB 2.0 Device: 480 Mbps, 4-kbyte FIFO, up to 7 bidirectional Endpoints, dedicated DMA
  - Up to 4 USARTs (ISO7816, IrDA®, Flow Control, SPI, Manchester support) and one UART
  - Up to 2 TWI (I2C compatible), 1 SPI, 1 SSC (I2S), 1 HSMCI (SDIO/SD/MMC)
  - 3-Channel 16-bit Timer/Counter (TC) for capture, compare and PWM
  - 4-channel 16-bit PWM (PWMC)
  - 32-bit Real Time Timer (RTT) and RTC with calendar and alarm features
  - 8-channel 12-bit 1MSPS ADC with differential input mode and programmable gain stage, 8-channel 10-bit ADC
- I/O
  - Up to 96 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination
  - Three 32-bit Parallel Input/Outputs (PIO)
- Packages
  - 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm
  - 100-ball LFBGA, 9 x 9 mm, pitch 0.8 mm
  - 144-lead LQFP, 20 x 20 mm, pitch 0.5 mm
  - 144-ball LFBGA, 10 x 10 mm, pitch 0.8 mm

AT91ARM Cortex M3-based Microcontrollers

ATSAM3U Series

Preliminary

Summary

NOTE: This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

6430CS–ATARM–09-Apr-10

1. SAM3U Description

Atmel's SAM3U series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM Cortex-M3 RISC processor. It operates at a maximum speed of 96 MHz and features up to 256 Kbytes of Flash and up to 52 Kbytes of SRAM. The peripheral set includes a High Speed USB Device port with embedded transceiver, a High Speed MCI for SDIO/SD/MMC, an External Bus Interface with NAND Flash controller, up to 4xUSARTs (SAM3U1C/2C/4C have 3), up to 2xTWIs (SAM3U1C/2C/4C have 1), up to 5xSPIs SAM3U1C/2C/4C have 4), as well as 4xPWM timers, 3xgeneral purpose 16-bit timers, an RTC, a 12-bit ADC and a 10-bit ADC.

The SAM3U architecture is specifically designed to sustain high speed data transfers. It includes a multi-layer bus matrix as well as multiple SRAM banks, PDC and DMA channels that enable it to run tasks in parallel and maximize data throughput.

It can operate from 1.62V to 3.6V and comes in 100-pin and 144-pin LQFP and BGA packages.

The SAM3U device is particularly well suited for USB applications: data loggers, PC peripherals and any high speed bridge (USB to SDIO, USB to SPI, USB to External Bus Interface).

1.1 Configuration Summary

The SAM3U series differ in memory sizes, package and features list. Table 1-1 summarizes the configurations of the six devices.

Table 1-1. Configuration Summary

Device	Flash	Flash Organization	SRAM	Number of PIOs	Number of USARTs	Number of TWI	FWUP, SHDN pins	External Bus Interface	HSMCI data size	Package	ADC
SAM3U4E	2x128 Kbytes	dual plane	52 Kbytes	96	4	2	Yes	8 or 16 bits, 4 chip selects, 24-bit address	8 bits	LQFP144 BGA144	2 (8+ 8 channels)
SAM3U2E	128 Kbytes	single plane	36 Kbytes	96	4	2	Yes	8 or 16 bits, 4 chip selects 24-bit address	8 bits	LQFP144 BGA144	2 (8+ 8 channels)
SAM3U1E	64 Kbytes	single plane	20 Kbytes	96	4	2	Yes	8 or 16 bits, 4 chip selects, 24-bit address	8 bits	LQFP144 BGA144	2 (8+ 8 channels)
SAM3U4C	2 x 128 Kbytes	dual plane	52 Kbytes	57	3	1	FWUP	8 bits, 2 chip selects, 8-bit address	4 bits	LQFP100 BGA100	2 (4+ 4 channels)
SAM3U2C	128 Kbytes	single plane	36 Kbytes	57	3	1	FWUP	8 bits, 2 chip selects, 8-bit address	4 bits	LQFP100 BGA100	2 (4+ 4 channels)
SAM3U1C	64 Kbytes	single plane	20 Kbytes	57	3	1	FWUP	8 bits 2 chip selects, 8-bit address	4 bits	LQFP100 BGA100	2 (4+ 4 channels)

Note: 1. The SRAM size takes into account the 4-Kbyte RAM buffer of the NAND Flash Controller (NFC) which can be used by the core if not used by the NFC.

2. SAM3U Block Diagram

Figure 2-1. 144-pin SAM3U4/2/1E Block Diagram

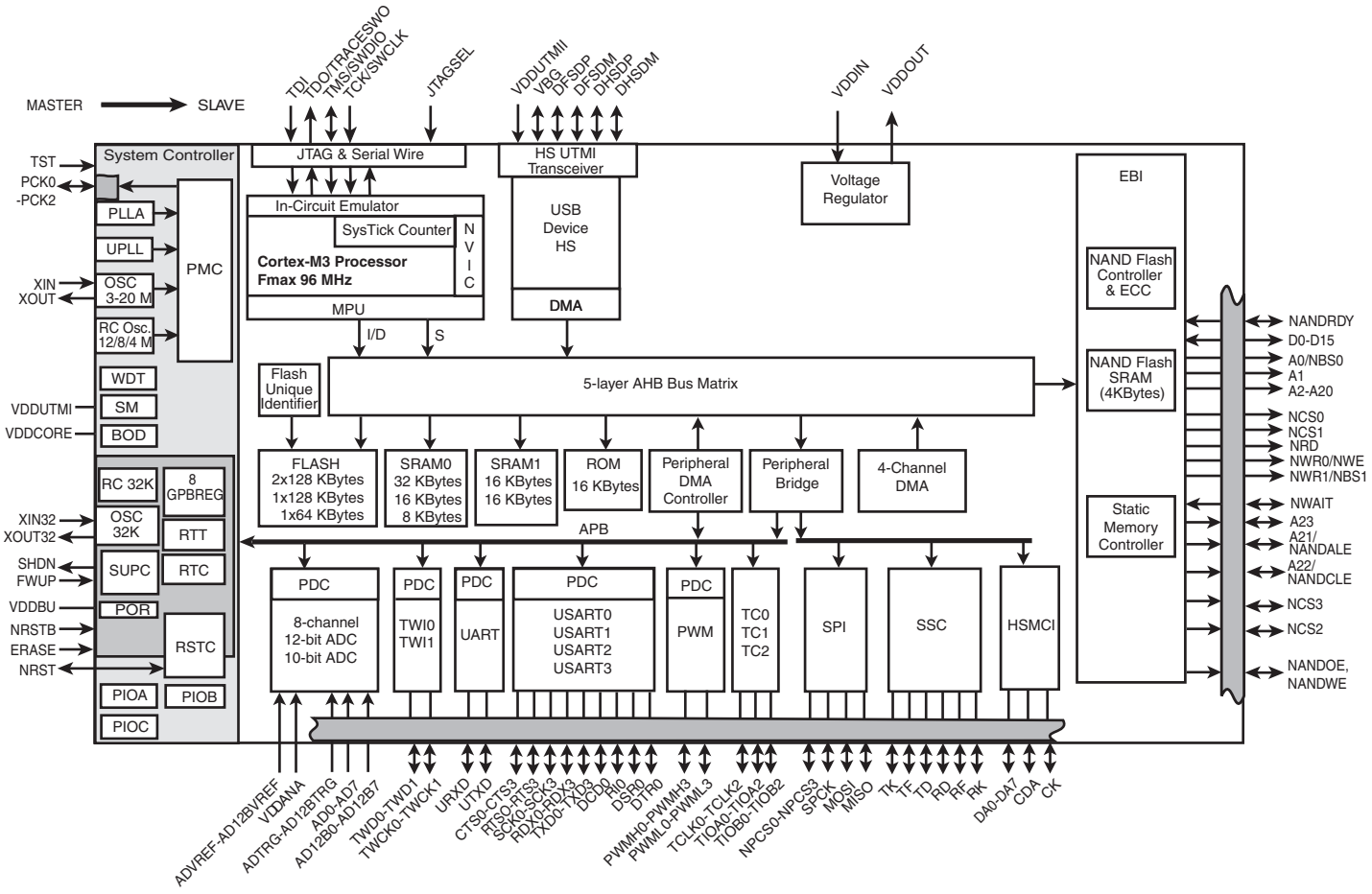
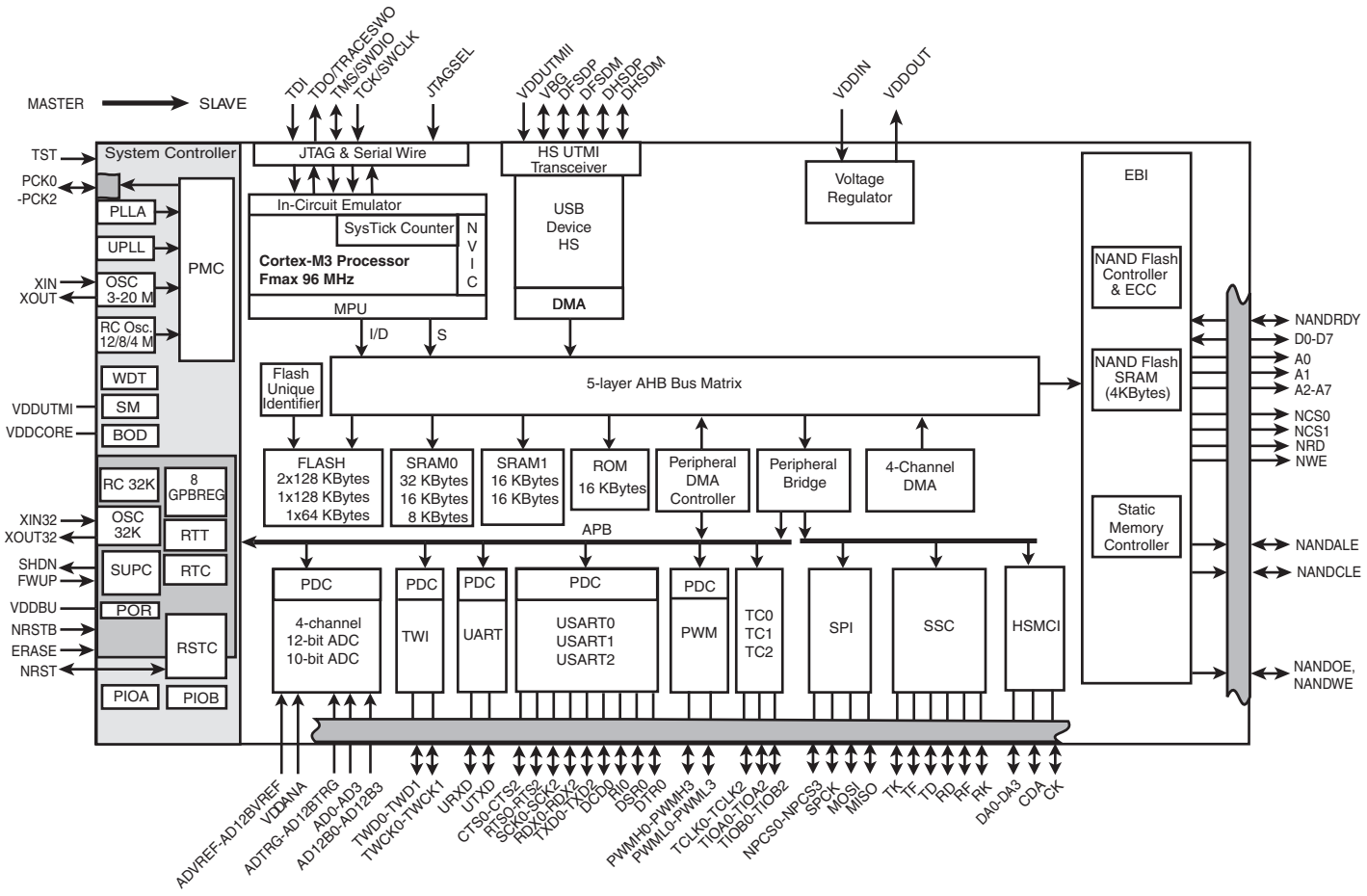


Figure 2-2. 100-pin SAM3U4/2/1C Block Diagram



3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines Power Supply	Power			1.62V to 3.6V
VDDIN	Voltage Regulator Input	Power			1.8V to 3.6V
VDDOUT	Voltage Regulator Output	Power			1.8V
VDDUTMII	USB UTMI+ Interface Power Supply	Power			3.0V to 3.6V
GNDUTMII	USB UTMI+ Interface Ground	Ground			
VDDBU	Backup I/O Lines Power Supply	Power			1.62V to 3.6V
GNDBU	Backup Ground	Ground			
VDDPLL	PLL A, UPLL and OSC 3-20 MHz Power Supply	Power			1.62 V to 1.95V
GNDPLL	PLL A, UPLL and OSC 3-20 MHz Ground	Ground			
VDDANA	ADC Analog Power Supply	Power			2.0V to 3.6V
GNDANA	ADC Analog Ground	Ground			
VDDCORE	Core, Memories and Peripherals Chip Power Supply	Power			1.62V to 1.95V
GND	Ground	Ground			
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input		VDDPLL	
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input		VDDBU	
XOUT32	Slow Clock Oscillator Output	Output			
VBG	Bias Voltage Reference	Analog			
PCK0 - PCK2	Programmable Clock Output	Output		VDDIO	
Shutdown, Wakeup Logic					
SHDN	Shut-Down Control	Output		VDDBU	push/pull 0: The device is in backup mode 1: The device is running (not in backup mode)
FWUP	Force Wake-Up Input	Input	Low		Needs external pull-up
Serial Wire/JTAG Debug Port (SWJ-DP)					
TCK/SWCLK	Test Clock/Serial Wire Clock	Input		VDDIO	No pull-up resistor
TDI	Test Data In	Input			No pull-up resistor
TDO/TRACESWO	Test Data Out/Trace Asynchronous Data Out	Output			
TMS/SWDIO	Test Mode Select/Serial Wire Input/Output	Input			No pull-up resistor
JTAGSEL	JTAG Selection	Input	High	VDDBU	Internal permanent pull-down

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDBU	Internal permanent 15K pulldown
Reset/Test					
NRST	Microcontroller Reset	I/O	Low	VDDIO	Internal permanent pullup
NRSTB	Asynchronous Microcontroller Reset	Input	Low	VDDBU	Internal permanent pullup
TST	Test Select	Input			Internal permanent pulldown
Universal Asynchronous Receiver Transceiver - UART					
URXD	UART Receive Data	Input			
UTXD	UART Transmit Data	Output			
PIO Controller - PIOA - PIOB - PIOC					
PA0 - PA31	Parallel IO Controller A	I/O		VDDIO	•Schmitt Trigger [1] Reset State: •PIO Input •Internal pullup enabled
PB0 - PB31	Parallel IO Controller B	I/O			•Schmitt Trigger [2] Reset State: •PIO Input •Internal pullup enabled
PC0 - PC31	Parallel IO Controller C	I/O			•Schmitt Trigger[3] Reset State: •PIO Input •Internal pullup enabled
External Bus Interface					
D0 - D15	Data Bus	I/O			
A0 - A23	Address Bus	Output			
NWAIT	External Wait Signal	Input	Low		
Static Memory Controller - SMC					
NCS0 - NCS3	Chip Select Lines	Output	Low		
NWR0 - NWR1	Write Signal	Output	Low		
NRD	Read Signal	Output	Low		
NWE	Write Enable	Output	Low		
NBS0 - NBS1	Byte Mask Signal	Output	Low		
NAND Flash Controller - NFC					
NANDOE	NAND Flash Output Enable	Output	Low		
NANDWE	NAND Flash Write Enable	Output	Low		
NANDRDY	NAND Ready	Input			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
High Speed Multimedia Card Interface - HSMCI					
CK	Multimedia Card Clock	I/O			
CDA	Multimedia Card Slot A Command	I/O			
DA0 - DA7	Multimedia Card Slot A Data	I/O			
Universal Synchronous Asynchronous Receiver Transmitter - USARTx					
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	I/O			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			
DTR0	USART0 Data Terminal Ready	I/O			
DSR0	USART0 Data Set Ready	Input			
DCD0	USART0 Data Carrier Detect	Input			
RI0	USART0 Ring Indicator	Input			
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output			
RD	SSC Receive Data	Input			
TK	SSC Transmit Clock	I/O			
RK	SSC Receive Clock	I/O			
TF	SSC Transmit Frame Sync	I/O			
RF	SSC Receive Frame Sync	I/O			
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Pulse Width Modulation Controller- PWMC					
PWMHx	PWM Waveform Output High for channel x	Output			
PWMLx	PWM Waveform Output Low for channel x	Output			only output in complementary mode when dead time insertion is enabled
PWMFI0-2	PWM Fault Input	Input			
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
NPCS1 - NPCS3	SPI Peripheral Chip Select	Output	Low		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Two-Wire Interface - TWI					
TWDx	TWIx Two-wire Serial Data	I/O			
TWCKx	TWIx Two-wire Serial Clock	I/O			
12-bit Analog-to-Digital Converter - ADC12B					
AD12Bx	Analog Inputs	Analog			
AD12BTRG	ADC Trigger	Input			
AD12BVREF	ADC Reference	Analog			
10-bit Analog-to-Digital Converter - ADC					
ADx	Analog Inputs	Analog			
ADTRG	ADC Trigger	Input			
ADVREF	ADC Reference	Analog			
Fast Flash Programming Interface - FFPI					
PGMEN0-PGMEN2	Programming Enabling	Input		VDDIO	
PGMM0-PGMM3	Programming Mode	Input			
PGMD0-PGMD15	Programming Data	I/O			
PGMRDY	Programming Ready	Output	High		
PGMNVALID	Data Direction	Output	Low		
PGMNOE	Programming Read	Input	Low		
PGMCK	Programming Clock	Input			
PGMNCMD	Programming Command	Input	Low		
USB High Speed Device - UDPHS					
DFSDM	USB Device Full Speed Data -	Analog		VDDUTMII	
DFSDP	USB Device Full Speed Data +	Analog			
DHSDM	USB Device High Speed Data -	Analog			
DHSDP	USB Device High Speed Data +	Analog			

Notes: 1. PIOA: Schmitt Trigger on all except PA14 on 100 and 144 packages.
2. PIOB: Schmitt Trigger on all except PB9 to PB16, PB25 to PB31 on 100 and 144 packages.
3. PIOC: Schmitt Trigger on all except PC20 to PC27 on 144 package.

3.1 Design Considerations

In order to facilitate schematic capture when using a SAM3U design, Atmel provides a “Schematics Checklist” Application note.

Please visit http://www.atmel.com/products/AT91/ for additional documentation.

4. Package and Pinout

The SAM3U4/2/1E is available in 144-lead LQFP and 144-ball LFBGA packages.

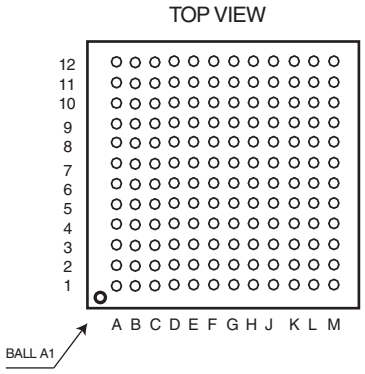
The SAM3U4/2/1C is available in 100-lead LQFP and 100-ball LFBGA packages.

4.1 SAM3U4/2/1E Package and Pinout

4.1.1 144-ball LFBGA Package Outline

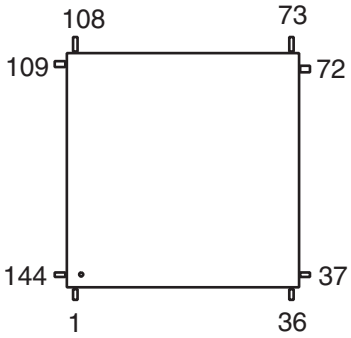
The 144-Ball LFBGA package has a 0.8 mm ball pitch and respects Green Standards. Its dimensions are 10 x 10 x 1.4 mm.

Figure 4-1. Orientation of the 144-ball LFBGA Package



4.1.2 144-lead LQFP Package Outline

Figure 4-2. Orientation of the 144-lead LQFP Package



4.1.3 144-lead LQFP Pinout

Table 4-1. 144-pin SAM3U4/2/1E Pinout

1	TDI	37	DHSDP	73	VDDANA	109	PA0/PGMNCMD
2	VDDOUT	38	DHSDM	74	ADVREF	110	PC0
3	VDDIN	39	VBG	75	GNDANA	111	PA1/PGMRDY
4	TDO/TRACESWO	40	VDDUTMI	76	AD12BVREF	112	PC1
5	PB31	41	DFSDM	77	PA22/PGMD14	113	PA2/PGMNOE
6	PB30	42	DFSDP	78	PA30	114	PC2
7	TMS/SWDIO	43	GNDUTMI	79	PB3	115	PA3/PGMNVALID
8	PB29	44	VDDCORE	80	PB4	116	PC3
9	TCK/SWCLK	45	PA28	81	PC15	117	PA4/PGMM0
10	PB28	46	PA29	82	PC16	118	PC4
11	NRST	47	PC22	83	PC17	119	PA5/PGMM1
12	PB27	48	PA31	84	PC18	120	PC5
13	PB26	49	PC23	85	VDDIO	121	PA6/PGMM2
14	PB25	50	VDDCORE	86	VDDCORE	122	PC6
15	PB24	51	VDDIO	87	PA13/PGMD5	123	PA7/PGMM3
16	VDDCORE	52	GND	88	PA14/PGMD6	124	PC7
17	VDDIO	53	PB0	89	PC10	125	VDDCORE
18	GND	54	PC24	90	GND	126	GND
19	PB23	55	PB1	91	PA15/PGMD7	127	VDDIO
20	PB22	56	PC25	92	PC11	128	PA8/PGMD0
21	PB21	57	PB2	93	PA16/PGMD8	129	PC8
22	PC21	58	PC26	94	PC12	130	PA9/PGMD1
23	PB20	59	PB11	95	PA17/PGMD9	131	PC9
24	PB19	60	GND	96	PB16	132	PA10/PGMD2
25	PB18	61	PB12	97	PB15	133	PA11/PGMD3
26	PB17	62	PB13	98	PC13	134	PA12/PGMD4
27	VDDCORE	63	PC27	99	PA18/PGMD10	135	FWUP
28	PC14	64	PA27	100	PA19/PGMD11	136	SHDN
29	PB14	65	PB5	101	PA20/PGMD12	137	ERASE
30	PB10	66	PB6	102	PA21/PGMD13	138	TST
31	PB9	67	PB7	103	PA23/PGMD15	139	VDDBU
32	PC19	68	PB8	104	VDDIO	140	GNDBU
33	GNDPLL	69	PC28	105	PA24	141	NRSTB
34	VDDPLL	70	PC29	106	PA25	142	JTAGSEL
35	XOUT	71	PC30	107	PA26	143	XOUT32
36	XIN	72	PC31	108	PC20	144	XIN32

4.1.4 144-ball LFBGA Pinout

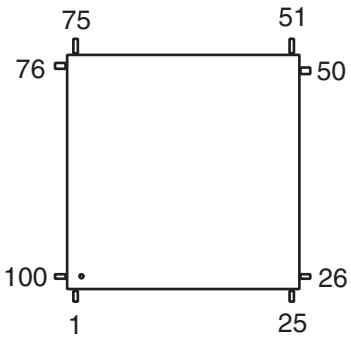
Table 4-2. 144-ball SAM3U4/2/1E Pinout

A1	VBG	D1	DFSDM	G1	PB0	K1	PB7
A2	VDDUTMI	D2	DHSDM	G2	PC26	K2	PC31
A3	PB9	D3	GNDPLL	G3	PB2	K3	PC29
A4	PB10	D4	PC14	G4	PC25	K4	PB3
A5	PB19	D5	PB21	G5	PB1	K5	PB4
A6	PC21	D6	PB23	G6	GND	K6	PA14/PGMD6
A7	PB26	D7	PB24	G7	GND	K7	PA16/PGMD8
A8	TCK/SWCLK	D8	PB28	G8	VDDCORE	K8	PA18/PGMD10
A9	PB30	D9	TDI	G9	PC4	K9	PC20
A10	TDO/TRACESWO	D10	VDDBU	G10	PA6/PGMM2	K10	PA1/PGMRDY
A11	XIN32	D11	PA10/PGMD2	G11	PA7/PGMM3	K11	PC1
A12	XOUT32	D12	PA11/PGMD3	G12	PC6	K12	PC2
B1	VDDCORE	E1	PC22	H1	PC24	L1	PC30
B2	GNDUTMI	E2	PA28	H2	PC27	L2	ADVREF
B3	XOUT	E3	PC19	H3	PA27	L3	AD12BVREF
B4	PB14	E4	VDDCORE	H4	PB12	L4	PA22/PGMD14
B5	PB17	E5	GND	H5	PB11	L5	PC17
B6	PB22	E6	VDDIO	H6	GND	L6	PC10
B7	PB25	E7	GNDBU	H7	VDDCORE	L7	PC12
B8	PB29	E8	NRST	H8	PB16	L8	PA19/PGMD11
B9	VDDIN	E9	PB31	H9	PB15	L9	PA23/PGMD15
B10	JTAGSEL	E10	PA12/PGMD4	H10	PC3	L10	PA0/PGMNCMD
B11	ERASE	E11	PA8/PGMD0	H11	PA5/PGMM1	L11	PA26
B12	SHDN	E12	PC8	H12	PC5	L12	PC0
C1	DFSDP	F1	PA31	J1	PB5	M1	VDDANA
C2	DHSDP	F2	PA29	J2	PB6	M2	GNDANA
C3	XIN	F3	PC23	J3	PC28	M3	PA30
C4	VDDPLL	F4	VDDCORE	J4	PB8	M4	PC15
C5	PB18	F5	VDDIO	J5	PB13	M5	PC16
C6	PB20	F6	GND	J6	VDDIO	M6	PC18
C7	PB27	F7	GND	J7	PA13/PGMD5	M7	PA15/PGMD7
C8	TMS/SWDIO	F8	VDDIO	J8	PA17/PGMD9	M8	PC11
C9	VDDOUT	F9	PC9	J9	PC13	M9	PA20/PGMD12
C10	NRSTB	F10	PA9/PGMD1	J10	PA2/PGMNOE	M10	PA21/PGMD13
C11	TST	F11	VDDCORE	J11	PA3/PGMNVALID	M11	PA24
C12	FWUP	F12	PC7	J12	PA4/PGMM0	M12	PA25

4.2 SAM3U4/2/1C Package and Pinout

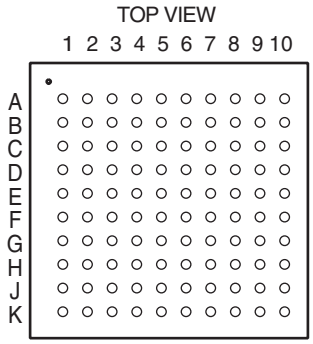
4.2.1 100-lead LQFP Package Outline

Figure 4-3. Orientation of the 100-lead LQFP Package



4.2.2 100-ball LFBGA Package Outline

Figure 4-4. Orientation of the 100-ball LFBGA Package



4.2.3 100-lead LQFP Pinout

Table 4-3. 100-pin SAM3U4/2/1C1 Pinout

1	VDDANA	26	PA0/PGMNCMD	51	TDI	76	DHSDP
2	ADVREF	27	PA1/PGMRDY	52	VDDOUT	77	DHSDM
3	GNDANA	28	PA2/PGMNOE	53	VDDIN	78	VBG
4	AD12BVREF	29	PA3/PGMNVALID	54	TDO/TRACESWO	79	VDDUTMI
5	PA22/PGMD14	30	PA4/PGMM0	55	TMS/SWDIO	80	DFSDM
6	PA30	31	PA5/PGMM1	56	TCK/SWCLK	81	DFSDP
7	PB3	32	PA6/PGMM2	57	NRST	82	GNDUTMI
8	PB4	33	PA7/PGMM3	58	PB24	83	VDDCORE
9	VDDCORE	34	VDDCORE	59	VDDCORE	84	PA28
10	PA13/PGMD5	35	GND	60	VDDIO	85	PA29
11	PA14/PGMD6	36	VDDIO	61	GND	86	PA31
12	PA15/PGMD7	37	PA8/PGMD0	62	PB23	87	VDDCORE
13	PA16/PGMD8	38	PA9/PGMD1	63	PB22	88	VDDIO
14	PA17/PGMD9	39	PA10/PGMD2	64	PB21	89	GND
15	PB16	40	PA11/PGMD3	65	PB20	90	PB0
16	PB15	41	PA12/PGMD4	66	PB19	91	PB1
17	PA18/PGMD10	42	FWUP	67	PB18	92	PB2
18	PA19/PGMD11	43	ERASE	68	PB17	93	PB11
19	PA20/PGMD12	44	TST	69	PB14	94	PB12
20	PA21/PGMD13	45	VDDBU	70	PB10	95	PB13
21	PA23/PGMD15	46	GNDBU	71	PB9	96	PA27
22	VDDIO	47	NRSTB	72	GNDPLL	97	PB5
23	PA24	48	JTAGSEL	73	VDDPLL	98	PB6
24	PA25	49	XOUT32	74	XOUT	99	PB7
25	PA26	50	XIN32	75	XIN	100	PB8

4.2.4 100-ball LFBGA Pinout

Table 4-4. 100-ball SAM3U4/2/1C Pinout

A1	VBG	C6	PB22	F1	PB1	H6	PA15/PGMD7
A2	XIN	C7	TMS/SWDIO	F2	PB12	H7	PA18/PGMD10
A3	XOUT	C8	NRSTB	F3	VDDIO	H8	PA24
A4	PB17	C9	JTAGSEL	F4	PA31	H9	PA1/PGMRDY
A5	PB21	C10	VDDBU	F5	VDDIO	H10	PA2/PGMNOE
A6	PB23	D1	DFSDM	F6	GND	J1	PB6
A7	TCK/SWCLK	D2	DHSDM	F7	PB16	J2	PB8
A8	VDDIN	D3	VDDPLL	F8	PA6/PGMM2	J3	ADVREF
A9	VDDOUT	D4	VDDCORE	F9	VDDCORE	J4	PA30
A10	XIN32	D5	PB20	F10	PA7/PGMM3	J5	PB3
B1	VDDCORE	D6	ERASE	G1	PB11	J6	PA16/PGMD8
B2	GNDUTMI	D7	TST	G2	PB2	J7	PA19/PGMD11
B3	VDDUTMI	D8	FWUP	G3	PB0	J8	PA21/PGMD13
B4	PB10	D9	PA11/PGMD3	G4	PB13	J9	PA26
B5	PB18	D10	PA12/PGMD4	G5	VDDCORE	J10	PA0/PGMNCMD
B6	PB24	E1	PA29	G6	GND	K1	PB7
B7	NRST	E2	GND	G7	PB15	K2	VDDANA
B8	TDO/TRACESWO	E3	PA28	G8	PA3/PGMNVALID	K3	GNDANA
B9	TDI	E4	PB9	G9	PA5/PGMM1	K4	AD12BVREF
B10	XOUT32	E5	GNDBU	G10	PA4/PGMM0	K5	PB4
C1	DFSDP	E6	VDDIO	H1	VDDCORE	K6	PA14/PGMD6
C2	DHSDP	E7	VDDCORE	H2	PB5	K7	PA17/PGMD9
C3	GNDPLL	E8	PA10/PGMD2	H3	PA27	K8	PA20/PGMD12
C4	PB14	E9	PA9/PGMD1	H4	PA22/PGMD14	K9	PA23/PGMD15
C5	PB19	E10	PA8/PGMD0	H5	PA13/PGMD5	K10	PA25

5. Power Considerations

5.1 Power Supplies

The SAM3U product has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals; voltage ranges from 1.62V to 1.95V.
- VDDIO pins: Power the Peripherals I/O lines; voltage ranges from 1.62V to 3.6V.
- VDDIN pin: Powers the Voltage regulator
- VDDOUT pin: It is the output of the voltage regulator.
- VDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage ranges from 1.62V to 3.6V. VDDBU must be supplied before or at the same time than VDDIO and VDDCORE.
- VDDPLL pin: Powers the PLL A, UPLL and 3-20 MHz Oscillator; voltage ranges from 1.62V to 1.95V.
- VDDUTMI pin: Powers the UTMI+ interface; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDANA pin: Powers the ADC cells; voltage ranges from 2.0V to 3.6V.

Ground pins GND are common to VDDCORE and VDDIO pins power supplies.

Separated ground pins are provided for VDDBU, VDDPLL, VDDUTMI and VDDANA. These ground pins are respectively GNDBU, GNDPLL, GNDUTMI and GNDANA.

5.2 Voltage Regulator

The SAM3U embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3U but can be used to supply other parts in the application. It features two different operating modes:

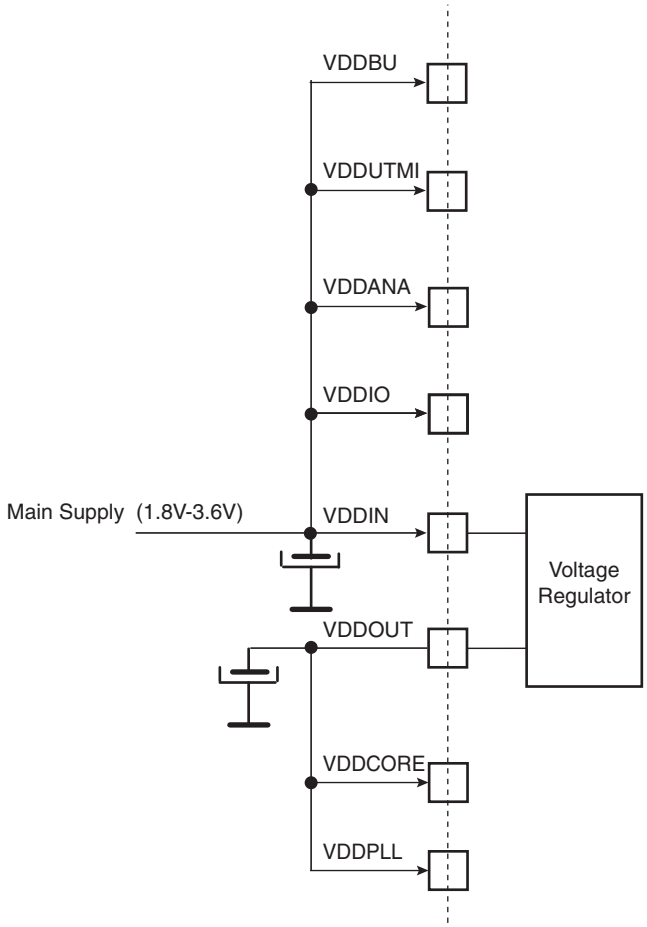
- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 150 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode or when the output current is low, quiescent current is only 7µA.
- In Shutdown mode, the voltage regulator consumes less than 1 µA while its output is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is inferior to 400 µs.

For adequate input and output power supply decoupling/bypassing, refer to “Voltage Regulator” in the “Electrical Characteristics” section of the product datasheet.

5.3 Typical Powering Schematics

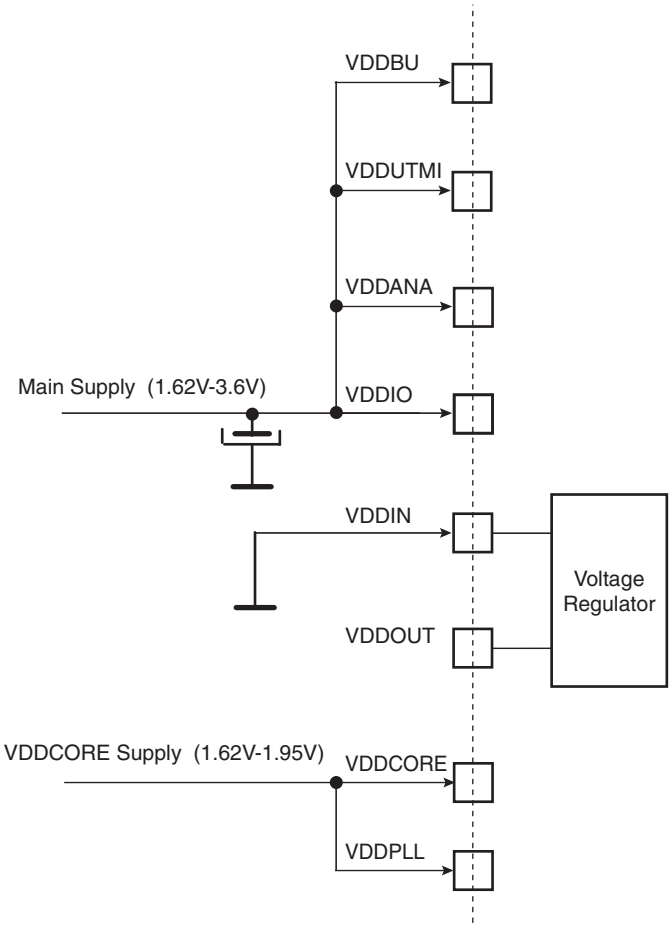
The SAM3U supports a 1.8V-3.6V single supply mode. The internal regulator input connected to the source and its output feed VDDCORE. Figure 5-1, Figure 5-2, Figure 5-3 show the power schematics.

Figure 5-1. Single Supply



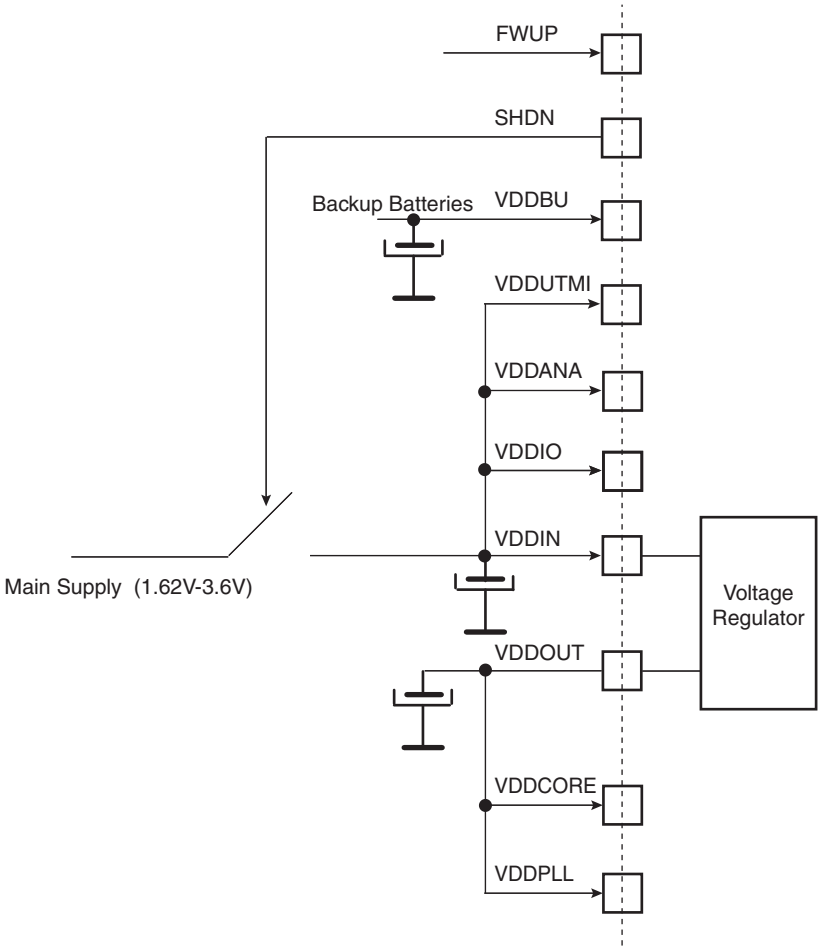
Note: Restrictions
With Main Supply < 2.0 V, USB and ADC are not usable.
With Main Supply ≥ 2.4V and < 3V, USB is not usable.
With Main Supply ≥ 3V, all peripherals are usable.

Figure 5-2. Core Externally Supplied



Note: Restrictions
With Main Supply < 2.0 V, USB and ADC are not usable.
With Main Supply ≥ 2.4V and < 3V, USB is not usable.
With Main Supply ≥ 3V, all peripherals are usable.

Figure 5-3. Backup Batteries Used



Note: Restrictions
With Main Supply < 2.0 V, USB and ADC are not usable.
With Main Supply ≥ 2.4V and < 3V, USB is not usable.
With Main Supply ≥ 3V, all peripherals are usable.

5.4 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.5 Low Power Modes

The various low power modes of the SAM3U are described below:

5.5.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time (<0.5ms).

The Supply Controller, zero-power power-on reset, RTT, RTC, Backup registers and 32 kHz Oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

Backup Mode is based on the Cortex-M3 deep-sleep mode with the voltage regulator disabled.

The SAM3U Series can be awakened from this mode through the Force Wake-Up pin (FWUP), and Wake-Up input pins WKUP0 to WKUP15, Supply Monitor, RTT or RTC wake-up event. Current Consumption is 2.5 µA typical on VDDBU.

Backup mode is entered by using WFE instructions with the SLEEPDEEP bit in the System Control Register of the Cortex-M3 set to 1. (See the “Power Management” description in The “ARM Cortex M3 Processor” section of the product datasheet).

Exit from Backup mode happens if one of the following enable wake up events occurs:

- FWUP pin (low level, configurable debouncing)
- WKUPEN0-15 pins (level transition, configurable debouncing)
- SM alarm
- RTC alarm
- RTT alarm

5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in

PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake-up the core (WFE). By configuring the external lines WKUP0-15 as fast startup wake-up pins (refer to Section 5.7 “Fast Start-Up”). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Current Consumption in Wait mode is typically 15 µA on VDDIN if the internal voltage regulator is used or 8 µA on VDDCORE if an external regulator is used.

Entering Wait Mode:

- Select the 4/8/12 MHz Fast RC Oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, Waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

5.5.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. This mode is entered via Wait for Interrupt (WFI) or Wait for Event (WFE) instructions with LPM = 0 in PMC_FSMR.

The processor can be awakened from an interrupt if WFI instruction of the Cortex M3 is used, or from an event if the WFE instruction is used to enter this mode.

5.5.4 Low Power Mode Summary Table

The modes detailed above are the main low power modes. Each part can be set to on or off separately and wake up sources can be individually configured. Table 5-1 below shows a summary of the configurations of the low power modes.

Table 5-1. Low Power Mode Configuration Summary

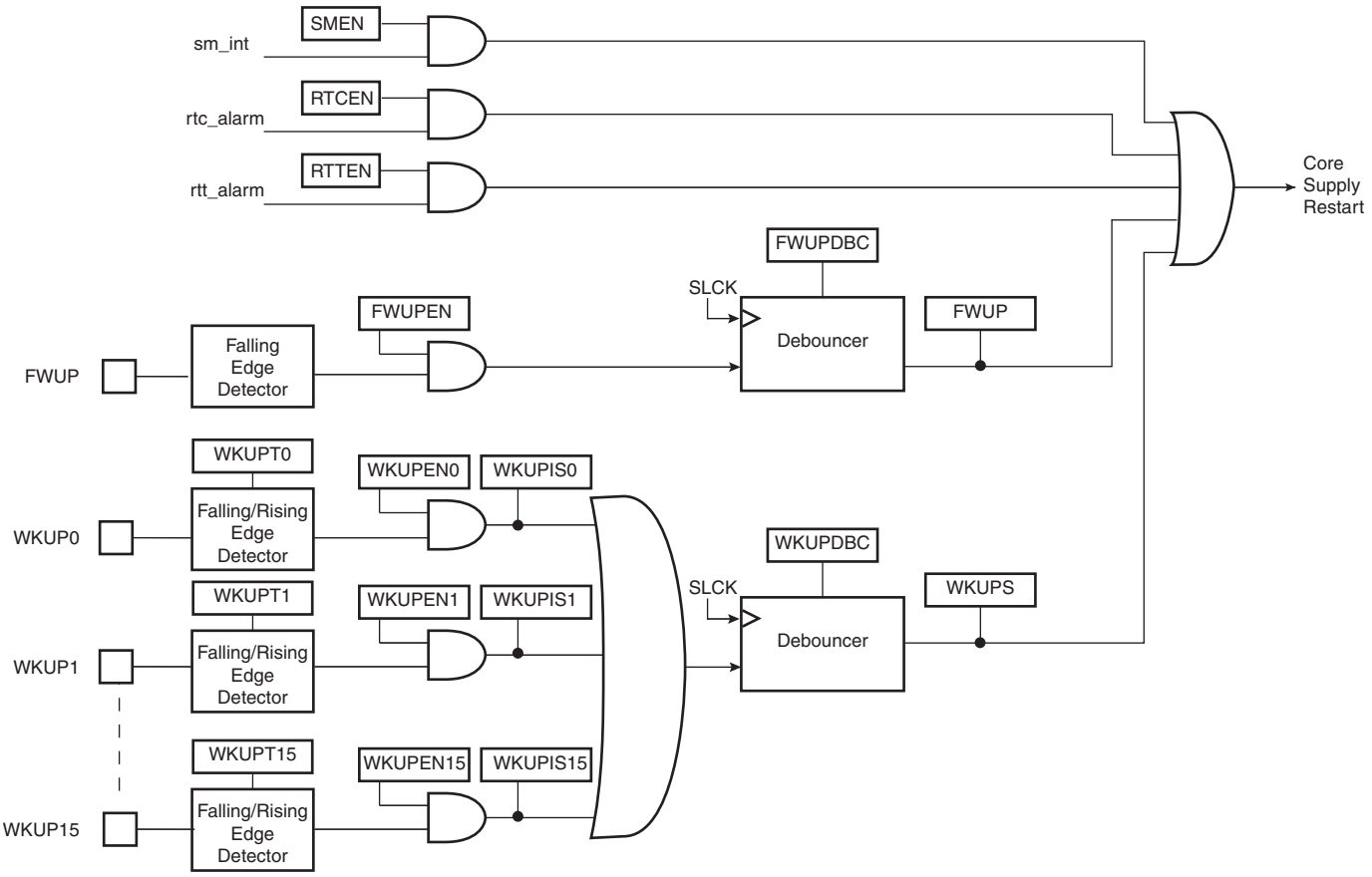
Mode	SUPC, 32 kHz Oscillator RTC RTT Backup Registers, POR (VDDBU Region)	Regulator	Core Memory Peripherals	Mode Entry	Potential Wake Up Sources	Core at Wake Up	PIO State while in Low Power Mode	PIO State at Wake Up	Consumption (2) (3)	Wake-up Time(1)
Backup Mode	ON	OFF SHDN =0	OFF (Not powered)	WFE +SLEEPDEEP bit = 1	FWUP pin WKUP0-15 pins BOD alarm RTC alarm RTT alarm	Reset	Previous state saved	PIOA & PIOB & PIOC Inputs with pull ups	2.5 µA typ(4)	< 0.5 ms
Wait Mode	ON	ON SHDN =1	Powered (Not clocked)	WFE +SLEEPDEEP bit = 0 +LPM bit = 1	Any Event from: Fast startup through WKUP0-15 pins RTC alarm RTT alarm USB wake-up	Clocked back	Previous state saved	Unchanged	8 µA/15 µA (5)	< 10 µs
Sleep Mode	ON	ON SHDN =1	Powered(7) (Not clocked)	WFE or WFI +SLEEPDEEP bit = 0 +LPM bit = 0	Entry mode =WFI Interrupt Only; Entry mode =WFE Any Enabled Interrupt and/or Any Event from: Fast start-up through WKUP0-15 pins RTC alarm RTT alarm USB wake-up	Clocked back	Previous state saved	Unchanged	(6)	(6)

Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz Fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake up until the first instruction is fetched.
2. The external loads on PIOs are not taken into account in the calculation.
3. BOD current consumption is not included.
4. Current consumption on VDDBU.
5. 8 µA total current consumption - **without** using internal voltage regulator.
   15 µA total current consumption - **using** internal voltage regulator.
6. Depends on MCK frequency.
7. In this mode the core is supplied and not clocked but some peripherals can be clocked.

5.6 Wake-up Sources

The wake-up events allow the device to exit backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply.

Figure 5-4. Wake-up Source

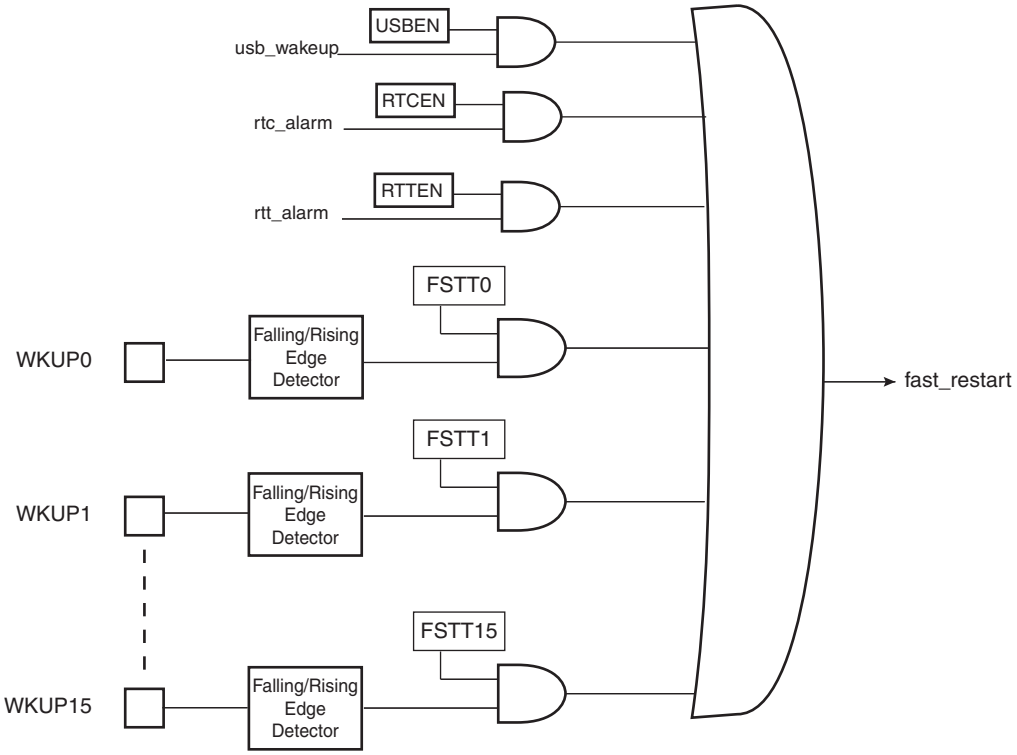


5.7 Fast Start-Up

The SAM3U allows the processor to restart in a few microseconds while the processor is in wait mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs.

The fast restart circuitry, as shown in Figure 5-5, is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4/8/12 MHz fast RC oscillator, switches the master clock on this 4/8/12 MHz clock and reenables the processor clock.

Figure 5-5. Fast Start-Up Sources



6. Input/Output Lines

The SAM3U has different kinds of input/output (I/O) lines, such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functions thanks to multiplexing capabilities of the PIO controllers. The same GPIO line can be used whether it is in IO mode or used by the multiplexed peripheral. System I/Os are pins such as test pin, oscillators, erase pin, analog inputs or debug pins.

With a few exceptions, the I/Os have input schmitt triggers. Refer to the footnotes associated with “PIO Controller - PIOA - PIOB - PIOC” on page 6 within Table 3-1, “Signal Description List”.

6.1 General Purpose I/O Lines (GPIO)

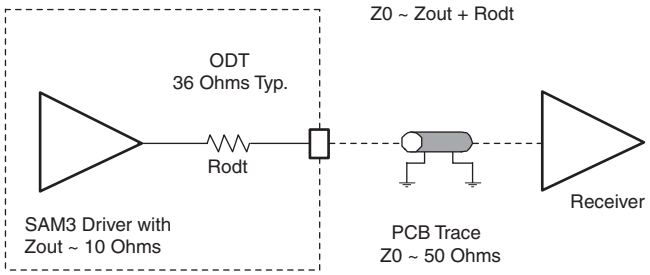
GPIO Lines are managed by PIO Controllers. All I/Os have several input or output modes such as, pull-up, input schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to the “PIO Controller” section of the product datasheet.

The input output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM3U embeds high speed pads able to handle up to 65 MHz for HSMCI and SPI clock lines and 35 MHz on other lines. See “AC Characteristics” of the product datasheet for more details. Typical pull-up value is 100 kΩ for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination), (see Figure 6-1 below). ODT consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM3) and the PCB track impedance preventing signal reflection. The series resistor helps to reduce I/Os switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion, ODT helps reducing signal integrity issues.

Figure 6-1. On-Die Termination schematic



6.2 System I/O Lines

System I/O lines are pins used by oscillators, test mode, reset, flash erase and JTAG to name but a few.

6.3 Serial Wire JTAG Debug Port (SWJ-DP)

The SWJ-DP pins are TCK/SWCLK, TMS/SWDIO, TDO/SWO, TDI and commonly provided on a standard 20-pin JTAG connector defined by ARM. For more details about voltage reference and reset state, refer to Table 3-1, “Signal Description List”

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations.

By default, the JTAG Debug Port is active. If the debugger host wants to switch to the Serial Wire Debug Port, it must provide a dedicated JTAG sequence on TMS/SWDIO and TCK/SWCLK which disables the JTAG-DP and enables the SW-DP. When the Serial Wire Debug Port is active, TDO/TRACESWO can be used for trace.

The asynchronous TRACE output (TRACESWO) is multiplexed with TDO. So the asynchronous trace can only be used with SW-DP, not JTAG-DP.

All the JTAG signals are supplied with VDDIO except JTAGSEL, supplied by VDDBU.

6.4 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or fast flash programming mode of the SAM3U series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the “Fast Flash Programming Interface” section of the product datasheet. For more on the manufacturing and test mode, refer to the “Debug and Test” section of the product datasheet.

6.5 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. It will reset the Core and the peripherals, except the Backup region (RTC, RTT and Supply Controller). There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length.

The NRST pin integrates a permanent pull-up resistor to VDDIO of about 100 kΩ.

6.6 NRSTB Pin

The NRSTB pin is input only and enables asynchronous reset of the SAM3U when asserted low. The NRSTB pin integrates a permanent pull-up resistor of about 15 kΩ. This allows connection of a simple push button on the NRSTB pin as a system-user reset. In all modes, this pin will reset the chip including the Backup region (RTC, RTT and Supply Controller). It reacts as the Power-on reset. It can be used as an external system reset source. In harsh environments, it is recommended to add an external capacitor (10 nF) between NRSTB and VDDBU. (For filtering values refer to “I/O Characteristics” in the “Electrical Characteristics” section of the product datasheet.)

It embeds an anti-glitch filter.

6.7 ERASE Pin

The ERASE pin is used to reinitialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform the reinitialization of the Flash.

Even in all low power modes, asserting the pin will automatically start-up the chip and erase the Flash.

7. Processor and Architecture

7.1 ARM Cortex-M3 Processor

- Version 2.0
- Thumb-2 (ISA) subset consisting of all base Thumb-2 instructions, 16-bit and 32-bit.
- Harvard processor architecture enabling simultaneous instruction fetch with data load/store.
- Three-stage pipeline.
- Single cycle 32-bit multiply.
- Hardware divide.
- Thumb and Debug states.
- Handler and Thread modes.
- Low latency ISR entry and exit.

7.2 APB/AHB Bridges

The SAM3U product embeds two separated APB/AHB bridges:

- low speed bridge
- high speed bridge

This architecture enables to make concurrent accesses on both bridges.

All the peripherals are on the low-speed bridge except SPI, SSC and HSMCI.

The UART, 10-bit ADC (ADC), 12-bit ADC (ADC12B), TWI0-1, USART0-3, PWM have dedicated channels for the Peripheral DMA Channels (PDC). These peripherals can not use the DMA Controller.

The high speed bridge regroups the SSC, SPI and HSMCI. These three peripherals do not have PDC channels but can use the DMA with the internal FIFO for Channel buffering.

Note that the peripherals of the two bridges are clocked by the same source: MCK.

7.3 Matrix Masters

The Bus Matrix of the SAM3U device manages 5 masters, which means that each master can perform an access concurrently with others to an available slave.

Each master has its own decoder and specifically defined bus. In order to simplify the addressing, all the masters have the same decoding.

Table 7-1. List of Bus Matrix Masters

Master 0	Cortex-M3 Instruction/Data
Master 1	Cortex-M3 System
Master 2	Peripheral DMA Controller (PDC)
Master 3	USB Device High Speed DMA
Master 4	DMA Controller

7.4 Matrix Slaves

The Bus Matrix of the SAM3U manages 10 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM0
Slave 1	Internal SRAM1
Slave 2	Internal ROM
Slave 3	Internal Flash 0
Slave 4	Internal Flash 1
Slave 5	USB Device High Speed Dual Port RAM (DPR)
Slave 6	NAND Flash Controller RAM
Slave 7	External Bus Interface
Slave 8	Low Speed Peripheral Bridge
Slave 9	High Speed Peripheral Bridge

7.5 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, for example allowing access from the USB Device High speed DMA to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and shown as "–" in Table 7-3 below.

Table 7-3. SAM3U Master to Slave Access

		0	1	2	3	4
Slaves	**Masters**	**Cortex-M3 I/D Bus**	**Cortex-M3 S Bus**	**PDC**	**USB Device High Speed DMA**	**DMA Controller**
0	Internal SRAM0	–	X	X	X	X
1	Internal SRAM1	–	X	X	X	X
2	Internal ROM	X	–	X	X	X
3	Internal Flash 0	X	–	–	–	–
4	Internal Flash 1	X	–	–	–	–
5	USB Device High Speed Dual Port RAM (DPR)	–	X	–	–	–
6	NAND Flash Controller RAM	–	X	X	X	X
7	External Bus Interface	–	X	X	X	X
8	Low Speed Peripheral Bridge	–	X	X	–	–
9	High Speed Peripheral Bridge	–	X	X	–	–

7.6 DMA Controller

- Acting as one Matrix Master
- Embeds 4 channels:
  - 3 channels with 8 bytes/FIFO for Channel Buffering
  - 1 channel with 32 bytes/FIFO for Channel Buffering
- Linked List support with Status Write Back operation at End of Transfer
- Word, HalfWord, Byte transfer support.
- Handles high speed transfer of SPI, SSC and HSMCI (peripheral to memory, memory to peripheral)
- Memory to memory transfer
- Can be triggered by PWM and T/C which enables to generate waveforms though the External Bus Interface

The DMA controller can handle the transfer between peripherals and memory and so receives the triggers from the peripherals listed below. The hardware interface numbers are also given in Table 7-4 below.

Table 7-4. DMA Controller

Instance name	Channel T/R	DMA Channel HW interface Number
HSMCI	Transmit/Receive	0
SPI	Transmit	1
SPI	Receive	2
SSC	Transmit	3
SSC	Receive	4
PWM Event Line 0	Trigger	5
PWM Event Line 1	Trigger	6
TIO Output of TImer Counter Channel 0	Trigger	7

7.7 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Nineteen channels
  - Two for each USART
  - Two for the UART
  - Two for each Two Wire Interface
  - One for the PWM
  - One for each Analog-to-digital Converter
- Low bus arbitration overhead
  - One Master Clock cycle needed for a transfer from memory to peripheral
  - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirement

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

Table 7-5. Peripheral DMA Controller

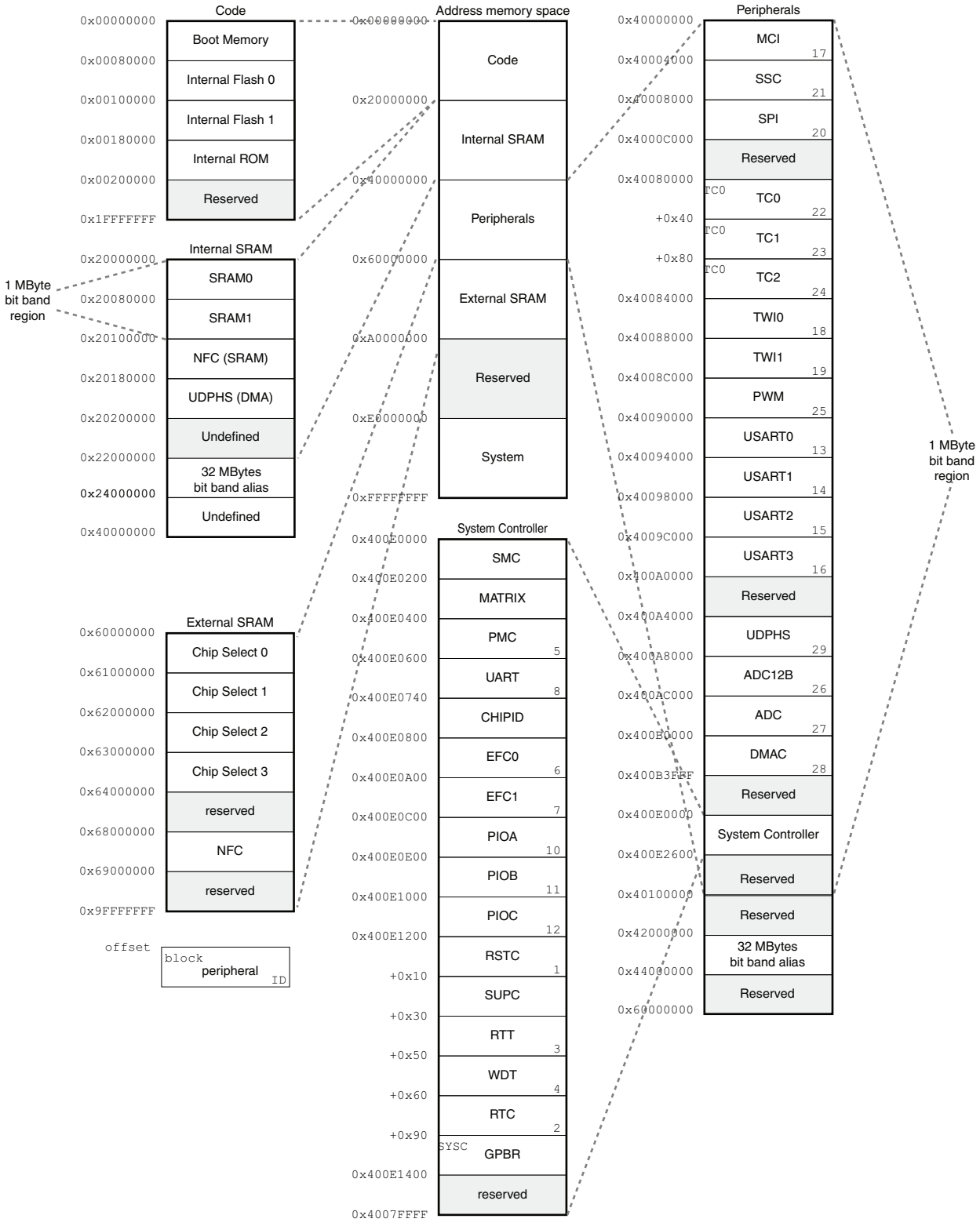
Instance name	Channel T/R
TWI1	Transmit
TWI0	Transmit
PWM	Transmit
UART	Transmit
USART3	Transmit
USART2	Transmit
USART1	Transmit
USART0	Transmit
TWI0	Receive
TWI1	Receive
UART	Receive
USART3	Receive
USART2	Receive
USART1	Receive
USART0	Receive
ADC	Receive
ADC12B	Receive

7.8 Debug and Test Features

- Debug access to all memory and registers in the system, including Cortex-M3 register bank when the core is running, halted, or held in reset.
- Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing break points and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watch points, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- IEEE® 1149.1 JTAG Boundary-scan on all digital pins

8. Product Mapping

Figure 8-1. SAM3U Memory Mapping



9. Memories

The embedded and external memories are described below.

9.1 Embedded Memories

9.1.1 Internal SRAM

The SAM3U4 (256 KBytes internal Flash version) embeds a total of 48 Kbytes high-speed SRAM (32 Kbytes SRAM0 and 16 Kbytes SRAM1).

The SAM3U2 (128 KBytes internal Flash version) embeds a total of 32 Kbytes high-speed SRAM (16 Kbytes SRAM0 and 16 Kbytes SRAM1).

The SAM3U1 (64 KBytes internal Flash version) embeds a total of 16 Kbytes high-speed SRAM (8 Kbytes SRAM0 and 8 Kbytes SRAM1).

The SRAM0 is accessible over System Cortex-M3 bus at address 0x2000 0000 and SRAM1 at address 0x2008 0000. The user can see the SRAM as contiguous.

The SRAM0 and SRAM1 are in the bit band region. The bit band alias region is from 0x2200 0000 and 0x23FF FFFF.

The NAND Flash Controller embeds 4224 bytes of internal SRAM. If the NAND Flash controller is not used, these 4224 Kbytes of SRAM can be used as general purpose. It can be seen at address 0x2010 0000.

9.1.2 Internal ROM

The SAM3U product embeds an Internal ROM, which contains the SAM-BA Boot and FFPI program.

At any time, the ROM is mapped at address 0x0018 0000.

9.1.3 Embedded Flash

9.1.3.1 Flash Overview

The Flash of the SAM3U4 (256 KBytes internal Flash version) is organized in two banks of 512 pages (dual plane) of 256 bytes.

The Flash of the SAM3U2 (128 KBytes internal Flash version) is organized in one bank of 512 pages (single plane) of 256 bytes.

The Flash of the is SAM3U1 (256 KBytes internal Flash version) organized in one bank of 256 pages (single plane) of 256 bytes.

The Flash contains a 128-byte write buffer, accessible through a 32-bit interface.

9.1.3.2 Flash Power Supply

The Flash is supplied by VDDCORE.

9.1.3.3 Enhanced Embedded Flash Controller

The Enhanced Embedded Flash Controller (EEFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped within the Memory Controller on the APB.

The Enhanced Embedded Flash Controller ensures the interface of the Flash block with the 32-bit internal bus. Its 128-bit wide memory interface increases performance.

The user can choose between high performance or lower current consumption by selecting either 128-bit or 64-bit access. It also manages the programming, erasing, locking and unlocking sequences of the Flash using a full set of commands.

One of the commands returns the embedded Flash descriptor definition that informs the system about the Flash organization, thus making the software generic.

The SAM3U4 (256 KBytes internal Flash version) embeds two EEFC (EEFC0 for Flash0 and EEFC1 for Flash1) whereas the SAM3U2/1 embeds one EEFC.

9.1.3.4 Lock Regions

In the **SAM3U4** (256 KBytes internal Flash version) two Enhanced Embedded Flash Controllers each manage 16 lock bits to protect 32 regions of the flash against inadvertent flash erasing or programming commands.

The **SAM3U4** (256 KBytes internal Flash version) contains 32 lock regions and each lock region contains 32 pages of 256 bytes. Each lock region has a size of 8 Kbytes.

The **SAM3U2** (128 KBytes internal Flash version) Enhanced Embedded Flash Controller manages 16 lock bits to protect 32 regions of the flash against inadvertent flash erasing or programming commands.

The **SAM3U2** (128 KBytes internal Flash version) contains 16 lock regions and each lock region contains 32 pages of 256 bytes. Each lock region has a size of 8 Kbytes.

The **SAM3U1**(64 KBytes internal Flash version) Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands.

The **SAM3U1**(64 KBytes internal Flash version) contains 8 lock regions and each lock region contains 32 pages of 256 bytes. Each lock region has a size of 8 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.1.3.5 Security Bit Feature

The SAM3U features a security bit, based on a specific General Purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, SRAM, Core Registers and Internal Peripherals either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the command "Set General Purpose NVM Bit 0" of

the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash, SRAM, Core Registers and Internal Peripherals either through the ICE interface or through the Fast Flash Programming Interface are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms. As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

9.1.3.6 *Calibration Bits*

NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.1.3.7 *Unique Identifier*

Each device integrates its own 128-bit unique identifier. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the unique identifier.

9.1.3.8 *Fast Flash Programming Interface*

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when TST, NRSTB and FWUP pins are tied high during power up sequence and if all supplies are provided externally (do not use internal regulator for VDDCORE). Please note that since the FFPI is a part of the SAM-BA Boot Application, the device must boot from the ROM.

9.1.3.9 *SAM-BA® Boot*

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the UART and USB.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped in Flash at address 0x0 when GPNVM bit 1 is set to 0.

9.1.3.10 *GPNVM Bits*

The SAM3U features three GPNVM bits that can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

The SAM3U4 is equipped with two EEFC, EEFC0 and EEFC1. EEFC1 does not feature the GPNVM bits. The GPNVM embedded on EEFC0 applies to the two blocks in the SAM3U4.

Table 9-1. General-purpose Non-volatile Memory Bits

GPNVMBit[#]	Function
0	Security bit
1	Boot mode selection
2	Flash selection (Flash 0 or Flash 1) Only on SAM3U4 (256 Kbytes internal Flash version)

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure a maximum boot possibilities the memory layout can be changed via GPNVM.

A general purpose NVM (GPNVM1) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface.

Setting the GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

GPNVM2 enables to select if Flash 0 or Flash 1 is used for the boot. Setting the GPNVM2 bit selects the boot from Flash 1, clearing it selects the boot from Flash 0.

9.2 External Memories

The SAM3U offers an interface to a wide range of external memories and to any parallel peripheral.

9.2.1 Static Memory Controller

- 8- or 16- bit Data Bus
- Up to 24-bit Address Bus (up to 16 MBytes linear per chip select)
- Up to 4 chips selects, Configurable Assignment
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
- Multiple device adaptability
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported

9.2.2 NAND Flash Controller

- Handles automatic Read/Write transfer through 4224 bytes SRAM buffer
- DMA support
- Supports SLC NAND Flash technology
- Programmable timing on a per chip select basis
- Programmable Flash Data width 8-bit or 16-bit

9.2.3 NAND Flash Error Corrected Code Controller

- Integrated in the NAND Flash Controller
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing
  - ECC value available in a register
- Automatic Hamming Code Calculation while reading
  - Error Report, including error flag, correctable error flag and word address being detected erroneous

– Supports 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-byte pages

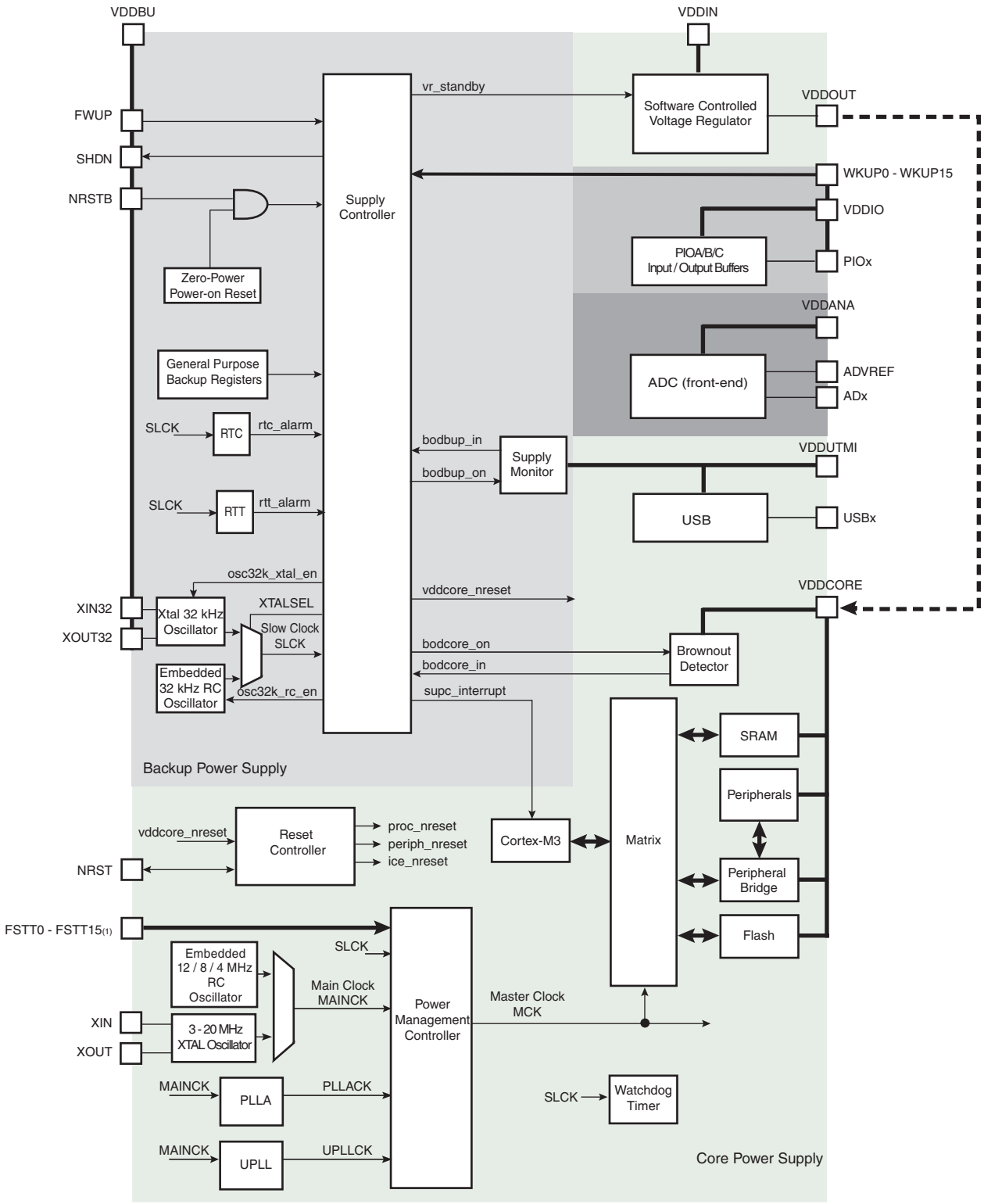
10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc...

The System Controller User Interface also embeds the registers used to configure the Matrix.

See the system controller block diagram in Figure 10-1 on page 37.

Figure 10-1. System Controller Block Diagram



FSTT0 - FSTT15 are possible Fast Startup Sources, generated by WKUP0-WKUP15 Pins, but are not physical pins.

10.1 System Controller and Peripheral Mapping

Please refer to Figure 8-1"SAM3U Memory Mapping" on page 30 .

All the peripherals are in the bit band region and are mapped in the bit band alias region.

10.2 Power-on-Reset, Brownout and Supply Monitor

The SAM3U embeds three features to monitor, warn and/or reset the chip:

- Power-on-Reset on VDDBU
- Brownout Detector on VDDCORE
- Supply Monitor on VDDUTMI

10.2.1 Power-on-Reset on VDDBU

The Power-on-Reset monitors VDDBU. It is always activated and monitors voltage at start up but also during power down. If VDDBU goes below the threshold voltage, the entire chip is reset. For more information, refer to the "Electrical Characteristics" section of the datasheet.

10.2.2 Brownout Detector on VDDCORE

The Brownout Detector monitors VDDCORE. It is active by default. It can be deactivated by software through the Supply Controller (SUPC_MR). It is especially recommended to disable it during low-power modes such as wait or sleep modes.

If VDDCORE goes below the threshold voltage, the reset of the core is asserted. For more information, refer to the "Supply Controller" and "Electrical Characteristics" sections of the product datasheet.

10.2.3 Supply Monitor on VDDUTMI

The Supply Monitor monitors VDDUTMI. It is not active by default. It can be activated by software and is fully programmable with 16 steps for the threshold (between 1.9V to 3.4V). It is controlled by the Supply Controller. A sample mode is possible. It allows to divide the supply monitor power consumption by a factor of up to 2048. For more information, refer to the "Supply Controller" and "Electrical Characteristics" sections of the product datasheet.

10.3 Reset Controller

The Reset Controller is capable to return to the software the source of the last reset, either a general reset, a wake-up reset, a software reset, a user reset or a watchdog reset.

The Reset Controller controls the internal resets of the system and the NRST pin output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset.

10.4 Supply Controller

The Supply Controller controls the power supplies of each section of the processor and the peripherals (via Voltage regulator control).

The Supply Controller has its own reset circuitry and is clocked by the 32 kHz Slow clock generator.

The reset circuitry is based on a zero-power power-on reset cell. The zero-power power-on reset allows the Supply Controller to start properly.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

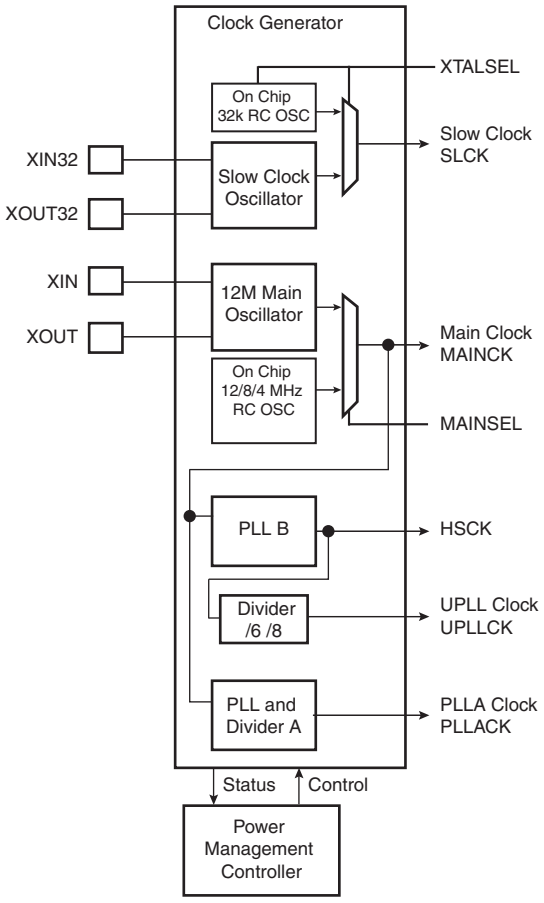
The Supply Controller starts up the device by enabling the Voltage Regulator, then it generates the proper reset signals to the core power supply.
It also enables to set the system in different low power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One Low Power 32768 Hz Slow Clock Oscillator with bypass mode
- One Low Power RC Oscillator
- One 3 to 20 MHz Crystal Oscillator, which can be bypassed
- One Fast RC Oscillator factory programmed, 3 output frequencies can be selected: 4, 8 or 12 MHz. By default 4 MHz is selected. 8 MHz and 12 MHz output are factory calibrated.
- One 480 MHz UPLL providing a clock for the USB High Speed Device Controller. Input frequency is 12 MHz (only).
- One 96 to 192 MHz programmable PLL (PLL A), capable to provide the clock MCK to the processor and to the peripherals. The input frequency of the PLL A is between 8 and 16 MHz.

Figure 10-2. Clock Generator Block Diagram



10.6 Power Management Controller

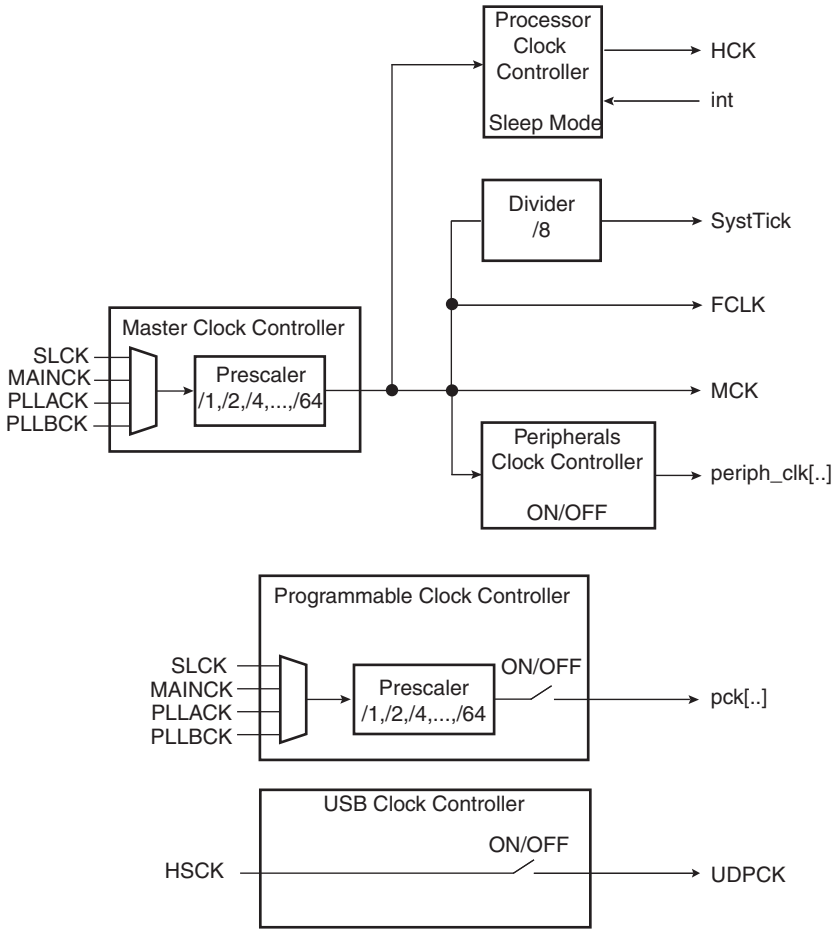
The Power Management Controller provides all the clock signals to the system. It provides:

- the Processor Clock HCLK
- the Free running processor clock FCLK
- the Cortex SysTick external clock
- the Master Clock MCK, in particular to the Matrix and the memory interfaces
- the USB Device HS Clock UDPCK
- independent peripheral clocks, typically at the frequency of MCK
- three programmable clock outputs: PCK0, PCK1 and PCK2

The Supply Controller selects between the 32 kHz RC oscillator or the crystal oscillator. The unused oscillator is disabled automatically so that power consumption is optimized.

By default, at startup the chip runs out of the Master Clock using the Fast RC Oscillator running at 4 MHz.

Figure 10-3. Power Management Controller Block Diagram



The SysTick calibration value is fixed at 10500, which allows the generation of a time base of 1 ms with SystTick clock to 10.5 MHz (max HCLK/8).

10.7 Watchdog Timer

- 16-bit key-protected once-only Programmable Counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

10.8 SysTick Timer

- 24-bit down counter
- Self-reload capability
- Flexible system timer

10.9 Real-time Timer

- Real-time Timer, allowing backup of time with different accuracies
  - 32-bit Free-running back-up Counter
  - Integrates a 16-bit programmable prescaler running on slow clock
  - Alarm Register capable to generate a wake-up of the system

10.10 Real-time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

10.11 General-Purpose Back-up Registers

- Eight 32-bit general-purpose backup registers

10.12 Nested Vectored Interrupt Controller

- Thirty maskable interrupts
- Sixteen priority levels
- Dynamic reprioritization of interrupts
- Priority grouping
  - selection of preempting interrupt levels and non preempting interrupt levels.
- Support for tail-chaining and late arrival of interrupts.
  - back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on
  - interrupt exit, with no instruction overhead.

10.13 Chip Identification

- Chip Identifier (CHIPID) registers permit recognition of the device and its revision.

Table 10-1. SAM3U Chip IDs Register - Engineering Samples

Chip Name	Flash Size KByte	Pin Count	CHIPID_CIDR	CHIPID_EXID
SAM3U4C (Rev A)	256	100	0x28000960	0x0
SAM3U2C (Rev A)	128	100	0x280A0760	0x0
SAM3U1C (Rev A)	64	100	0x28090560	0x0
SAM3U4E (Rev A)	256	144	0x28100960	0x0
SAM3U2E (Rev A)	128	144	0x281A0760	0x0
SAM3U1E (Rev A)	64	144	0x28190560	0x0

- JTAG ID: 0x0582A03F

Table 10-2. SAM3U Chip IDs Register - Revision A Parts

Chip Name	Flash Size KByte	Pin Count	CHIPID_CIDR	CHIPID_EXID
SAM3U4C (Rev A)	256	100	0x28000961	0x0
SAM3U2C (Rev A)	128	100	0x280A0761	0x0
SAM3U1C (Rev A)	64	100	0x28090561	0x0
SAM3U4E (Rev A)	256	144	0x28100961	0x0
SAM3U2E (Rev A)	128	144	0x281A0761	0x0
SAM3U1E (Rev A)	64	144	0x28190561	0x0

- JTAG ID: 0x0582A03F

10.14 PIO Controllers

- 3 PIO Controllers, PIOA, PIOB, and PIOC, controlling a maximum of 96 I/O Lines
- Each PIO Controller controls up to 32 programmable I/O Lines
  - PIOA has 32 I/O Lines
  - PIOB has 32 I/O Lines
  - PIOC has 32 I/O Lines
- Fully programmable through Set/Clear Registers
- Multiplexing of two peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change, rising edge, falling edge, low level and level interrupt
  - Debouncing and Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

11. Peripherals

11.1 Peripheral Identifiers

Table 11-1 defines the Peripheral Identifiers of the SAM3U. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Note that some Peripherals are always clocked. Please refer to the table below.

Table 11-1. Peripheral Identifiers

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
0	SUPC	X		Supply Controller
1	RSTC	X		Reset Controller
2	RTC	X		Real Time Clock
3	RTT	X		Real Time Timer
4	WDT	X		Watchdog Timer
5	PMC	X		Power Management Controller
6	EEFC0	X		Enhanced Embedded Flash Controller 0
7	EEFC1	X		Enhanced Embedded Flash Controller 1
8	UART	X	X	Universal Asynchronous Receiver Transmitter
9	SMC	X	X	Static Memory Controller
10	PIOA	X	X	Parallel I/O Controller A,
11	PIOB	X	X	Parallel I/O Controller B
12	PIOC	X	X	Parallel I/O Controller C
13	USART0	X	X	USART 0
14	USART1	X	X	USART 1
15	USART2	X	X	USART 2
16	USART3	X	X	USART 3
17	HSMCI	X	X	High Speed Multimedia Card Interface
18	TWI0	X	X	Two-Wire Interface 0
19	TWI1	X	X	Two-Wire Interface 1
20	SPI	X	X	Serial Peripheral Interface
21	SSC	X	X	Synchronous Serial Controller
22	TC0	X	X	Timer Counter 0
23	TC1	X	X	Timer Counter 1
24	TC2	X	X	Timer Counter 2
25	PWM	X	X	Pulse Width Modulation Controller
26	ADC12B	X	X	12-bit ADC Controller
27	ADC	X	X	10-bit ADC Controller
28	DMAC	X	X	DMA Controller
29	UDPHS	X	X	USB Device High Speed

11.2 Peripheral Signal Multiplexing on I/O Lines

The SAM3U features 3 PIO controllers, PIOA, PIOB and PIOC that multiplex the I/O lines of the peripheral set.

Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. The multiplexing tables in the following pages define how the I/O lines of peripherals A and B are multiplexed on the PIO Controllers. The two columns “Extra Function” and “Comments” have been inserted in this table for the user’s own comments, they may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only, might be duplicated within the tables.

11.2.1 PIO Controller A Multiplexing

Table 11-2. Multiplexing on PIO Controller A (PIOA)

I/O Line	Peripheral A	Peripheral B	Extra Function	Comments
PA0	TIOB0	NPCS1	WKUP0[1][2]	
PA1	TIOA0	NPCS2	WKUP1[1][2]	
PA2	TCLK0	AD12BTRG	WKUP2[1][2]	
PA3	MCCK	PCK1		
PA4	MCCDA	PWMH0		
PA5	MCDA0	PWMH1		
PA6	MCDA1	PWMH2		
PA7	MCDA2	PWML0		
PA8	MCDA3	PWML1		
PA9	TWD0	PWML2	WKUP3[1][2]	
PA10	TWCK0	PWML3	WKUP4[1][2]	
PA11	URXD	PWMFI0		
PA12	UTXD	PWMFI1		
PA13	MISO			
PA14	MOSI			
PA15	SPCK	PWMH2		
PA16	NPCS0	NCS1	WKUP5[1][2]	
PA17	SCK0	ADTRG	WKUP6[1][2]	
PA18	TXD0	PWMFI2	WKUP7[1][2]	
PA19	RXD0	NPCS3	WKUP8[1][2]	
PA20	TXD1	PWMH3	WKUP9[1][2]	
PA21	RXD1	PCK0	WKUP10[1][2]	
PA22	TXD2	RTS1	AD12B0	
PA23	RXD2	CTS1		
PA24	TWD1	SCK1	WKUP11[1][2]	Only on 144-pin version
PA25	TWCK1	SCK2	WKUP12[1][2]	Only on 144-pin version
PA26	TD	TCLK2		
PA27	RD	PCK0		
PA28	TK	PWMH0		
PA29	RK	PWMH1		
PA30	TF	TIOA2	AD12B1	
PA31	RF	TIOB2		

Notes: 1. Wake-Up source in Backup mode (managed by the SUPC).
2. Fast Start-Up source in Wait mode (managed by the PMC).

11.2.2 PIO Controller B Multiplexing

Table 11-3. Multiplexing on PIO Controller B (PIOB)

I/O Line	Peripheral A	Peripheral B	Extra Function	Comments
PB0	PWMH0	A2	WKUP13[1][2]	
PB1	PWMH1	A3	WKUP14[1][2]	
PB2	PWMH2	A4	WKUP15[1][2]	
PB3	PWMH3	A5	AD12B2	
PB4	TCLK1	A6	AD12B3	
PB5	TIOA1	A7	AD0	
PB6	TIOB1	D15	AD1	
PB7	RTS0	A0/NBS0	AD2	
PB8	CTS0	A1	AD3	
PB9	D0	DTR0		
PB10	D1	DSR0		
PB11	D2	DCD0		
PB12	D3	RI0		
PB13	D4	PWMH0		
PB14	D5	PWMH1		
PB15	D6	PWMH2		
PB16	D7	PWMH3		
PB17	NANDOE	PWML0		
PB18	NANDWE	PWML1		
PB19	NRD	PWML2		
PB20	NCS0	PWML3		
PB21	A21/NANDALE	RTS2		
PB22	A22/NANDCLE	CTS2		
PB23	NWR0/NWE	PCK2		
PB24	NANDRDY	PCK1		
PB25	D8	PWML0		Only on 144-pin version
PB26	D9	PWML1		Only on 144-pin version
PB27	D10	PWML2		Only on 144-pin version
PB28	D11	PWML3		Only on 144-pin version
PB29	D12			Only on 144-pin version
PB30	D13			Only on 144-pin version
PB31	D14			Only on 144-pin version

Notes: 1. Wake-Up source in Backup mode (managed by the SUPC).
2. Fast Start-Up source in Wait mode (managed by the PMC).

11.2.3 PIO Controller C Multiplexing

Table 11-4. Multiplexing on PIO Controller C (PIOC)

I/O Line	Peripheral A	Peripheral B	Extra function	Comments
PC0	A2			Only on 144-pin version
PC1	A3			Only on 144-pin version
PC2	A4			Only on 144-pin version
PC3	A5	NPCS1		Only on 144-pin version
PC4	A6	NPCS2		Only on 144-pin version
PC5	A7	NPCS3		Only on 144-pin version
PC6	A8	PWML0		Only on 144-pin version
PC7	A9	PWML1		Only on 144-pin version
PC8	A10	PWML2		Only on 144-pin version
PC9	A11	PWML3		Only on 144-pin version
PC10	A12	CTS3		Only on 144-pin version
PC11	A13	RTS3		Only on 144-pin version
PC12	NCS1	TXD3		Only on 144-pin version
PC13	A2	RXD3		Only on 144-pin version
PC14	A3	NPCS2		Only on 144-pin version
PC15	NWR1/NBS1		AD12B4	Only on 144-pin version
PC16	NCS2	PWML3	AD12B5	Only on 144-pin version
PC17	NCS3		AD12B6	Only on 144-pin version
PC18	NWAIT		AD12B7	Only on 144-pin version
PC19	SCK3	NPCS1		Only on 144-pin version
PC20	A14			Only on 144-pin version
PC21	A15			Only on 144-pin version
PC22	A16			Only on 144-pin version
PC23	A17			Only on 144-pin version
PC24	A18	PWMH0		Only on 144-pin version
PC25	A19	PWMH1		Only on 144-pin version
PC26	A20	PWMH2		Only on 144-pin version
PC27	A23	PWMH3		Only on 144-pin version
PC28		MCDA4	AD4	Only on 144-pin version
PC29	PWML0	MCDA5	AD5	Only on 144-pin version
PC30	PWML1	MCDA6	AD6	Only on 144-pin version
PC31	PWML2	MCDA7	AD7	Only on 144-pin version

Notes: 1. Wake-Up source in Backup mode (managed by the SUPC).
2. Fast Start-Up source in Wait mode (managed by the PMC).

12. Embedded Peripherals Overview

12.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

12.2 Two Wire Interface (TWI)

- Master, Multi-Master and Slave Mode Operation
- Compatibility with Atmel two-wire interface, serial memory and I^2C compatible devices
- One, two or three bytes for slave address
- Sequential read/write operations
- Bit Rate: Up to 400 kbit/s
- General Call Supported in Slave Mode
- Connecting to PDC channel capabilities optimizes data transfers in Master Mode only
  - One channel for the receiver, one channel for the transmitter
  - Next buffer support

12.3 Universal Asynchronous Receiver Transceiver (UART)

- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

12.4 Universal Synchronous Asynchronous Receiver Transmitter (USART)

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- SPI Mode
  - Master or Slave
  - Serial Clock programmable Phase and Polarity
  - SPI Serial Clock (SCK) Frequency up to MCK/6
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

12.5 Serial Synchronous Controller (SSC)

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I^2S, TDM Buses, Magnetic Card Reader, ...)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

12.6 Timer Counter (TC)

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement

  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/Down Capabilities
  - Quadrature Decoder Logic
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

12.7 Pulse Width Modulation Controller (PWM)

- 4 channels, one 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
  - A Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
  - High Frequency Asynchronous clocking mode
- Independent channel programming
  - Independent Enable Disable Commands
  - Independent Clock Selection
  - Independent Period and Duty Cycle, with Double Buffering
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform
  - Independent Output Override for each channel
  - Independent complementary Outputs with 12-bit dead time generator for each channel
  - Independent Enable Disable Commands
  - Independent Clock Selection
  - Independent Period and Duty Cycle, with Double Buffering
- Synchronous Channel mode
  - Synchronous Channels share the same counter
  - Mode to update the synchronous channels registers after a programmable number of periods
- Connection to one PDC channel
  - Offers Buffer transfer without Processor Intervention, to update duty cycle of synchronous channels
- Two independent event lines which can send up to 8 triggers on ADC within a period
- Four programmable Fault Inputs providing asynchronous protection of outputs

12.8 High Speed Multimedia Card Interface (HSMCI)

- Compatibility with MultiMedia Card Specification Version 4.3
- Compatibility with SD Memory Card Specification Version 2.0
- Compatibility with SDIO Specification Version V2.0.
- Compatibility with CE-ATA Specification 1.1
- Cards clock rate up to Master Clock divided by 2
- Boot Operation Mode support
- High Speed mode support
- Embedded power management to slow down clock rate when not used
- HSMCI has one slot supporting
  - One MultiMediaCard bus (up to 30 cards) or
  - One SD Memory Card
  - One SDIO Card
- Support for stream, block and multi-block data read and write
- Supports Connection to DMA controller
  - Minimizes Processor intervention for large buffer transfers
- Built in FIFO (32 bytes) with large Memory Aperture Supporting Incremental access
- Support for CE-ATA Completion Signal Disable Command

12.9 USB High Speed Device Port (UDPHS)

- USB V2.0 high-speed compliant, 480 MBits per second
- Embedded USB V2.0 UTMI+ high-speed transceiver
- Embedded 4-Kbyte dual-port RAM for endpoints
- Embedded 6 channels DMA controller
- Suspend/Resume logic
- Up to 2 or 3 banks for isochronous and bulk endpoints
- Seven endpoints, configurable by software
- Maximum configuration: seven endpoints:
  - Endpoint 0: 64 bytes, 1 bank mode
  - Endpoint 1 & 2: 512 bytes, 2 banks mode, HS isochronous capable
  - Endpoint 3 & 4:64 bytes, 3 banks mode
  - Endpoint 5 & 6: 1024 bytes, 3 banks mode, HS isochronous capable

12.10 Analog-to-Digital Converter (ADC)

Two ADCs are embedded in the product.

12.10.1 12-bit High Speed ADC

- 8-channel ADC
- 12-bit 1 Msamples/sec. Cyclic Pipeline ADC
- Integrated 8-to-1 multiplexer
- 12-bit resolution

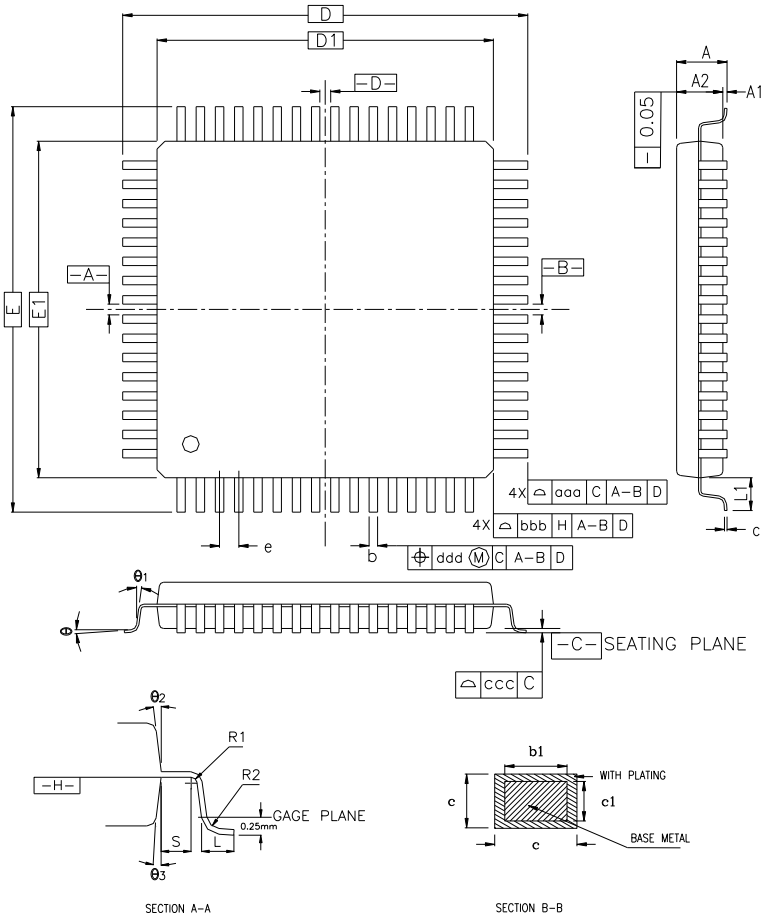
- Selectable single ended or differential input voltage
- Programmable gain for maximum full scale input range
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
  - PWM trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

12.10.2 10-bit Low Power ADC

- 8-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 533 Ksamples/sec. Successive Approximation Register ADC
- -2/+2 LSB Integral Non Linearity, -1/+1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
  - PWM trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

13. Package Drawings

Figure 13-1. 100-ball LQFP Package Drawing



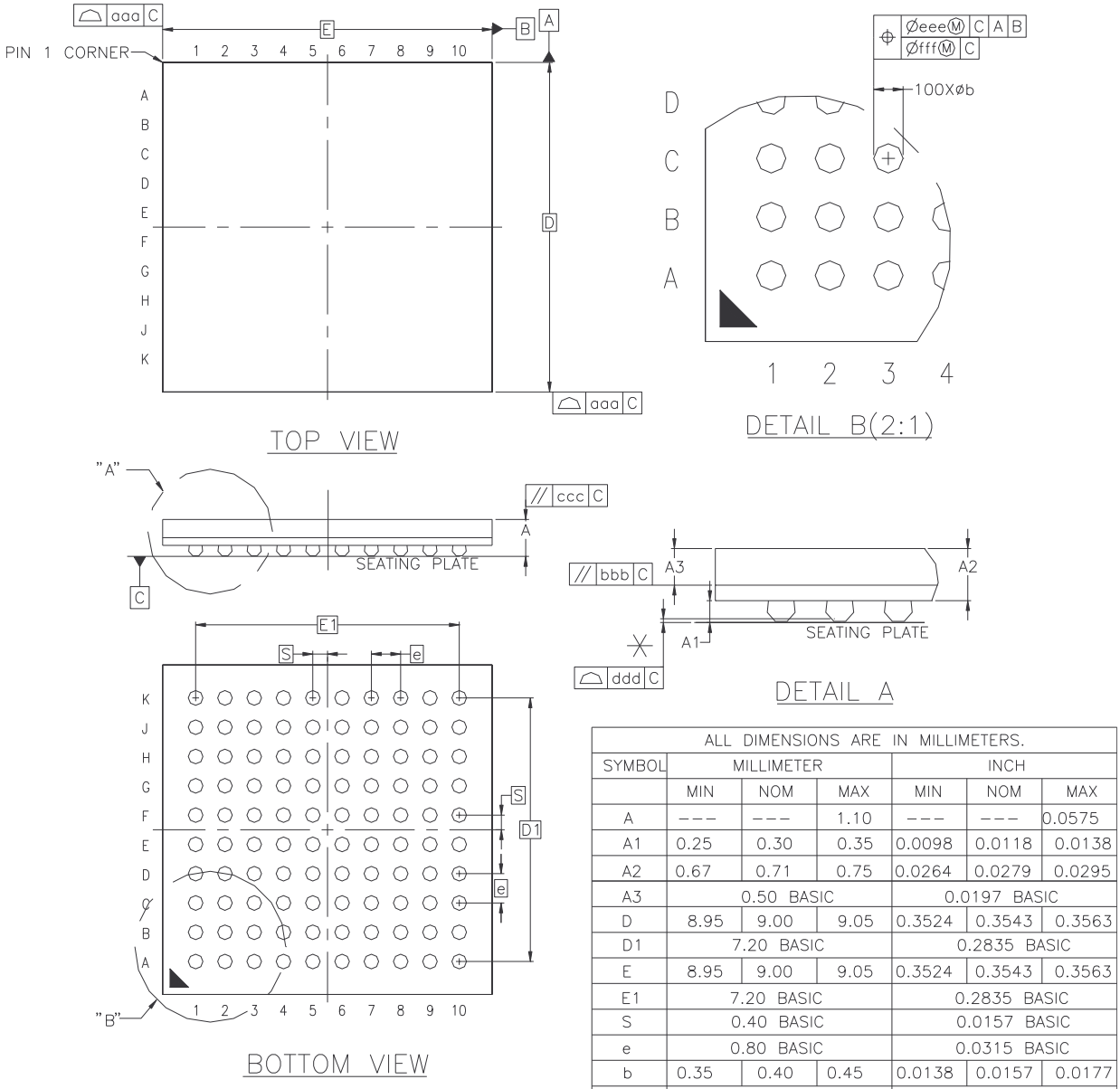
CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D_1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
L_1	1.00 REF			0.039 REF		
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.17	—	0.27	0.007	—	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
e	0.50 BSC.			0.020 BSC.		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

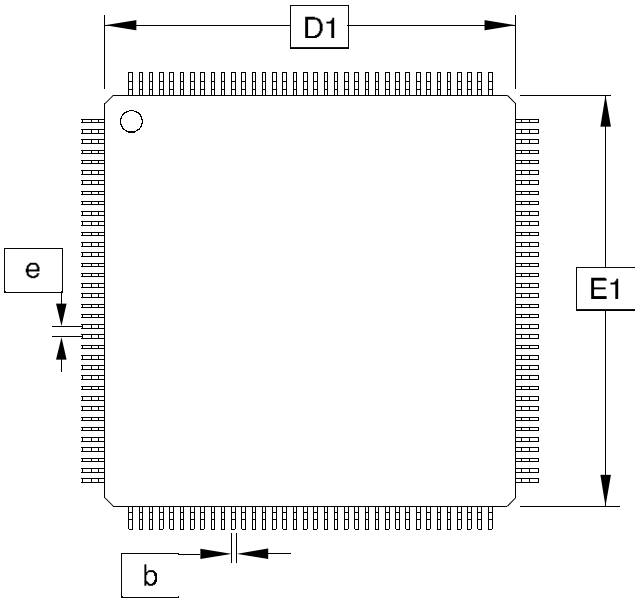
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08MM TOTAL IN EXESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

Figure 13-2. 100-ball LFBGA Package Drawing

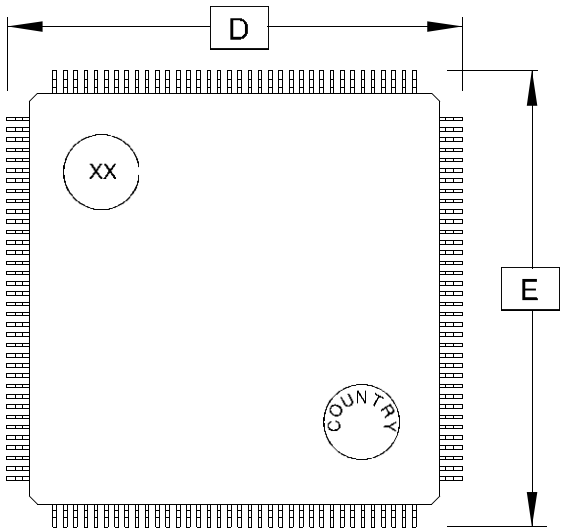


ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.0575
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.67	0.71	0.75	0.0264	0.0279	0.0295
A3	0.50 BASIC			0.0197 BASIC		
D	8.95	9.00	9.05	0.3524	0.3543	0.3563
D1	7.20 BASIC			0.2835 BASIC		
E	8.95	9.00	9.05	0.3524	0.3543	0.3563
E1	7.20 BASIC			0.2835 BASIC		
S	0.40 BASIC			0.0157 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
aaa	0.15			0.0059		
bbb	0.20			0.0079		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

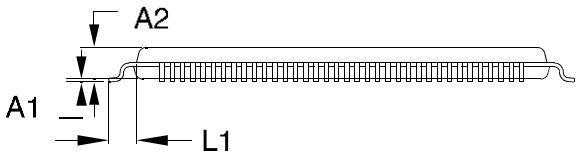
Figure 13-3. 144-lead LQFP Package Drawing



Top View



Bottom View



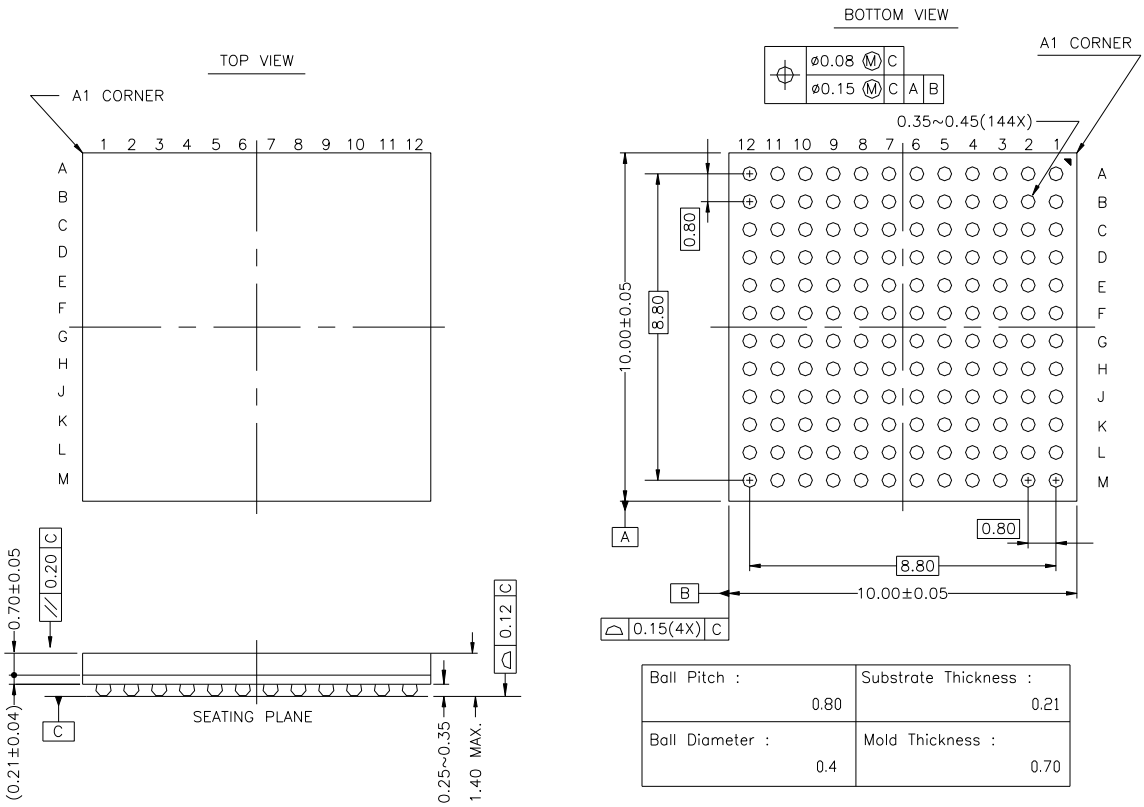
Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.05		0.15	6
A2	1.35	1.40	1.45	
D		22.00 BSC		
D1		20.00 BSC		2, 3
E		22.00 BSC		
E1		20.00 BSC		2, 3
e		0.50 BSC		
b	0.17	0.22	0.27	4, 5
L1		1.00 REF		

Notes:
1. This drawing is for general information only; refer to JEDEe Drawing MS-026 for additional information.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating place to the lowest point on the package body.

Figure 13-4. 144-ball LFBGA Package Drawing



All dimensions are in mm.

14. Ordering Information

Table 14-1. ATSAM3U4/2/1 Ordering Information

Ordering Code	MRL	Flash (Kbytes)	Package	Package Type	Temperature Operating Range
ATSAM3U4EA-AU	A	256	LQFP144	Green	Industrial -40°C to 85°C
ATSAM3U4EA-CU	A	256	LFBGA 144	Green	Industrial -40°C to 85°C
ATSAM3U4CA-AU	A	256	LQFP 100	Green	Industrial -40°C to 85°C
ATSAM3U4CA-CU	A	256	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3U2EA-AU	A	128	LQFP144	Green	Industrial -40°C to 85°C
ATSAM3U2EA-CU	A	128	LFBGA144	Green	Industrial -40°C to 85°C
ATSAM3U2CA-AU	A	128	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3U2CA-CU	A	128	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3U1EA-AU	A	64	LQFP144	Green	Industrial -40°C to 85°C
ATSAM3U1EA-CU	A	64	LFBGA144	Green	Industrial -40°C to 85°C
ATSAM3U1CA-AU	A	64	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3U1CA-CU	A	64	TFBGA100	Green	Industrial -40°C to 85°C

Revision History

In the tables that follow, the most recent version of the document appears first.

"rfo" indicates changes requested during the review and approval loop.

Doc. Rev 6430CS	Comments	Change Request Ref.
	Section 2. "SAM3U Block Diagram", changed orientation of block diagrams. Section 5. "Power Considerations", fixed grammar in Voltage ranges. Section 3. "Signal Description", USART signal DCD0 is an Input	rfo 6681
	Figure 5-1 "Single Supply", Main supply range is 1.8V-3.6V. Figure 5-1, Figure 5-2, Figure 5-3, updated "Note" below figures, "With Main Supply <2.0V USB and ADC are not usable.	6698
	Section 5.5 "Low Power Modes", stray references to WUPx pins, renamed WKUPx	6711
	Table 5-1, "Low Power Mode Configuration Summary", updated footnote "5".	6964
	Table 11-2, "Multiplexing on PIO Controller A (PIOA)", TWD1 and TWCK1 only available on 144-pin version.	6686
	Section 10.13 "Chip Identification" Table 10-2, "SAM3U Chip IDs Register - Revision A Parts", added to datasheet. Section 12.4 "Universal Synchronous Asynchronous Receiver Transmitter (USART)..."SCK up to MCK/6"	6951 rfo–7097

Doc Rev 6430BS	Comments	Change Request Ref.
	Introduction: Section 1. "SAM3U Description", Updated: 52 Kbytes of SRAM. 4x USARTs (SAM3U1C/2C/4C have 3), up to 2x TWIs (SAM3U1C/2C/4C have 1), up to 5x SPIs SAM3U1C/2C/4C have 4), Table 1-1, "Configuration Summary",EBI column updated, 8 bits for SAM3U1C/2C/4C SAM3U4/3/2C rows FWUP replaces NO in FWUP,SHDN pins column	6400 6642
	Figure 2-1 "144-pin SAM3U4/2/1E Block Diagram" and Figure 2-2 "100-pin SAM3U4/2/1C Block Diagram" updated, SM cell removed; UART moved to peripheral area, added Flash Unique block, removed 12B from ADC block, added SysTick counter and Fmax 96 MHz to M3 block. FWUP replaces WKUP in fig 2-1, FWUP added to fig 2-2 Figure 2-2 "100-pin SAM3U4/2/1C Block Diagram", NWR1/NBS1, NXRP0, A0 removed from block diagram.	6482/6642 rfo
	Table 3-1, "Signal Description List", Schmitt Trigger added "PIO Controller - PIOA - PIOB - PIOC". exception details given in footnote. VDDIN, VDDOUT added to table. "Serial Wire/JTAG Debug Port (SWJ-DP)" replaced ICE and JTAG. This section of the table updated status of pulldowns and pullups specified.	6480 rfo
	Section 4. "Package and Pinout", reorganized according to product. Section 4.1 "SAM3U4/2/1E Package and Pinout" and Section 4.2 "SAM3U4/2/1C Package and Pinout", pinouts finalized in datasheet.	6471/rfo 6607
	Section 5.5.1 "Backup Mode", BOD replaced by Supply Monitor/SM. FWUP →Falling Edge Detector. Figure 5-4 "Wake-up Source", BODEN replaced by SMEN. Table 5-1, "Low Power Mode Configuration Summary", PIO state in Low Power Modes, backup mode is; "Previous state saved.	rfo 6645
	Section 6.6 "NRSTB Pin", VDDIO changed to VDDBU Section 6. "Input/Output Lines", replaces Section 5.8 "Programmable I/O Lines". Section 6.1 "General Purpose I/O Lines (GPIO)" and Section 6.2 "System I/O Lines", replace Section 6. "I/O Line Considerations". Figure 6-1 "On-Die Termination schematic", added. Section 6.8 "PIO Controllers", removed. Section 8. "Product Mapping", title changed from "Memories". Section 9. "Memories", now comprises Section 9.1 "Embedded Memories" and Section 9.2 "External Memories". Section 9.1.3.5 "Security Bit Feature", updated	6646 6481/rfo
	Table 7-3, "SAM3U Master to Slave Access", Slave 9, High Speed Peripheral Bridge line added. Section 7.2 "APB/AHB Bridges", reference to ADC updated "10-bit ADC, 12-bit ADC (ADC12B)". Table 11-3, "Multiplexing on PIO Controller B (PIOB)", ADC12B2, ADC12B3 properly listed. Section 12.10.1 "12-bit High Speed ADC", Section 12.10.2 "10-bit Low Power ADC", titles changed. "Quadrature Decoder Logic" on page 51, properly stated in list of TC functions.	6663 6397
	Section 12.10.1 "12-bit High Speed ADC", 2nd item on list updated. Section 12.10.2 "10-bit Low Power ADC", Ksample values updated on 2nd item of list.	rfo

Doc. Rev	Comments	Change Request Ref.
6430AS	First issue	

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