AN5733

Dual Attenuator

■ Outline

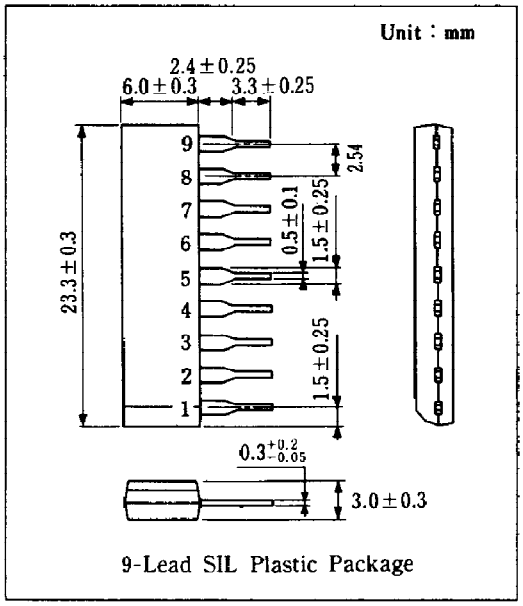
The AN5733 is an integrated circuit designed for dual attenuator and is in SIL package. With this, sets can be made compact.

■ Features

- Output DC control
- Linear Output response
- Two attenuators controlled by one volume control
- Large attenuation
- Small crosstalk and level difference between the two channels

■ Use

- Volume control, etc.

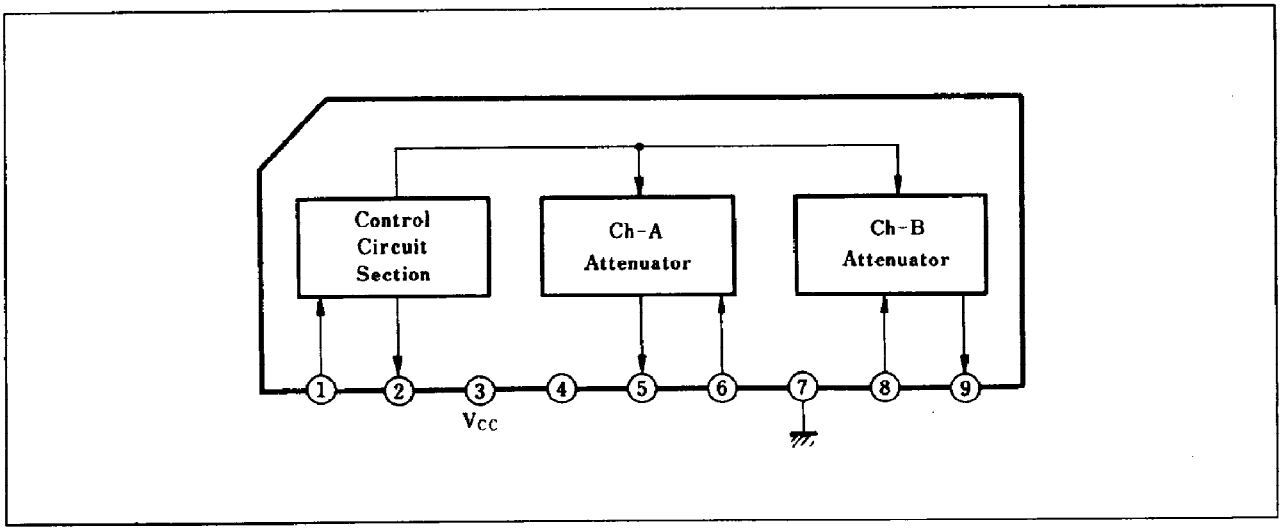


9-Lead SIL Plastic Package

■ Pin

Pin No.	Pin Name
1	Control Voltage
2	Ref. Voltage
3	Vcc
4	Decoupling
5	Ch.A Output
6	Ch.A Input
7	GND
8	Ch.B Input
9	Ch.B Output

■ Block Diagram



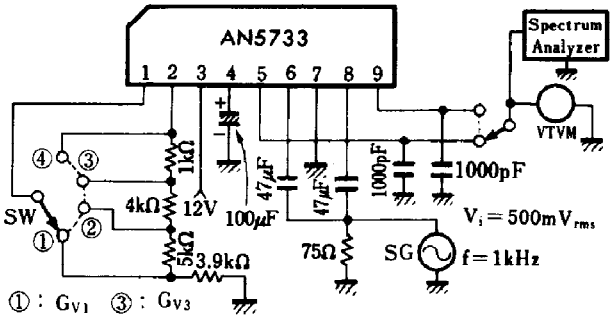
■ Absolute Maximum Ratings (Ta=25°C)

Item		Symbol	Rating	Unit
Supply Voltage		V_{CC}	14.4	V
Power Dissipation		P_D	197	mW
Temperature	Operating Ambient Temperature	T_{opr}	−20～+70	°C
	Storage Temperature	T_{stg}	−40～+150	°C

■ Electrical Characteristics (V_{CC}=12V, Ta=25°C)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Total Circuit Current	I_{tot}			9.5	11.3	13.5	mA
Voltage Gain (1)	$G_{V1\ V1}$	1	f=1kHz, V_i=500mV$_{rms}$ At VR max.	4	6	7.6	dB
Voltage Gain Difference Between Channels (1)	$\Delta G_{V(1)}$	1		−1.5		1.5	dB
Voltage Gain (2)	$G_{V(2)}$	1		−2	0	2.2	dB
Voltage Gain Difference Between Channels (2)	$\Delta G_{V(2)}$	1		−2		2	dB
Voltage Gain (3)	$G_{V(3)}$	1		−20	−16	−12	dB
Voltage Gain Difference Between Channels (3)	$\Delta G_{V(3)}$	1		2.5		2.5	dB
Attenuation (max.)	A_{tt}	1		75			dB
Separation	Sep	2		70			dB
Input Resistance	Ri	3	f=1kHz		25		kΩ
Output Resistance	R_O	4			1.7		kΩ
Ripple Rejection Ratio	RR			34			dB

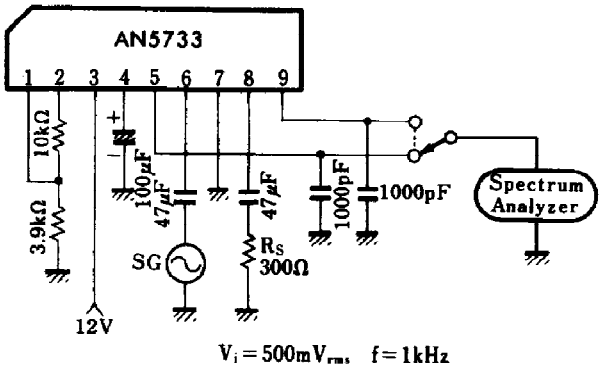
Test Circuit 1 ($G_{V(1-3)}$, $\Delta G_{V(1-3)}$, Att)



① : G_{V1} ③ : G_{V3}
② : G_{V2} ④ : Att

- Circuit voltage gain : Gain between Pins ⑤ and ⑥
- Voltage gain difference between channels : Output level difference between Pins ① and ⑤

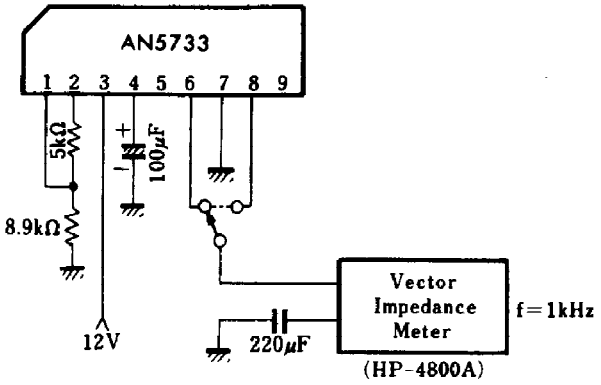
Test Circuit 2 (Sep)



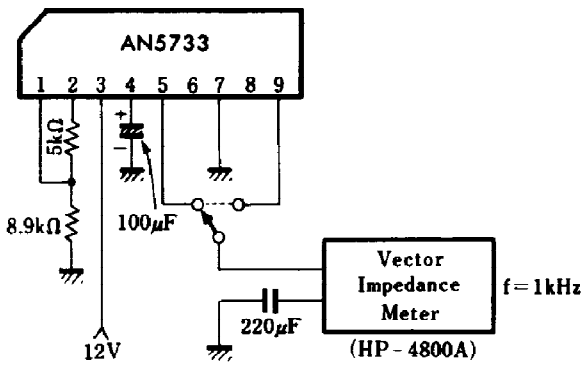
V_i=500mV$_{rms}$, f=1kHz

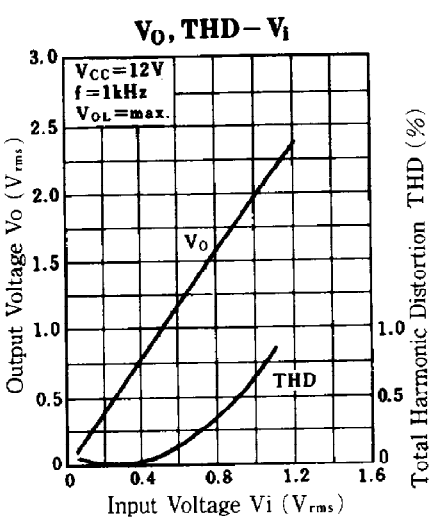
- Level difference between Pins ⑤ and ⑨

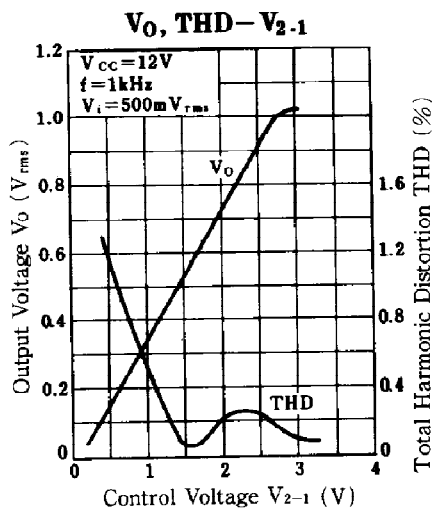
Test Circuit 3 (R_i)

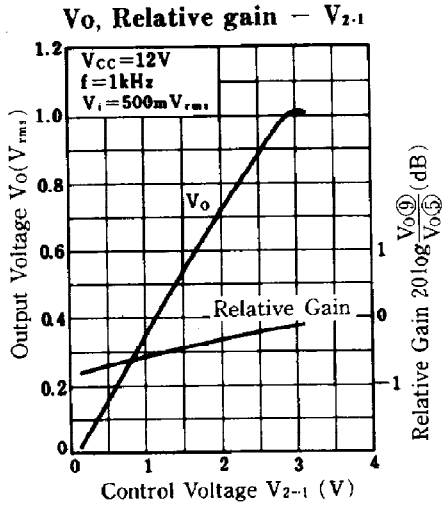


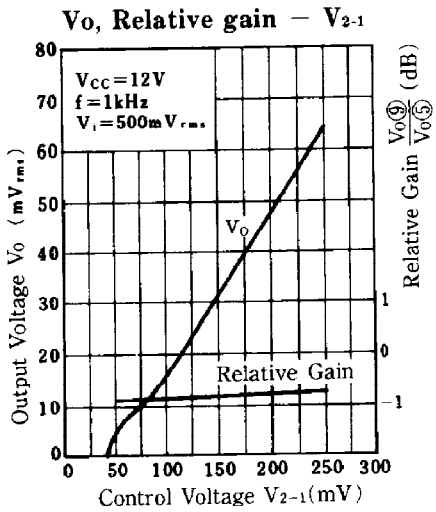
Test Circuit 4 (R_O)

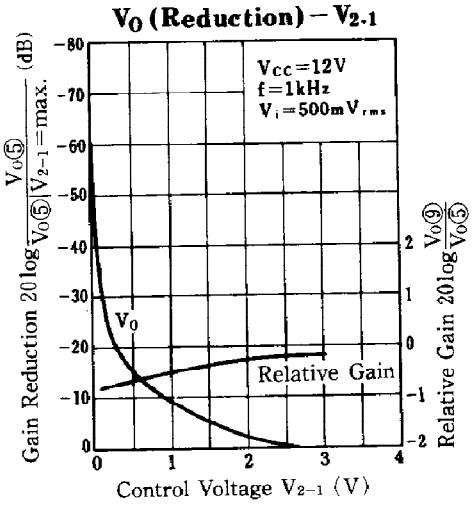


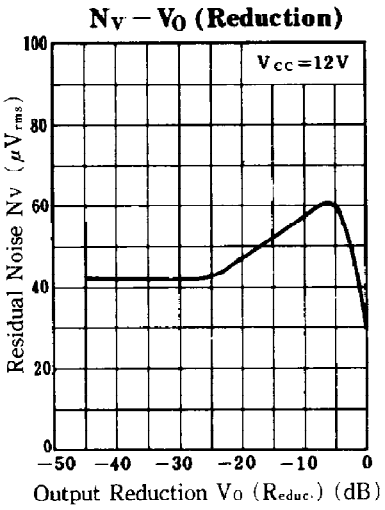












■ Application Circuit