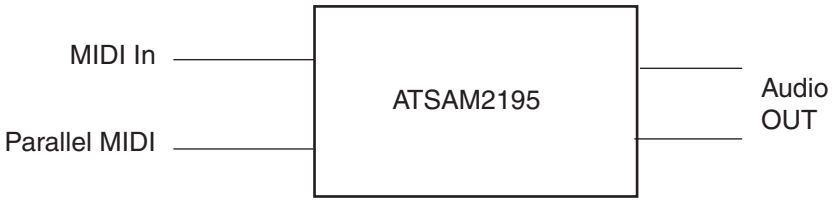
Features

- **Single Chip All-in-one Design**
  - **MIDI Control Processor, Serial and Parallel Interface**
  - **Synthesis, General MIDI Wavetable Implementation**
  - **General MIDI Compatible Effects: Reverb + Chorus**
  - **Spatial Effect**
  - **4-band Stereo Equalizer**
  - **Stereo DAC. DR: 86 dB min, THD+N: -80 dB max**
- **State of the art Synthesis for Products Providing Best Quality for Price**
  - **64-voice Polyphony (without effects)**
  - **38-voice Polyphony + Effects**
  - **On-chip CleanWave™ Wavetable Data, Firmware, RAM Delay Lines**
- **Audio Stereo Line Output**
- **Typical Applications: Battery Operated Musical Keyboards, Portable Phones, Karaokes**
- **QFN44 (7mm x 7mm) Package: Small Footprint, Small Pin Count**
- **Low Power**
  - **75 mW typ. Operating**
  - **Single 3.3V or Single 1.8V Power Supply**
  - **Built-in Power Switch and 3.3V to 1.8V Regulator**

1. Typical Hardware Configuration

Figure 1-1. Typical Hardware Configuration



Audio Processing

ATSAM2195 Low-power Single Chip Synthesizer with Effects

6308A–DRMSD–10-May-07

2. Pin Description

2.1 Pins By Function – 44-lead QFN Package

Table 2-1. Power Supply Group

Pin Name	Pin #	Type	Function
GND	20, 31, 33	PWR	DIGITAL GROUND All pins should be connected to a ground plane
GND	exposed die pad	PWR	DIGITAL GROUND Ground supply; down bonded to the exposed die pad (heatsink). It is recommended, but not obligatory, to connect this pad to a ground plane during PCB layout
VD33	21	PWR	I/O POWER SUPPLY This pin should be connected to a nominal 3.3V power for 3.3V single supply applications. This pin should be connected to a nominal 1.8V power for 1.8V single supply applications
VD18	19, 30	PWR	CORE POWER SUPPLY These pins should be connected to nominal 1.8V. 3.3V single supply application: If the built-in regulator is used, then these pins should be connected to the output of the regulator OUTVC18 (pin 35). 1.8V single supply application: If the built-in power switch is used for minimum power down consumption, then all these pins should be connected to the output of the power switch PWROUT (pin 39).
AGND	43, 44	PWR	ANALOG GROUND These pins should be connected to an analog ground plane
VA33	4	PWR	DAC PERIPHERY ANALOG SUPPLY 3.3V single supply application: This pin should be connected to a nominal 3.3V power through a serial inductor filter (better result) or a 10 ohm resistor. 1.8V single supply application: This pin should be connected to a nominal 1.8V power through a serial inductor filter (better result) or a 10 ohm resistor.
VA18	2	PWR	DAC 1.8V ANALOG SUPPLY This pin should be connected to a clean 1.8V. 3.3V single supply application: If the built-in regulator is used, then this pin should be connected to the output of the regulator OUTVC18 (pin 35) through a serial inductor filter (better result) or a 10 ohm resistor. 1.8V single supply application: If the built-in power switch is used, then this pin should be connected to the output of the power switch PWROUT (pin 39) through a serial inductor filter (better result) or a 10 ohm resistor.
REGIN	34	PWR	Regulator input This pin should be connected to a nominal 3.3V power for 3.3V single supply applications. This pin should be grounded for 1.8V single supply applications
PWRIN	38	PWR	Power switch input. This pin should be left not connected for 3.3V single supply applications. This pin should connected to a 1.8V nominal power for 1.8V single supply applications

Table 2-2. Serial MIDI, parallel MIDI (MPU-401)

Pin Name	Pin #	Type	Function
MIDI IN	10	IN	Serial TTL MIDI IN. Connected to the built-in synthesizer at power-up or after MPU reset. Connected to the D0-D7 bus (read mode) when MPU switched to UART mode. This pin should be tied HIGH if not used.
D0-D7	15, 16, 17, 18, 22, 23, 24, 25	I/O	8 bit bi-directional bus, under control of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$. These pins have a built-in pull down. They should be left unconnected if not used
A0	11	IN	Select data(0) or control(1) for write, data(0) or status(1) for read. This pin has a built-in pull-down. It should be left unconnected if not used.
$\overline{CS}$	12	IN	Chip select, active low. This pin has a built-in pull up. It should be left unconnected if not used.
$\overline{RD}$	13	IN	Read, active low. When $\overline{CS}$ and $\overline{RD}$ are low, data(A0=0) or status(A0=1) is read on D0-D7. Read data is acknowledged on the rising edge of $\overline{RD}$. This pin has a built-in pull up. It should be left unconnected if not used.
$\overline{WR}$	14	IN	Write, active low. When $\overline{CS}$ and $\overline{WR}$ are low, data (A0=0) or control (A0=1) is written from the D0-D7 bus to the ATSAM2195 on the rising edge of $\overline{WR}$. This pin has a built-in pull up. It should be left unconnected if not used.
IRQ	26	OUT	A rising edge indicates that a MIDI byte is available for read on D0-D7. Acknowledged by reading the byte.

Table 2-3. Analog audio group

Pin Name	Pin #	Type	Function
AGNDREF	42	IN	These pin is used as a reference by the internal DAC. It should be connected to a clean analog ground plane
VREF	41	OUT	Reference voltage. Generated on-chip. Should be stabilized by external capacitors 10 µF // 100 nF to AGND.
VCM	40	OUT	On-chip output stage common-mode voltage. Should be stabilized by external capacitors 10 µF // 100 nF to AGND.
VBG	3	OUT	Bandgap voltage. Can be stabilized by capacitors 1µF // 100 nF to AGND. Can be left unconnected for low-cost application.
AOUTL	1	OUT	Left channel audio output
AOUTR	5	OUT	Right channel audio output

Table 2-4. Digital audio group

Pin Name	Pin #	Type	Function
OUTLEV	6	IN	Selects the full scale output level for AOUTL and AOUTR. OUTLEV = 0 for 1.1Vpp OUTLEV = 1 for 2.2Vpp If 1.8V single supply (VA33 = 1.8V), OUTLEV should be tied to 0.
DITH0-DITH1	7, 8	IN	Activate a dither signal to reduce eventual noise tones at the output. See Dither Modes Description.

Table 2-5. Miscellaneous group

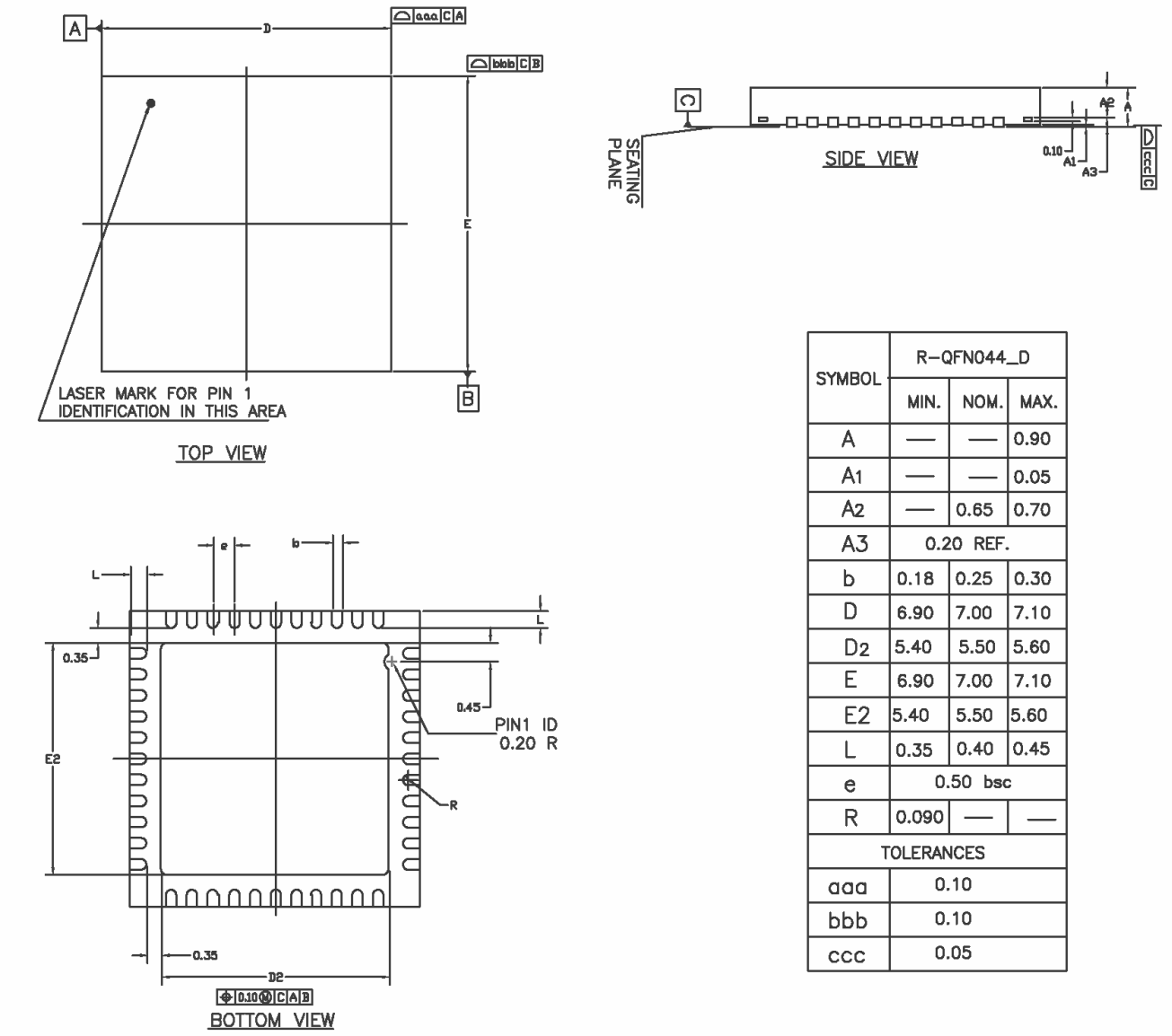
Pin Name	Pin #	Type	Function
X1-X2	29, 28	-	9.6 MHz crystal connection. An external 9.6 MHz clock can also be used on X1 (1.95Vpp max through 47 pF capacitor). X2 cannot be used to drive external circuits.
$\overline{\text{RESET}}$	9	IN	Reset input, active low. This is a Schmitt trigger input, allowing direct connection to an RC network
OUTVC18	35	PWR	3.3V to 1.8 V regulator output. When 3.3V single supply application this pin can be used to power VD18 pins, and VA18 pin through a serial inductor filter (better result) or a 10 ohm resistor. Decoupling capacitors 470 pF in parallel with 2.2 or 4.7 µF must be connected between OUTVC18 and GND.
PWROUT	39	PWR	Power switch output. When 1.8V single supply application this pin can be used to power VD18 pins, and VA18 pin through a serial inductor filter (better result) or a 10 ohm resistor.
$\overline{\text{PDWN}}$	37	IN	Power down, active low. When power down is active, all digital outputs are set to logic level 0, D0-D7 bus is set in high Z, analog outputs decrease to 0V, the PLL and crystal oscillator are stopped. 3.3V single supply application: If the built-in regulator is used then 1.8V supply is removed from the core. To exit from power down, $\overline{\text{PDWN}}$ must be set to VD33, then $\overline{\text{RESET}}$ applied. When unused this pin must be connected to VD33. 1.8V single supply application: If the built-in power switch is used then 1.8V supply is removed from the core. To exit from power down, $\overline{\text{PDWN}}$ must be set to VD18, then $\overline{\text{RESET}}$ applied. When unused this pin must be connected to VD18
TEST0-TEST1-TEST2	36, 27, 32	IN	Test pins. Should be grounded

2.2 Pinout By Pin Number - 44-lead QFN Package

Table 2-6. Pinout

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	AOUTL	12	$\overline{CS}$	23	D5	34	REGIN
2	VA18	13	$\overline{RD}$	24	D6	35	OUTVC18
3	VBG	14	$\overline{WR}$	25	D7	36	TEST0
4	VA33	15	D0	26	IRQ	37	$\overline{PDWN}$
5	AOUTR	16	D1	27	TEST1	38	PWRIN
6	OUTLEV	17	D2	28	X2	39	PWROUT
7	DITH0	18	D3	29	X1	40	VCM
8	DITH1	19	VD18	30	VD18	41	VREF
9	$\overline{RESET}$	20	GND	31	GND	42	AGNDREF
10	MIDI IN	21	VD33	32	TEST2	43	AGND
11	A0	22	D4	33	GND	44	AGND

3. Mechanical Dimensions – 44-lead QFN Package



SYMBOL	R–QFN044_D		
	MIN.	NOM.	MAX.
A	—	—	0.90
A1	—	—	0.05
A2	—	0.65	0.70
A3	0.20 REF.		
b	0.18	0.25	0.30
D	6.90	7.00	7.10
D2	5.40	5.50	5.60
E	6.90	7.00	7.10
E2	5.40	5.50	5.60
L	0.35	0.40	0.45
e	0.50 bsc		
R	0.090	—	—
TOLERANCES			
aaa	0.10		
bbb	0.10		
ccc	0.05		

Notes: 1. All package dimensions are in mm.
2. R-QFN044_D - QFN

4. Marking

5. Absolute Maximum Ratings

All voltages with respect to 0V, GND=0V.

Table 5-1. Absolute Maximum Ratings*

Temperature under bias	-55° C to +125° C
Storage Temperature	-65°C to +150°C
Voltage on any Input Pins except X1	-0.3V to +VD33+0.3V
Voltage on X1	-0.3V to VD18+0.3V
Supply voltage (I/O) (VD33)	-0.3V to +3.6V
Supply voltage (core) (VD18)	-0.3V to +1.95V
Supply voltage (DAC analog 3.3V) (VA33)	-0.3V to +3.6V
Supply voltage (DAC analog 1.8V) (VA18)	-0.3V to +1.95V
Maximum IOL per I/O pin	4 mA
Maximun IOH per I/O pin	4 mA
Maximum Output current from PWROUT pin (max duration = 1sec) (IPWRO)	650 mA
Maximum Output current from OUTVC18 pin (max duration = 1sec) (IREGO)	100 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5-2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Digital supply voltage: - OUTLEV = 1 - OUTLEV = 0	VD33 VD33	3 1.65	3.3 1.8	3.6 1.95	V V
Digital supply voltage	VD18	1.65	1.8	1.95	V
Analog supply voltage: - OUTLEV = 1 - OUTLEV = 0	VA33 VA33	3 1.65	3.3 1.8	3.6 1.95	V V
Analog supply voltage	VA18	1.65	1.8	1.95	V
Power switch supply	PWRIN	1.75	1.80	1.95	V
Regulator supply	REGIN	2.7	3.3	3.6	V
Power Switch output current	IPWRO	-	-	217	mA
OUTVC18 output current	IREGO	-	60	-	mA
Operating ambient temperature	tA	0	-	+70	°C

Table 5-3. Digital Characteristics (TA=25°C, VD33=3.3V±10%, 1.65 V< VD18 < 1.95V)

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage (Except X1)	VIL	-0.3	-	0.8	V
High level input voltage (Except X1)	VIH	2	-	3.6	V
Low level input voltage for X1	VIL	-0.3	-	0.3	V
High level input voltage for X1	VIH	1.2	-	VD18+0.3	V
Low level output voltage IOL=-2mA	VOL	-	-	0.4	V
High level output voltage IOH=2mA	VOH	VD33-0.4	-	-	V
Power consumption (crystal freq.=9.6MHz)	-	-	75		mW
Power down supply current (using power switch)	-		<1		µA
Drop down from PWRIN to PWROUT (at IPWRO = 180mA)	-			0.1	V
Voltage on OUTVC18 (at IREGO = 60mA)	VREGO	1.65	1.8	1.95	V

Table 5-4. Analog Characteristics (TA=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Total Harmonic Distortion + Noise (at 0 dB, full scale) VA33 = 3.3V, OUTLEV = 1 VA33 = 1.8V, OUTLEV = 0	 THD + N THD + N	 - -	 - -	 -80 -76	 dB dB
Dynamic Range (A-Weighted) VA33 = 3.3V, OUTLEV = 1 VA33 = 1.8V, OUTLEV = 0	 DR DR	 86 80	 - -	 - -	 dB dB
Inter-channel isolation (1kHz) VA33 = 3.3V, OUTLEV = 1 VA33 = 1.8V, OUTLEV = 0	 -	 83 80	 -	 -	 dB
Inter-channel gain mismatch	-	-0.1	-	+01	dB
Gain drift	-	-	± 100	-	ppm/ °C
Full-scale output voltage VA33 = 3.3V, OUTLEV = 1 VA33 = 1.8V or 3.3V, OUTLEV = 0	 - -	 2.04 1.02	 2.2 1.1	 2.36 1.18	 Vpp Vpp
VCM Maximum allowable DC current source	-	-	-	0.1	mA
VCM Nominal voltage VA33 = 3.3V, OUTLEV = 1 VA33 = 1.8V or 3.3V, OUTLEV = 0	 - -	 1.38 0.74	 1.5 0.80	 1.58 0.84	 V V
AC-Load resistance	RL	3	4.7		kΩ
Load capacitance	CL	-	10	100	pF

Table 5-5. Filter Characteristics (TA=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Frequency response (10Hz – 17kHz)	-	-0.05	-	+0.05	dB
Passband to -0.1dB corner to -6 dB corner	 PB PB	 0 0	 - -	 17 18.74	 kHz kHz
Stopband	SB		20.49		kHz
Stopband attenuation (20.49kHz – 112.5kHz)	SA	65	-	-	dB
Group delay	GD		1.12		ms
Gain drift	-	-	± 100	-	ppm/ °C

6. Timings

6.1 Slave 8-bit Parallel Interface

This interface is typically used to connect the chip to an host processor.

Figure 6-1. 8-bit Parallel Interface Read Cycle

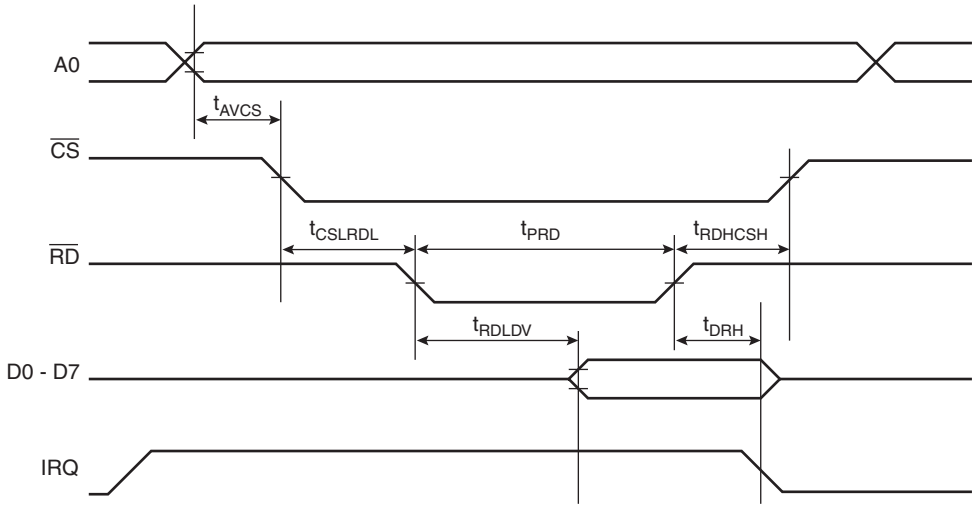


Figure 6-2. 8-bit Parallel Interface Write Cycle

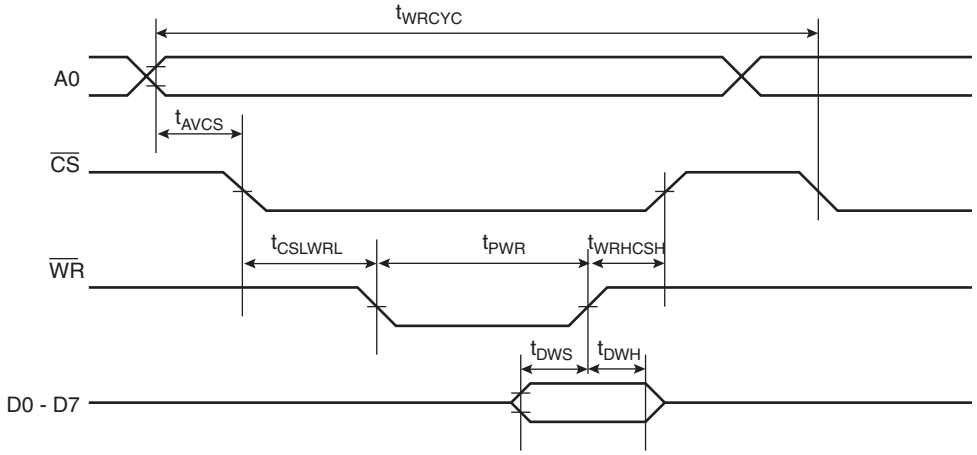


Table 6-1. Timings

Parameter	Symbol	Min	Typ	Max	Unit
Address valid to chip select low	t_{AVCS}	0	-	-	ns
Chip select low to $\overline{RD}$ low	t_{CSLRDL}	5	-	-	ns
$\overline{RD}$ high to $\overline{CS}$ high	t_{RDHCSH}	5	-	-	ns
$\overline{RD}$ pulse width	t_{PRD}	50	-	-	ns
Data out valid from $\overline{RD}$	t_{RDLDV}	-	-	20	ns
Data out hold from $\overline{RD}$	t_{DRH}	5	-	10	ns

Table 6-1. Timings

Chip select low to $\overline{WR}$ low	$t_{CSLRWRL}$	5	-	-	ns
$\overline{WR}$ high to $\overline{CS}$ high	t_{WRHCSH}	5	-	-	ns
$\overline{WR}$ pulse width	t_{PWR}	50	-	-	ns
Write data setup time	t_{DWS}	10	-	-	ns
Write data hold time	t_{DWH}	0	-	-	ns
Write cycle	t_{WRCYC}	3.5			µs

Notes:
1. When data is pending on parallel port, the host should read it within 1 ms. If not, the parallel port is deactivated. Reactivating the port can be done with the following control sequence: 0FFh (Closed port), 03FFh (Open port).
2. For safe operation, write cycle time should not be lower than 3.5 µs.

7. Reset and Power Down

During power-up, the $\overline{\text{RESET}}$ input should be held low until the crystal oscillator and PLL are stabilized, which can take about 20 ms. A typical RC/diode power-up network can be used.

After $\overline{\text{RESET}}$, the ATSAM2195 enters an initialization routine. It takes around 50 ms before a MIDI IN or MPU message can be processed.

Audio begins after 500 ms, maximum.

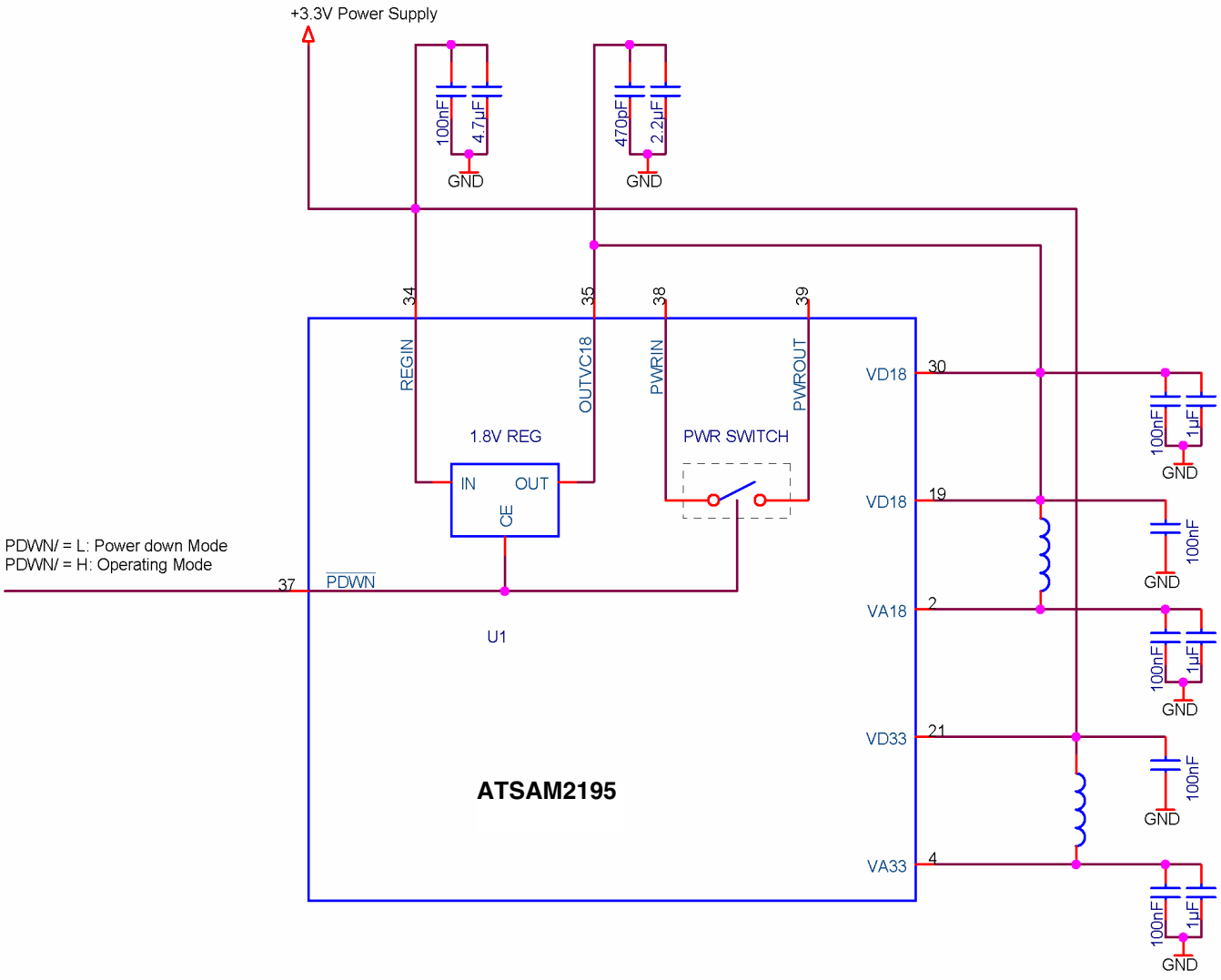
To enter power-down, Reset should be held low 500 ms min and then $\overline{\text{PDWN}}$ asserted low.

In Power-down mode, the crystal oscillator and PLL are stopped. The chip enters a deep power down sleep mode.

To exit power down, $\overline{\text{PDWN}}$ has to be asserted high, then $\overline{\text{RESET}}$ applied.

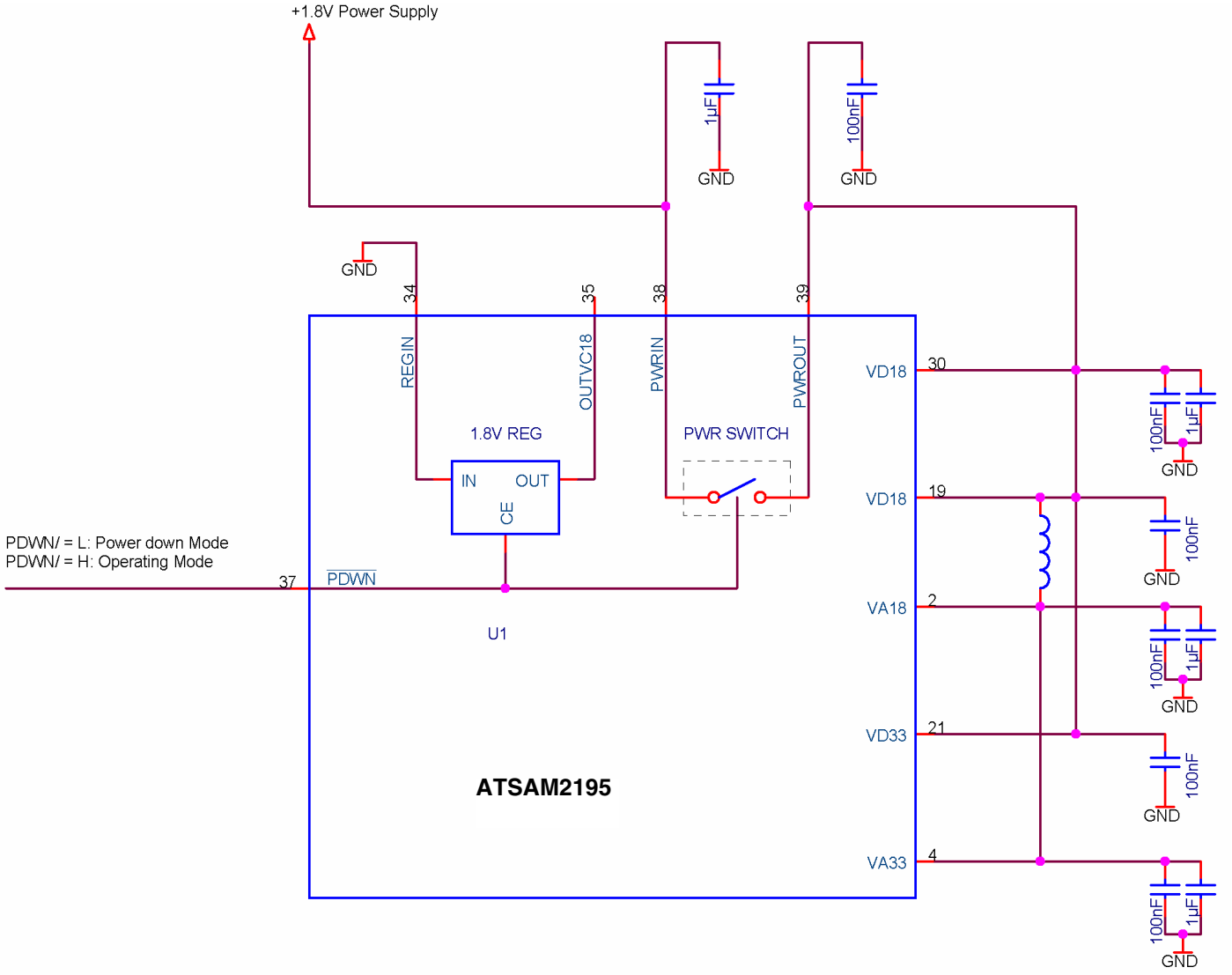
7.1 3.3V Single Supply Application

Power down mode is managed by the internal regulator. The equivalent schematic and standard connection is shown on the diagram below.



7.2 1.8V Single Supply Application

Power down mode is managed by the internal power switch. The equivalent schematic and standard connection is shown on the diagram below.



8. Dither Modes Description (Dithering Signal Programmability)

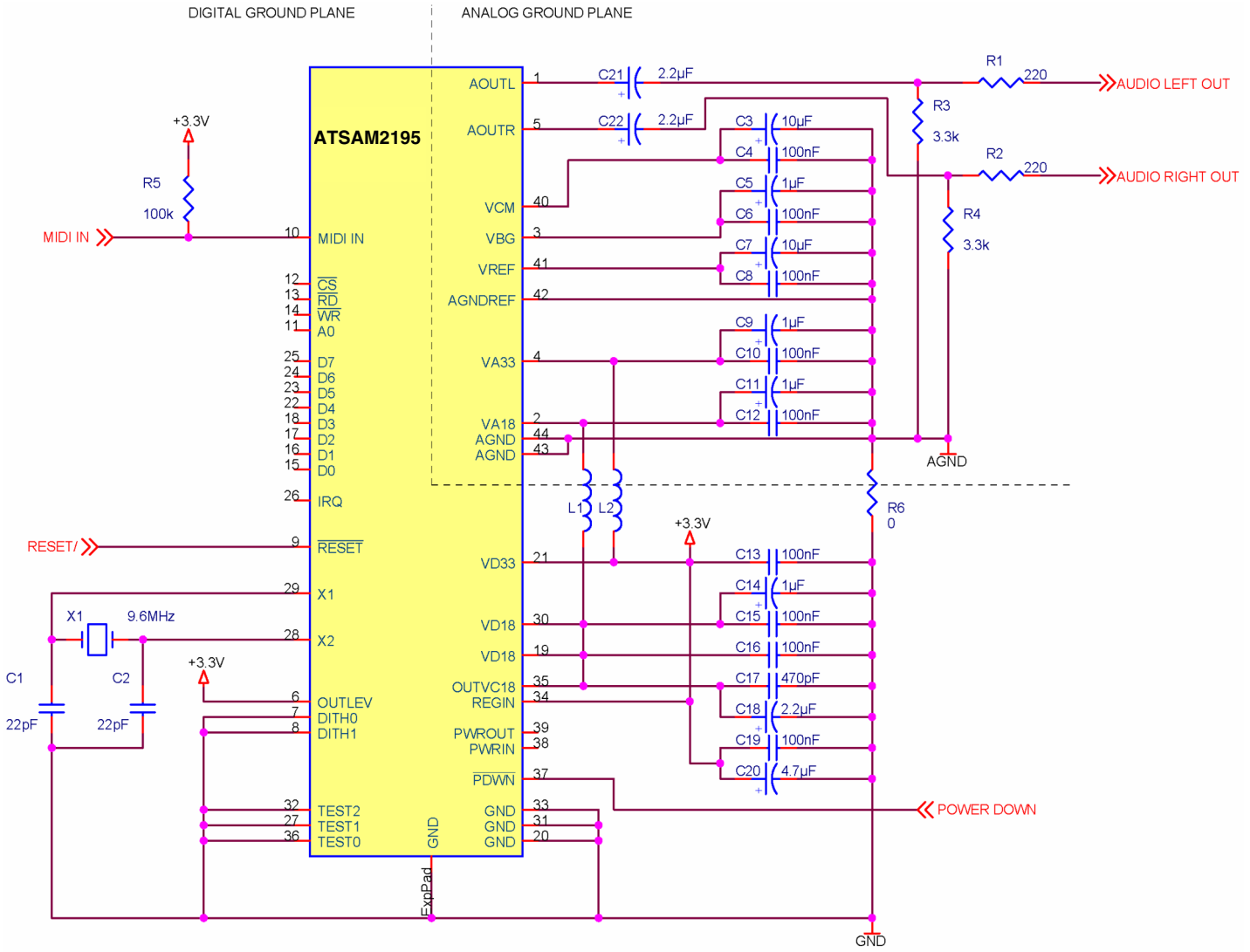
Dithering is used to attenuate the so-called idle tones caused by correlation between DAC input signal and truncation noise. This correlation manifests as spurious signals in the audio band and hence can be perceived by the user. The addition of a random digital signal to the truncator input in the digital modulator has been proven to be very effective to reduce the presence of idle tones. However, this is actually a noisy signal so that its power must be traded-off with the required dynamic range. For better control, the ATSAM2195 allows programmability of the dithering signal power as shown below.

dith[1:0]	Mode description	Comments
00	No dither	
01	Dither signal power = -30dBFS	Minimum recommended dither.
10	Dither signal power = -27dBFS	Typical value
11	Dither signal power = -24dBFS	Maximum recommended value. Above it dither noise may become dominant.

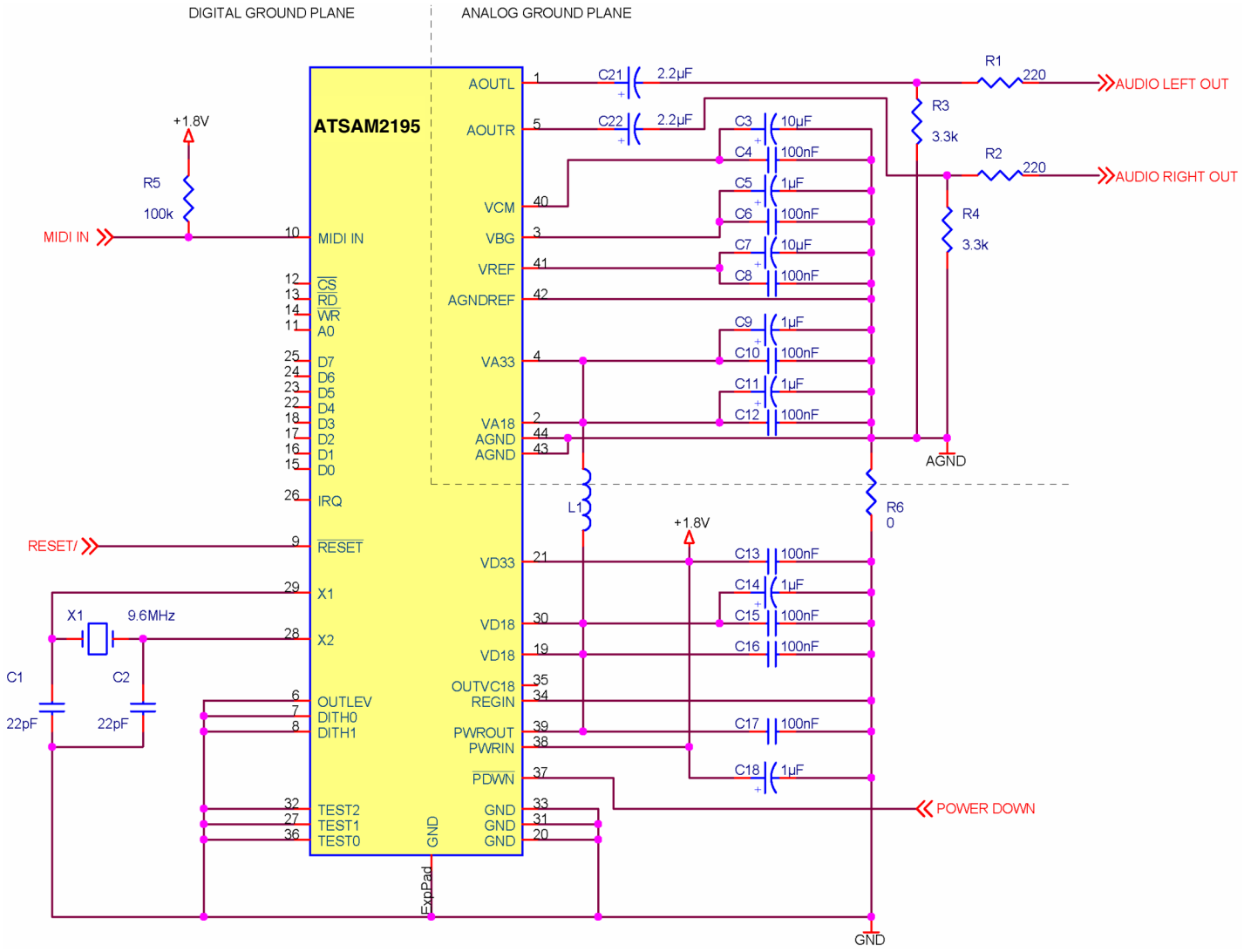
9. System Design

The schematics of this section are the reference designs for applications with ATSAM2195. The conformity with these schematics ensures the best performance.

9.1 3.3V Single Supply Application



9.2 1.8V Single Supply Application



10. Recommended Board Layout

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations:

- GND, VD33, VD18, VA33, VA18 distribution and decoupling

All GND, VD33, VD18, VA33, VA18 pins should be connected. A GND plane is strongly recommended below the ATSAM2195. The board GND, VD33, VD18 distribution should be in grid form. Recommended decoupling is 0.1 µF at each VD33, VD18, VA33, VA18 pin of the IC with an additional 1µF-T between pins 30 and 31. Decoupling capacitors should be implemented close to the IC.

- Crystal

The paths between the crystal and the ATSAM2195 should be short and shielded. The ground return from the crystal compensation capacitors should be pin 31.

- Analog section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane.

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