DATASHEET

1. Fema Part Number

GM1601289-17-OLX2NLF	
Description	1.69" 160 X 128 FULL COLOR OLED DISPLAY
	ROHS Compliant

Customer Approval

Customer Approval Signature	
Approval Date	

Revision History

Revision	Date	Page	Comment

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1. Basic Specifications

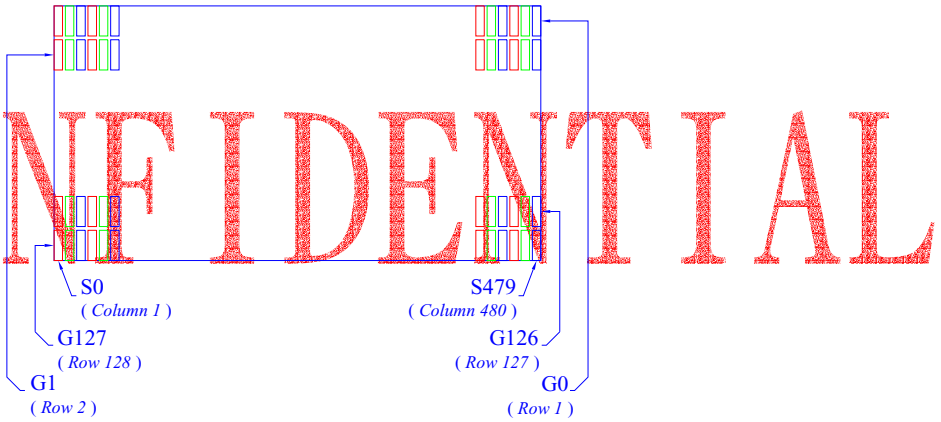
1.1 Display Specifications

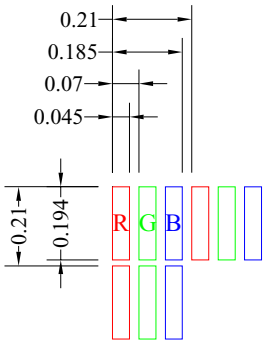
1) Display Mode: Passive Matrix
2) Display Color: 262,144 Colors (Maximum)
3) Drive Duty: 1/128 Duty

1.2 Mechanical Specifications

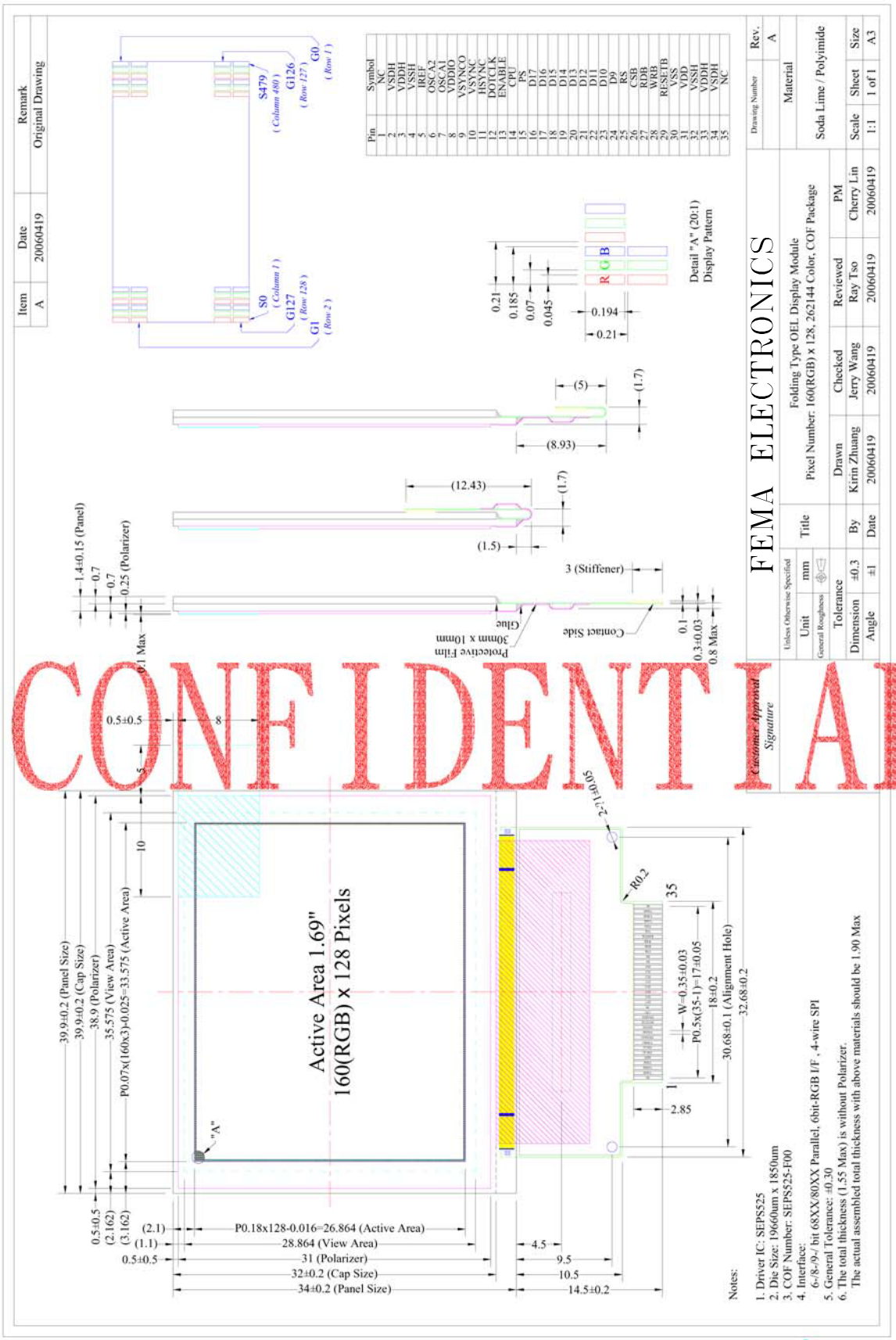
1) Outline Drawing: According to the annexed outline drawing number
2) Number of Pixels: 160 (RGB) × 128
3) Panel Size: 39.90 × 34.00 × 1.80 (mm)
4) Active Area: 33.575 × 26.864 (mm)
5) Pixel Pitch: 0.07 × 0.21(mm)
6) Pixel Size: 0.045 × 0.194 (mm)
7) Weight: 4.5 (g)

1.3 Active Area & Pixel Construction





1.4 Mechanical Drawing



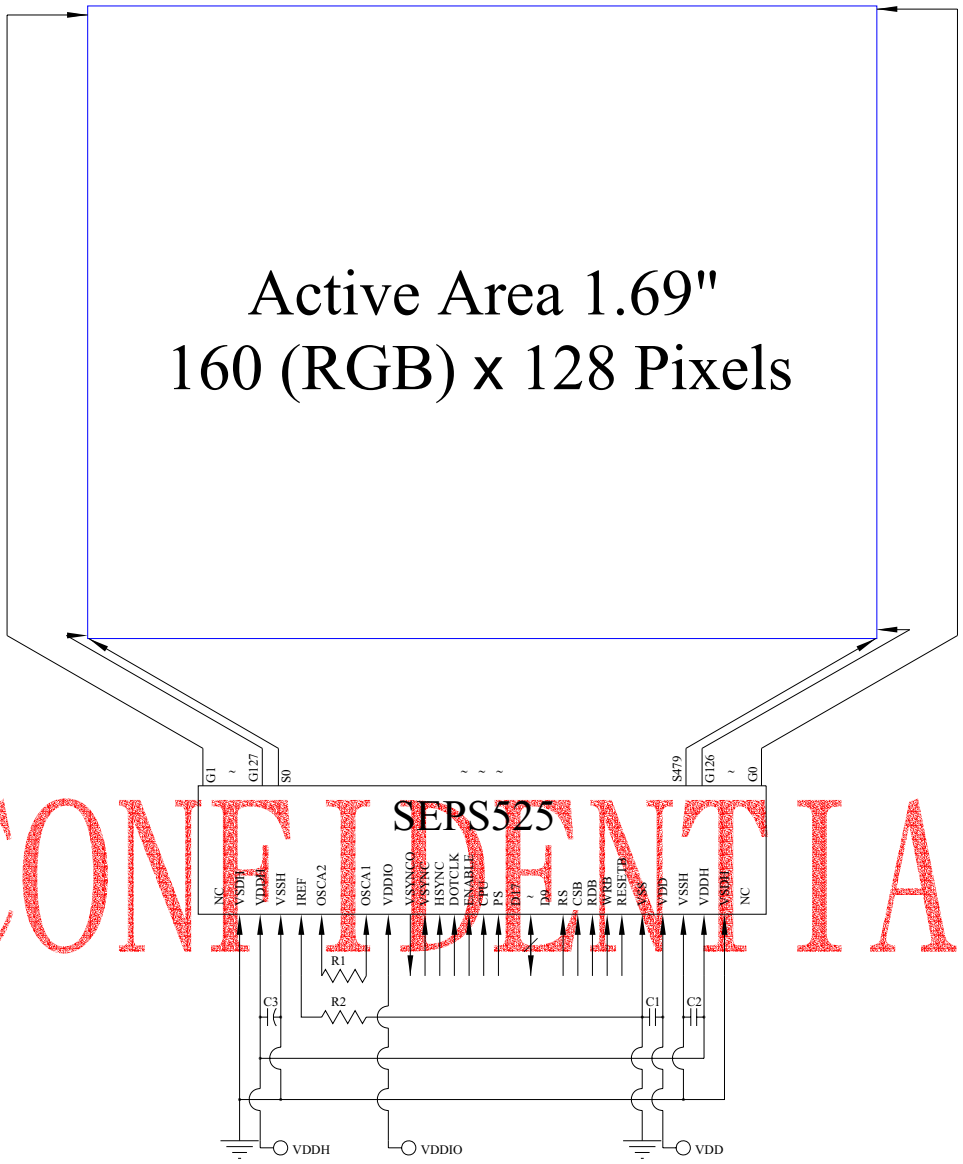
1.5 Pin Definition

Pin Number	Symbol	Type	Function
Power Supply Pins			
4,32	VSDH	P	*Data Driver Ground*
2,33	VSSH	P	*Scan Driver Ground*
3,34	VDDH	P	*Data, Scan Driver Power Supply.*
30	VSS	P	*Logic Ground*
31	VDD.	P	*Logic Power Supply.*
8	VDDIO	P	*MPU I/F PAD Power Supply*
System Control Pins			
5	IREF	I	*Current Reference for Brightness Adjustment* Tie 68KΩ resistor to VSS.
6	OSCA2	O	*Fine adjustment for oscillation* Tie 10 KΩ resistor to OSCA1 between OSCA2. When the external clock mode is selected, OSCA1 is used external clock input.
7	OSCA1	I	
14	CPU	I	*Selects the CPU type* Low: 80-series CPU, High: 68-Series CPU.
15	PS	I	*Selects parallel/Serial interface type* Low: serial, High: parallel.
MPU Interface Pins			
9	VSYNCO	O	*RGB Mode Functional Pins* VSYNCO: Vertical Sync. Output VSYNC: Vertical Sync. Input HSYNC: Horizontal Sync. Input DOTCLK: Dot Clock Input ENABLE: Video Enable Input
10	VSYNC	I	
11	HSYNC	I	
12	DOTCLK	I	
13	ENABLE	I	
16~24	D17~D9	I/O	*Host Data Input/Output Bus* These pins are 9-bit bi-directional data bus to be connected with MCU data bus. PS: 1 → 8_bit bus : D[17:10]; 9_bit bus : D[17:9] PS: 0 → D[17] SCL : Synchronous clock input; D[16] SDI : Serial data input; D[15] SDO : Serial data output Fix unused pins to the VSS level.
25	RS	I	*Selects the data/command* Low: command, High: parameter/data
26	CSB	I	*Chip Select* Low: SEPS525 is selected and can be accessed. High: SEPS525 is not selected and cannot be accessed.
27	RDB	I	*Read or Read/Write Enable* 80-system bus interface: read strobe signal (active low). 68-system bus interface: bus enable strobe (active high). When serial mode, fix it to VDD or VSS level.

1.5 Pin Definition (Continued)

Pin Number	Symbol	Type	Function
MPU Interface Pins (Continued)			
28	WRB	I	*Write or Read/Write Select* 80-system bus interface: write strobe signal (active low). 68-system bus interface: read/write select. Low: write, High: read. When serial mode, fix it to VDD or VSS level.
29	RESETB	I	*Chip Reset* Reset SEPS525 (active low)
Reserved Pins			
1,35	NC	-	*No Connection*

1.6 Block Diagram



MCU Interface Selection: PS, CPU

Pins connected to MCU interface: D17~D9, RS, CSB, RDB, WRB, RESETB, ENABLE, DOTCLK, HSYNC, and VSYNC

* When RGB mode is used, D[17:12], ENABLE, DOTCLK, HSYNC, and VSYNC should follow the 6-bit RGB interface instruction. Otherwise, ENABLE, DOTCLK, HSYNC, and VSYNC these four input signal should be tie to VSS level, and VSYNCO should be floating.

C1:	1μF
C2, C3:	4.7μF
R1:	10kΩ
R2:	68kΩ

2. *Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	VDD	-0.3	4	V	1, 2
Supply Voltage for I/O Pins	VDDIO	-0.3	4	V	1, 2
Driver Supply Voltage	VDDH	-0.3	19.5	V	1, 2
Operating Temperature	T_{OP}	-30	70	°C	-
Storage Temperature	T_{STG}	-40	80	°C	-

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3. Electrical Characteristics

3.1 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VDD		2.6	2.8	3.3	V
Supply Voltage for I/O Pins	VDDIO		1.6	2.8	3.3	V
Driver Supply Voltage	VDDH		13.5	14.0	14.5	V
High Level Input	V_{IH}		0.8×VDD	-	VDD	V
Low Level Input	V_{IL}		0	-	0.4	V
High Level Output	V_{OH}		VDD-0.4	-	-	V
Low Level Output	V_{OL}		-	-	0.4	V

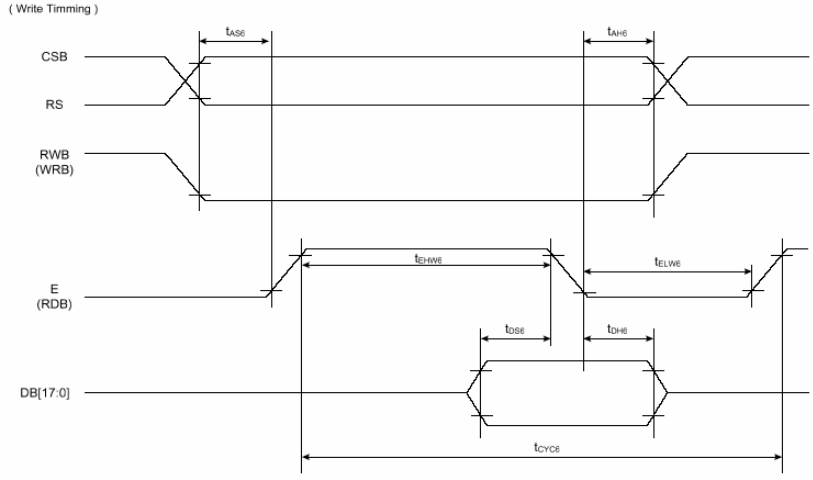
3.2 AC Characteristics

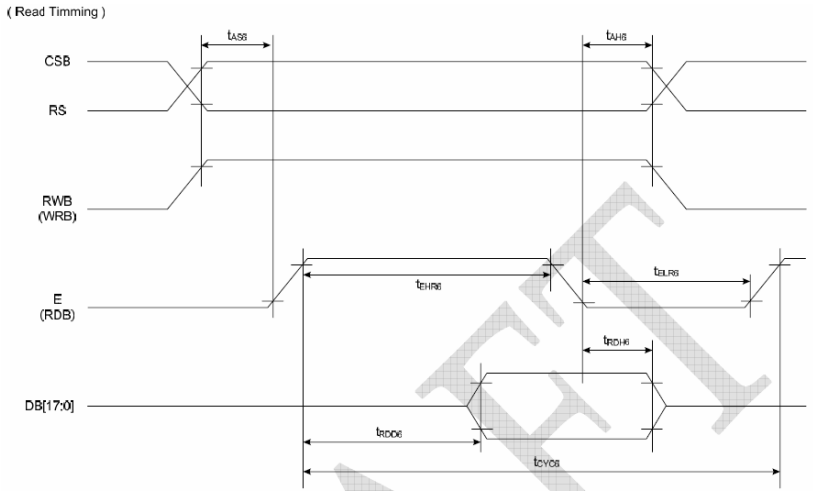
3.2.1 68XX-Series MPU Parallel Interface Timing Characteristics:

(VDD = 2.8V, Ta = 25℃)

Item	Symbol	Condition	Min	Max	Unit	Port
Write Timing						
Address hold timing Address setup timing	t_{AH6} t_{AS6}	-	5 5	-	ns	CSB RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC6} t_{ELW6} t_{EHW6}	-	100 45 45	-	ns	E
Data setup timing Data hold Timing	t_{DS6} t_{DH6}		40 10	-	ns	DB[17:0]
Read Timing						
Address hold timing Address setup timing	t_{AH6} t_{AS6}	-	10 10	-	ns	CSB RS
System cycle timing Read "L" pulse width Read "H" pulse width	t_{CYC6} t_{ELR6} t_{EHR6}	-	200 90 90	-	ns	E
Read data output delay time Data hold Timing	t_{RDD6} t_{RDH6}	C_L = 15pF	0	70	ns	DB[17:0]

*) All the timing reference is 10% and 90% of VDD.



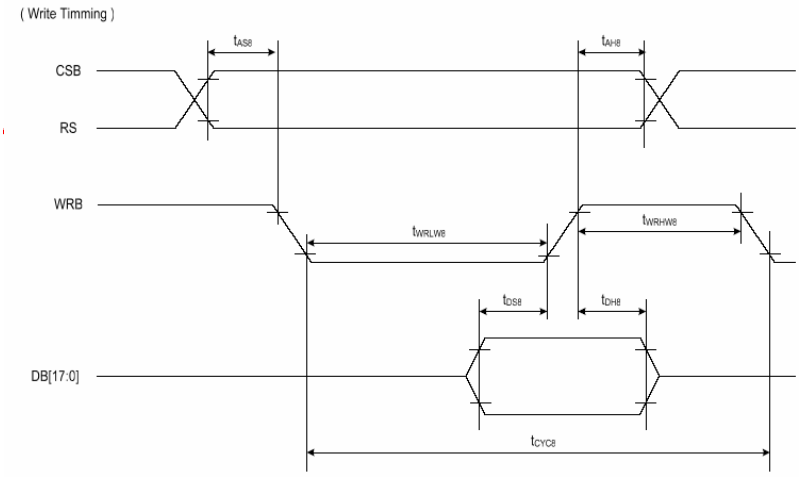


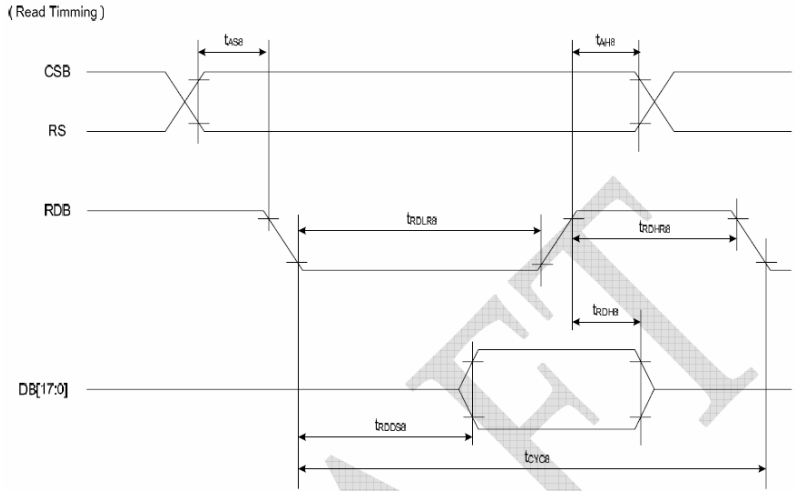
3.2.2 80XX-Series MPU Parallel Interface Timing Characteristics:

(VDD = 2.8V, Ta = 25℃)

Item	Symbol	Condition	Min	Max	Unit	Port
Write Timing						
Address hold timing Address setup timing	t_{AH8} t_{AS8}	-	5 5	-	ns	CSB RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}	-	100 45 45	-	ns	WRB
Data setup timing Data hold Timing	t_{DS8} t_{DH8}		30 10	-	ns	DB[17:0]
Read Timing						
Address hold timing Address setup timing	t_{AH8} t_{AS8}	-	10 10	-	ns	CSB RS
System cycle timing Read "L" pulse width Read "H" pulse width	t_{CYC8} t_{RDLR8} t_{RDHR8}	-	200 90 90	-	ns	RDB
Read data output delay time Data hold Timing	t_{RDD8} t_{RDH8}	C_L = 15pF	- 0	60	ns	DB[17:0]

*) All the timing reference is 10% and 90% of VDD.



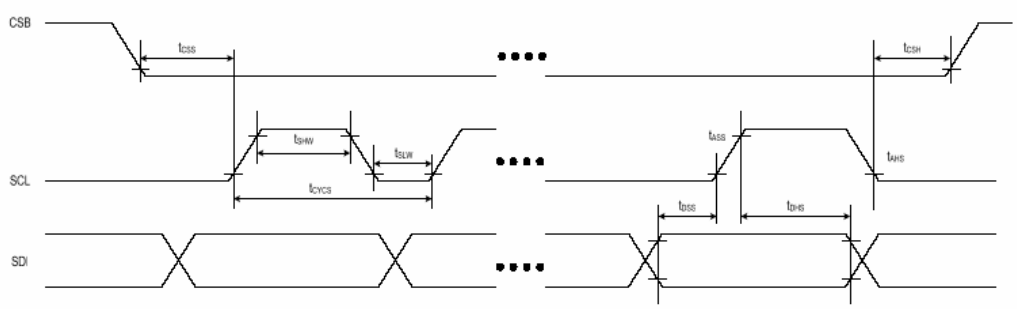


3.2.3 Serial Interface Timing Characteristics:

(VDD = 2.8V, Ta = 25℃)

Item	Symbol	Condition	Min	Max	Unit	Port
Serial clock cycle	t_{CYCS}	-	60	-	ns	SCL
SCL "H" pulse width	t_{SHW}		25			
SCL "L" pulse width	t_{SLW}		25			
Data setup timing	t_{DSS}	-	25	-	ns	SDI
Data hold Timing	t_{DHS}		25			
CSB-SCL timing	t_{CSS}		25	-	ns	CSB
CSB-hold timing	t_{CSH}		25			

*) All the timing reference is 10% and 90% of VDD.



3.3 Optics & Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (White)	L_{br}	Note 3	70	100	-	cd/m^2
C.I.E. (White)	(x) (y)	Note 3	0.22 0.24	0.26 0.28	0.30 0.32	
C.I.E. (Red)	(x) (y)	Note 3	0.61 0.30	0.65 0.34	0.69 0.38	
C.I.E. (Green)	(x) (y)	Note 3	0.26 0.58	0.30 0.62	0.34 0.66	
C.I.E. (Blue)	(x) (y)	Note 3	0.10 0.15	0.14 0.19	0.18 0.23	
Dark Room Contrast	CR		-	>1000:1	-	
View Angle			>160	-	-	degree

Note3: Optical measurement with polarizer is taken @ VDD, VDDIO = 2.8V, VDDH = 14V, and the software initial setting with section 4.4.2 Reference Parameter Table for Normal Operation Mode.

3.4 General Electrical Specification

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VDD		2.4	2.8	3.3	V
Supply Voltage for I/O Pins	VDDIO		1.6	2.8	3.3	V
Driver Supply Voltage	VDDH		13.5	14.0	14.5	V
Operating Current for VDD	I_{VDD}	Note 4	-	2.5	3.5	mA
		Note 5	-	2.5	3.5	mA
Operating Current for VDDH	I_{VDDH}	Note 4	-	25	31	mA
		Note 5	-	8	10	mA
Sleep Mode Current for VDD	$I_{VDD, SLEEP}$		-	1	5	μA
Sleep Mode Current for VDDH	$I_{VDDH, SLEEP}$		-	1	5	μA

Note 4: VDD & VDDIO = 2.8V, VDDH = 14V, L_{br} @ $100cd/m^2$, full white with polarizer, software initial setting follow section 4.4.2 Reference Parameter Table for Normal Operation Mode.

Note 5: VDD & VDDIO = 2.8V, VDDH = 14V, L_{br} @ $30cd/m^2$, full white with polarizer, software initial setting follow section 4.4.2 Reference Parameter Table for Power Saving Mode.

4. *Functional Specification*

4.1. Commands

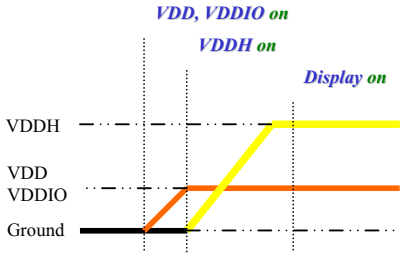
Refer to the Technical Manual for the SEPS525

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

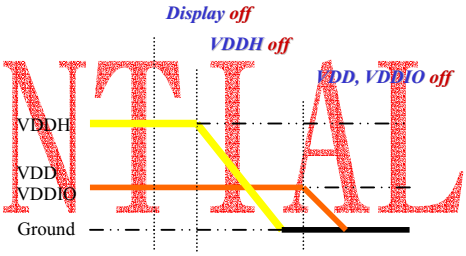
4.2.1 Power up Sequence:

1. Power up VDD, VDDIO
2. Send Display off command
3. Clear Screen
4. Power up VDDH
5. Delay 100ms
   (when VDD is stable)
6. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down VDDH
3. Delay 100ms
   (when VDDH is reach 0 and panel is completely discharges)
4. Power down VDD, VDDIO



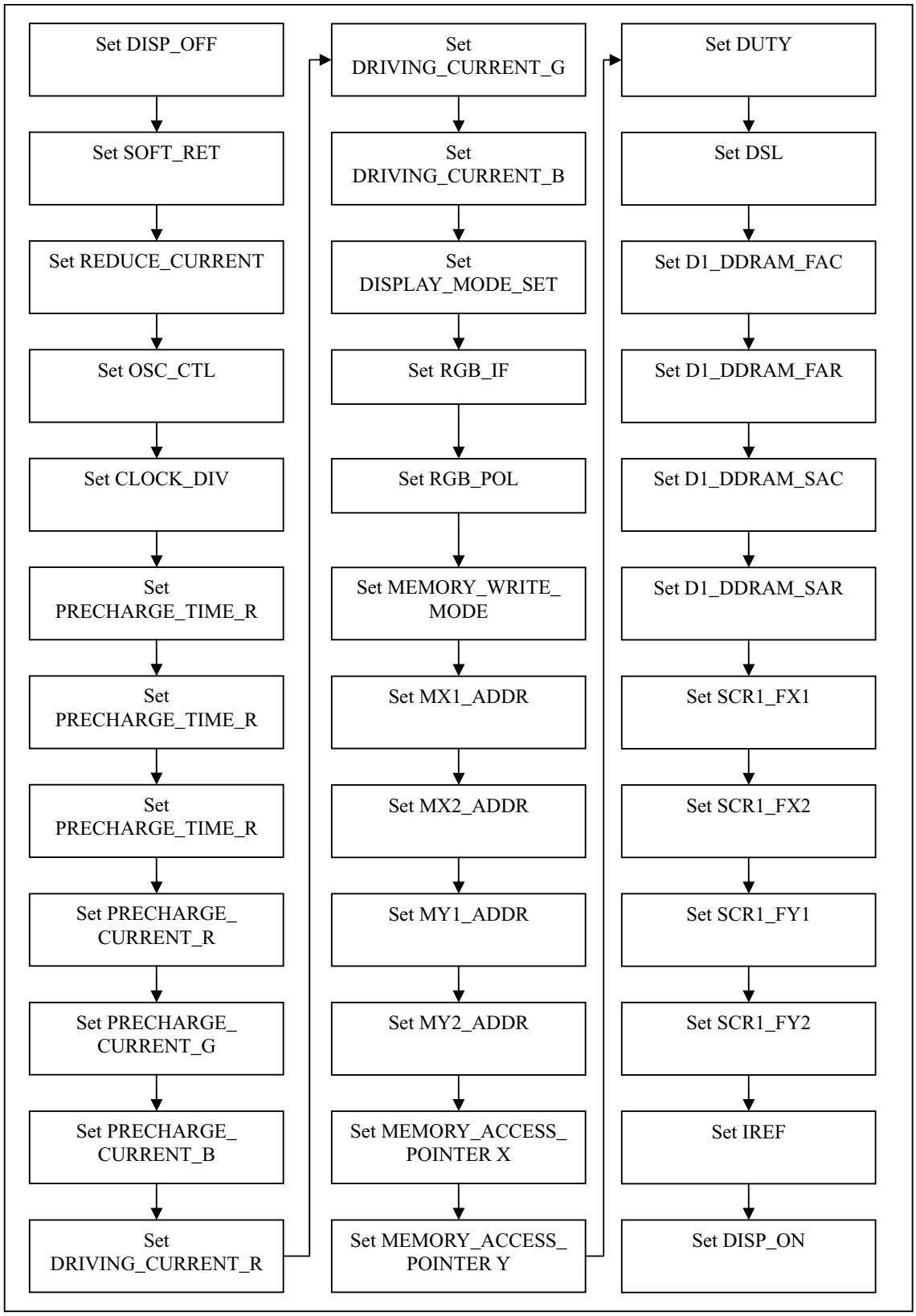
4.3 Reset Circuit

When RESETB input is low, the chip is initialized with the following status:

1. Frame frequency: 90Hz
2. OSC: internal OSC
3. Internal OSC: ON
4. DDRAM write horizontal address: MX1 = 00h, MX2 = 9Fh
5. DDRAM write vertical address: MY1 = 00h, MY2 = 7Fh
6. Display data RAM write: HC = 1, VC = 1, HV = 0
7. RGB data swap: OFF
8. Row scan shift direction: G0, G1, … , G126, G127
9. Column data shift direction: S0, S1, … , S478, S479
10. Display ON/OFF: OFF
11. Panel display size: FX1 = 00h, FX2 = 9Fh, FY1 = 00h, FY2 = 7Fh
12. Display data RAM read column/row address: FAC = 00h, FAR = 00h
13. Precharge time(R/G/B): 0 clock
14. Precharge current(R/G/B): 0 uA
15. Driving current(R/G/B): 0 uA

4.4 Actual Application Example

4.4.1 Driver IC Initial Setting Flowchart



4.4.2 Reference Parameters Table

(VDD = 2.8V, Ta = 25℃)

Command Parameter	Normal Operation Mode	Power Saving Mode
Set Display On_OFF	0x06 , 0x00	
Set SOFT_RST	0x05 , 0x00	
Set REDUCE_CURRENT	0x04 , 0x01 wait 1ms 0x04,0x00	
Set OSC_CTL	0x02 , 0x01	
Set CLOCK_DIV	0x03 , 0x09	
Set PRECHARGE_TIME_R	0x08 , 0x03	0x08 , 0x00
Set PRECHARGE_TIME_G	0x09 , 0x05	0x09 , 0x00
Set PRECHARGE_TIME_B	0x0A , 0x05	0x0A , 0x00
Set PRECHARGE_CURRENT_R	0x0B , 0x56	0x0B , 0x00
Set PRECHARGE_CURRENT_G	0x0C , 0x4D	0x0C , 0x00
Set PRECHARGE_CURRENT_B	0x0D , 0x46	0x0D , 0x00
Set DRIVING_CURRENT_R	0x10 , 0x0A	0x10 , 0x0D
Set DRIVING_CURRENT_G	0x11 , 0x0A	0x11 , 0x0C
Set DRIVING_CURRENT_B	0x12 , 0x0A	0x12 , 0x0B
Set DISPLAY_MODE_SET	0x13 , 0x00	
Set RGB_IF	0x14 , 0x01	
Set RGB_POL	0x15 , 0x00	
Set MEMORY_WRITE_MODE	0x16 , 0x76	
Set MX1_ADDR	0x17 , 0x00	
Set MX2_ADDR	0x18 , 0x9F	
Set MY1_ADDR	0x19 , 0x00	
Set MY2_ADDR	0x1A , 0x7F	
Set MEMORY_ACCESS_POINTER X	0x20 , 0x00	
Set MEMORY_ACCESS_POINTER Y	0x21 ,0x00	
Set DUTY	0x28 , 0x7F	
Set DSL	0x29 , 0x00	
Set D1_DDRAM_FAC	0x2E , 0x00	
Set D1_DDRAM_FAR	0x2F , 0x00	
Set D1_DDRAM_SAC	0x31 , 0x00	
Set D1_DDRAM_SAR	0x32 , 0x00	
Set SCR1_FX1	0x33 , 0x00	
Set SCR1_FX2	0x34 , 0x9F	
Set SCR1_FY1	0x35 , 0x00	
Set SCR1_FY2	0x36 , 0x7F	
Set IREF	0x80 , 0x00	
Set DISP_ON_OFF	0x06 , 0x01	

5. *Reliability*

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-30°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 1 hr dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	10,000	-	Hrs	70 cd/m^2, 50%checkerboard	6
Storage Life Time	20,000	-	Hrs	Ta=25°C, 50%RH	-

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. *Outgoing Quality Control Specifications*

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15 %RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50 cm
Distance between the Panel & Eyes of the Inspector:	≥ 30 cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

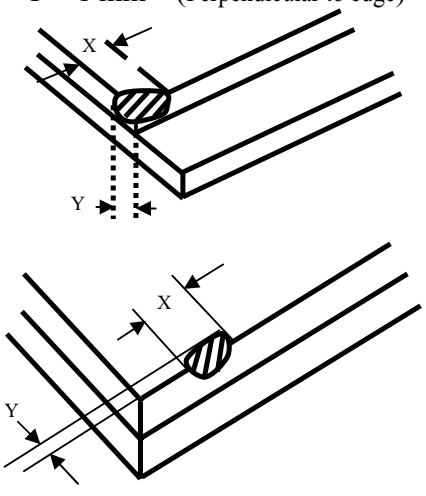
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

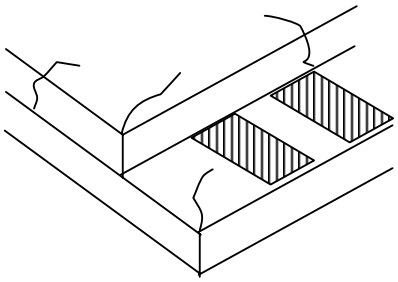
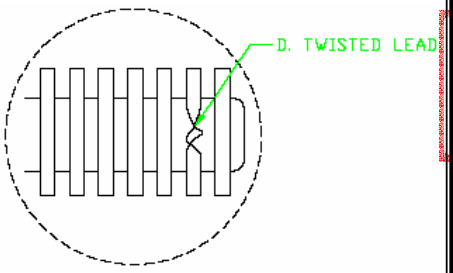
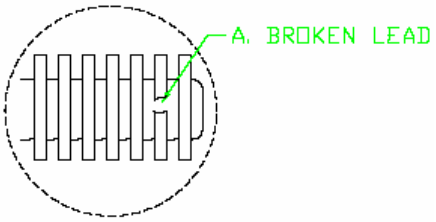
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

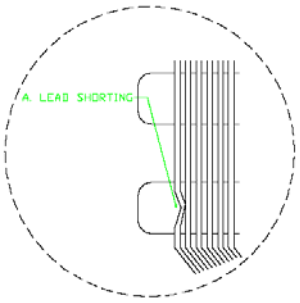
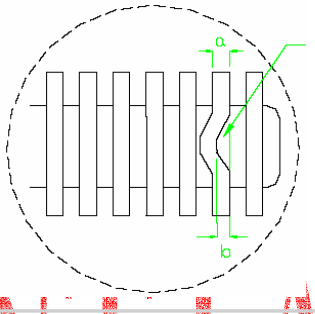
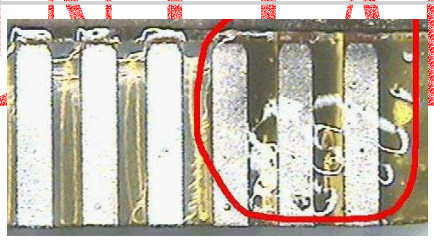
6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

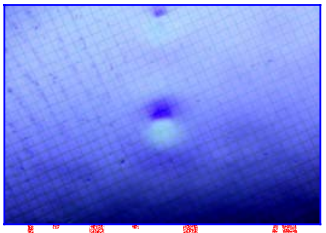
Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Twist	Minor	Not Allowable 
Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Probe Mark	Acceptable	Ok

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Terminal Lead Bent (Not Twist or Broken)	Minor	NG if any bent lead cause lead shorting. 
	Minor	NG for horizontally bent lead more than 50% of its width. 
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

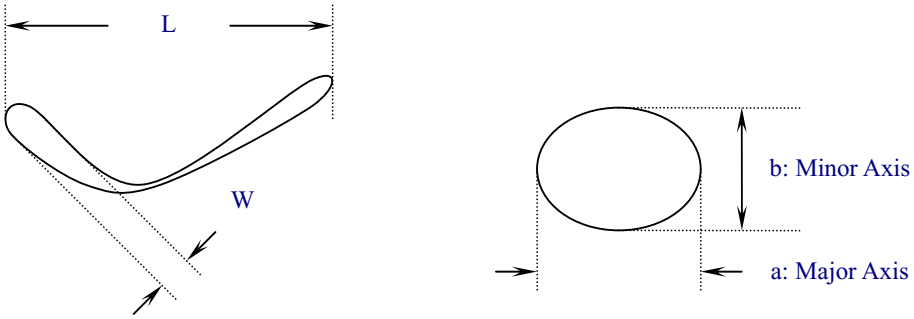
6.3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

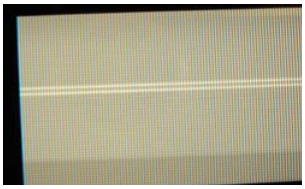
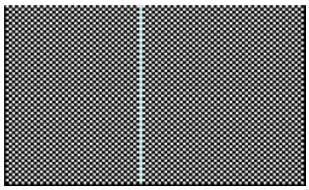
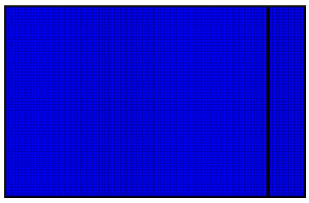
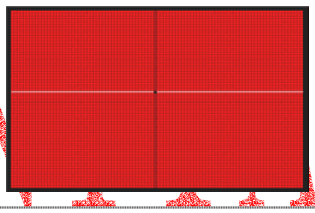
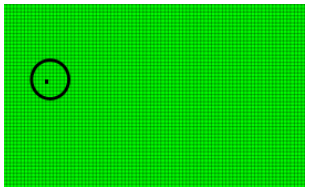
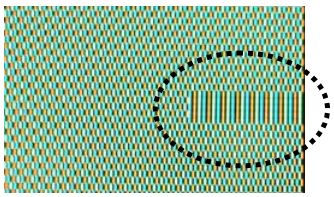
Check Item	Classification	Criteria
Any Dirt & Scratch on Protective Film	Acceptable	Ignore for Any
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore
		W ≤ 0.1 Ignore W > 0.1, L ≤ 1 n ≤ 1 L > 1 n = 0
Dirt, Spot-Shape Defect (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 <Φ ≤ 0.2 n ≤ 1 0.2 <Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not allowable

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	Not allowable
Bright Line	Major	
Missed Line	Major	 
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-Uniform (Luminance Variation within a Display)	Major