

<b>SANYO</b>	No. 5082A	<b>LC321664BJ, BM, BT-70/80</b>
		<b>1 MEG (65536 words × 16 bits) DRAM</b> <b>Fast Page Mode, Byte Write</b>

## Overview

The LC321664BJ, BM, BT is a CMOS dynamic RAM operating on a single 5 V power source and having a 65536 words × 16 bits configuration. Equipped with large capacity capabilities, high speed transfer rates and low power dissipation, this series is suited for a wide variety of applications ranging from computer main memory and expansion memory to commercial equipment.

Address input utilizes a multiplexed address bus which permits it to be enclosed in a compact plastic package of 40-pin SOJ. Refresh rates are within 4 ms with 256 row address (A0 to A7) selection and support Row Address Strobe ( $\overline{\text{RAS}}$ )-only refresh, Column Address Strobe ( $\overline{\text{CAS}}$ )-before- $\overline{\text{RAS}}$  refresh and hidden refresh settings. There are functions such as fast page mode, read-modify-write and byte write.

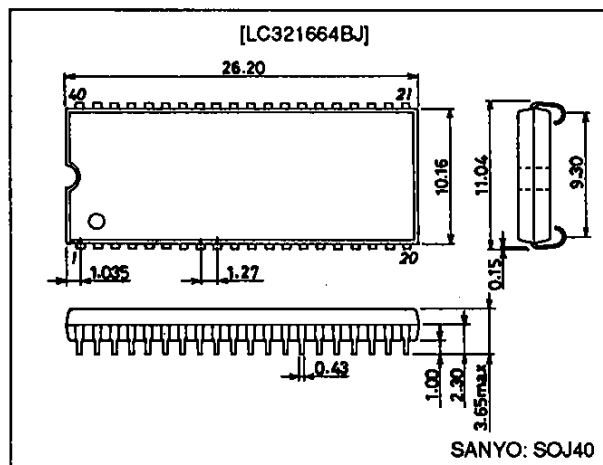
## Features

- 65536 words × 16 bits configuration.
- Single 5 V ± 10% power supply.
- All input and output (I/O) TTL compatible.
- Supports fast page mode, read-modify-write and byte write.
- Supports output buffer control using early write and Output Enable ( $\overline{\text{OE}}$ ) control.
- 4 ms refresh using 256 refresh cycles.
- Supports  $\overline{\text{RAS}}$ -only refresh,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh and hidden refresh.
- Packages
  - SOJ 40-pin (400 mil) plastic package : LC321664BJ
  - SOP 40-pin (525 mil) plastic package : LC321664BM
  - TSOP 44-pin (400 mil) plastic package : LC321664BT
- $\overline{\text{RAS}}$  access time/column address access time/ $\overline{\text{CAS}}$  access time/cycle time/power dissipation

## Package Dimensions

unit: mm

3200-SOJ40



Parameter	LC321664BJ, BM, BT	
	-70	-80
$\overline{\text{RAS}}$ access time	70 ns	80 ns
Column address access time	40 ns	45 ns
$\overline{\text{CAS}}$ access time	25 ns	25 ns
Cycle time	125 ns	135 ns
Power dissipation (max)	During operation	688 mW
	During standby	5.5 mW (CMOS level)/11 mW (TTL level)

**SANYO Electric Co., Ltd. Semiconductor Business Headquarters**  
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

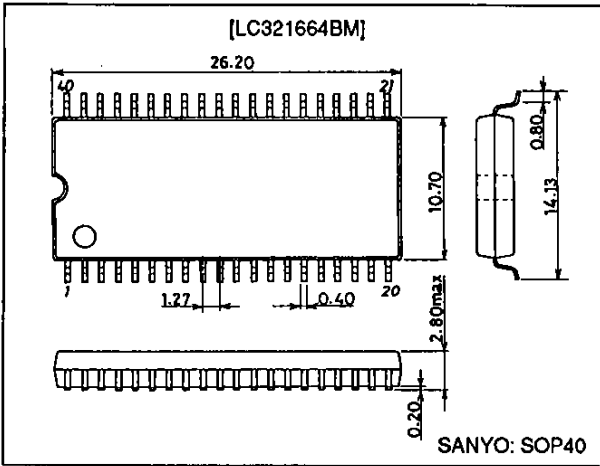
32896HA (OT)/33195TH (OT) No. 5082-1/28

# LC321664BJ, BM, BT-70/80

## Package Dimensions

unit: mm

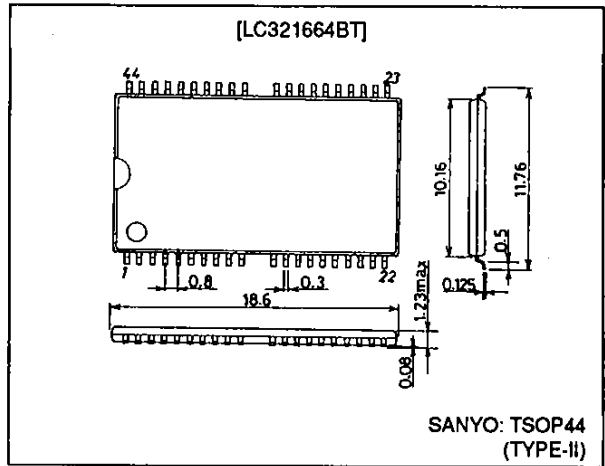
### 3195-SOP40



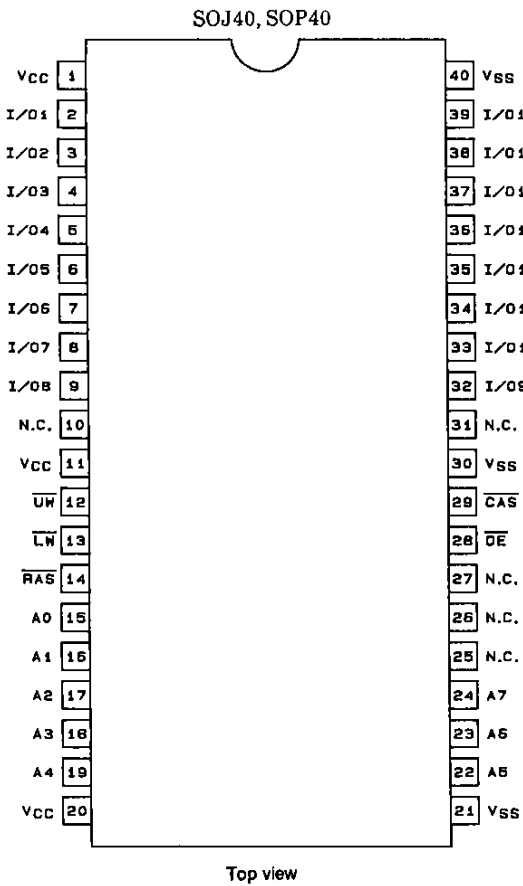
## Package Dimensions

unit: mm

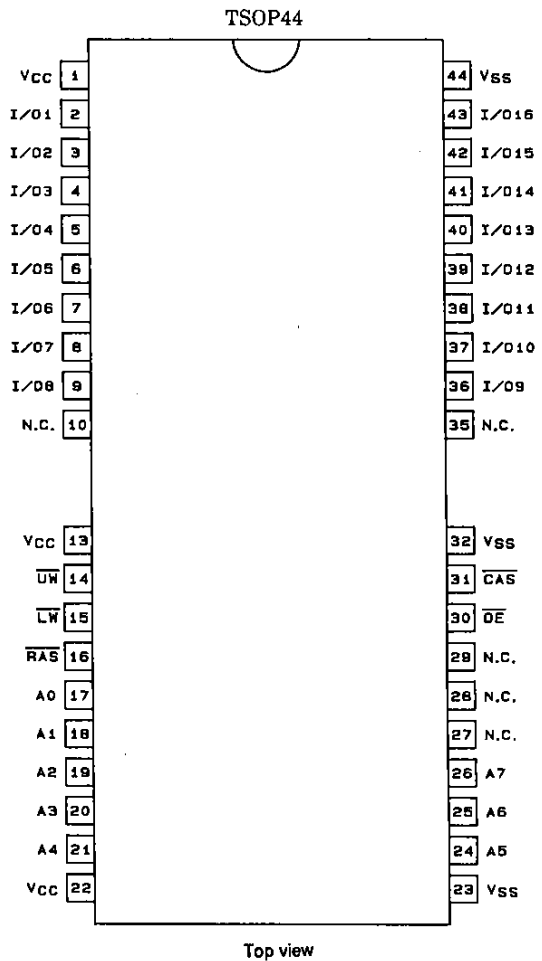
### 3207-TSOP44



## Pin Assignments

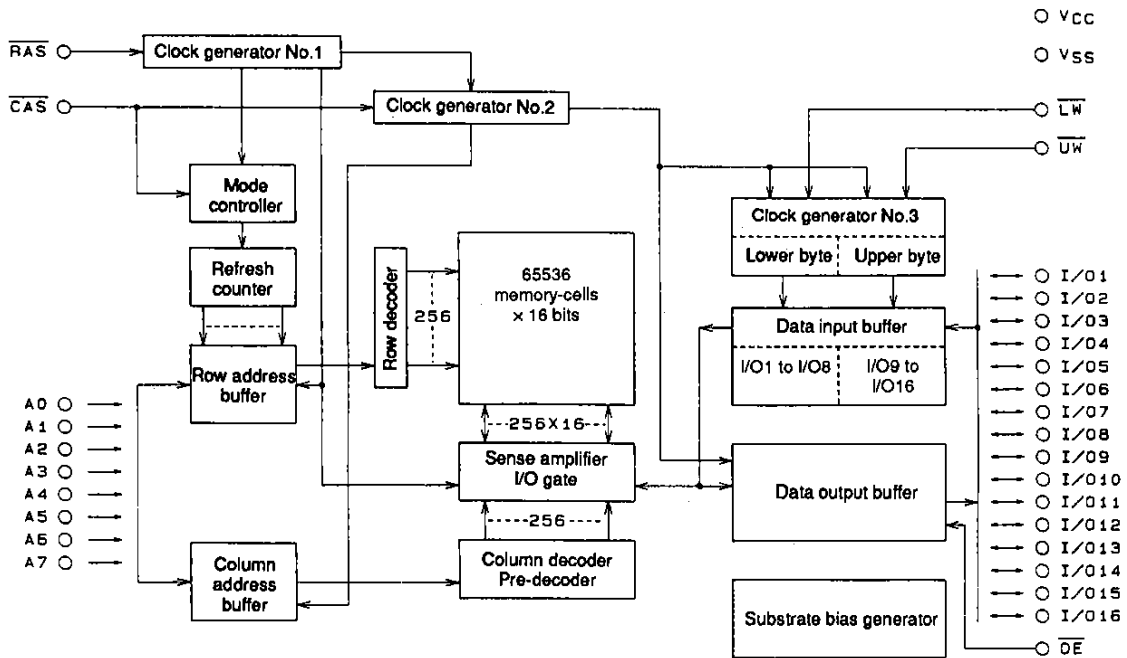


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Block Diagram



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Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	V <sub>CC</sub> max	-1.0 to +7.0	V	1
Input voltage	V <sub>IN</sub>	-1.0 to +7.0	V	1
Output voltage	V <sub>OUT</sub>	-1.0 to +7.0	V	1
Allowable power dissipation	Pd max	800	mW	1
		700		
Output short-circuit current	I <sub>OUT</sub>	50	mA	1
Operating temperature range	T <sub>opr</sub>	0 to +70	°C	1
Storage temperature range	T <sub>stg</sub>	-55 to +150	°C	1

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Power supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	2
Input high level voltage	V <sub>IH</sub>	2.4		6.5	V	2
Input low level voltage (A0 to A7, RAS, CAS, UW, LW, OE)	V <sub>IL</sub>	-1.0*		+0.8	V	2
Input low level voltage (I/O1 to I/O16)	V <sub>IL</sub>	-0.5*		+0.8	V	2

Note: 2. All voltages are referenced to V<sub>SS</sub>.  
 A bypass capacitor of about 0.1 μF should be connected between V<sub>CC</sub> and V<sub>SS</sub> of the device.  
 \*: -2.0 V when pulse width is less than 20 ns.

LC321664BJ, BM, BT-70/80

DC Electrical Characteristics at Ta = 0 to +70°C, VCC = 5 V ± 10%

Parameter	Symbol	Conditions	LC321664BJ, BM, BT				Unit	Note
			-70		-80			
			min	max	min	max		
Operating current (Average current during operation)	I <sub>CC1</sub>	$\overline{RAS}, \overline{CAS}$ , address cycling: t <sub>RC</sub> = t <sub>RC</sub> min		125		115	mA	3, 4, 5
Standby current	I <sub>CC2</sub>	$\overline{RAS} = \overline{CAS} = V_{IH}$		2		2	mA	
$\overline{RAS}$ -only refresh current	I <sub>CC3</sub>	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ ; t <sub>RC</sub> = t <sub>RC</sub> min		125		115	mA	3, 5
Fast page mode current	I <sub>CC4</sub>	$\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , address cycling: t <sub>PC</sub> = t <sub>PC</sub> min		80		70	mA	3, 4, 5
Standby current	I <sub>CC5</sub>	$\overline{RAS} = \overline{CAS} = V_{CC} - 0.2 V$		1		1	mA	
$\overline{CAS}$ -before- $\overline{RAS}$ refresh current	I <sub>CC6</sub>	$\overline{RAS}$ , $\overline{CAS}$ cycling: t <sub>RC</sub> = t <sub>RC</sub> min		125		115	mA	3
Input leakage current	I <sub>IL</sub>	0 V ≤ V <sub>IN</sub> ≤ 6.5 V, pins other than test pin = 0 V	-10	+10	-10	+10	μA	
Output leakage current	I <sub>OL</sub>	D <sub>OUT</sub> disable, 0 V ≤ V <sub>OUT</sub> ≤ 5.5 V	-10	+10	-10	+10	μA	
Output high level voltage	V <sub>OH</sub>	I <sub>OUT</sub> = -2.5 mA	2.4		2.4		V	
Output low level voltage	V <sub>OL</sub>	I <sub>OUT</sub> = 2.1 mA		0.4		0.4	V	

Note: 3. All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller.

4. I<sub>CC1</sub> and I<sub>CC4</sub> are dependent on output loads. Maximum values for I<sub>CC1</sub> and I<sub>CC4</sub> represent values with output open.

5. Address change is less than or equal to one time during  $\overline{RAS} = V_{IL}$ . Concerning I<sub>CC4</sub>, it is less than or equal to one time during 1 cycle (t<sub>PC</sub>).

AC Electrical Characteristics at Ta = 0 to +70°C, VCC = 5 V ± 10% (Notes 6, 7 and 8)

Parameter	Symbol	LC321664BJ, BM, BT				Unit	Note
		-70		-80			
		min	max	min	max		
Random read, write cycle time	t <sub>RC</sub>	125		135		ns	
Read-write/read-modify-write cycle time	t <sub>RWC</sub>	170		180		ns	
Fast page mode cycle time	t <sub>PC</sub>	50		55		ns	
Fast page mode read-write/read-modify-write cycle time	t <sub>PRWC</sub>	95		100		ns	
$\overline{RAS}$ access time	t <sub>RAC</sub>		70		80	ns	9, 14, 15
$\overline{CAS}$ access time	t <sub>CAC</sub>		25		25	ns	9, 14
Column address access time	t <sub>AA</sub>		40		45	ns	9, 15
$\overline{CAS}$ precharge access time	t <sub>CPA</sub>		45		50	ns	9
Output low-impedance time from $\overline{CAS}$ low	t <sub>CLZ</sub>	0		0		ns	9
Output buffer turn-off delay time	t <sub>OFF</sub>	0	20	0	20	ns	10
Rise, fall time	t <sub>T</sub>	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t <sub>RP</sub>	45		45		ns	
$\overline{RAS}$ pulse width	t <sub>RAS</sub>	70	10000	80	10000	ns	
$\overline{RAS}$ pulse width for fast page mode only	t <sub>RASP</sub>	70	100000	80	100000	ns	
$\overline{RAS}$ hold time	t <sub>RSH</sub>	25		25		ns	
$\overline{CAS}$ hold time	t <sub>CSH</sub>	70		80		ns	
$\overline{CAS}$ pulse width	t <sub>CAS</sub>	25	10000	25	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t <sub>RCD</sub>	20	45	20	55	ns	14
$\overline{RAS}$ to column address delay time	t <sub>RAD</sub>	15	30	15	35	ns	15
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t <sub>CRP</sub>	10		10		ns	
$\overline{CAS}$ precharge time	t <sub>CP</sub>	10		10		ns	
Row address setup time	t <sub>ASR</sub>	0		0		ns	
Row address hold time	t <sub>RAH</sub>	10		10		ns	
Column address setup time	t <sub>ASC</sub>	0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t <sub>AR</sub>	50		55		ns	
Column address to $\overline{RAS}$ lead time	t <sub>RAL</sub>	35		40		ns	
Read command setup time	t <sub>RCS</sub>	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t <sub>RCH</sub>	0		0		ns	11
Read command hold time referenced to $\overline{RAS}$	t <sub>RRH</sub>	0		0		ns	11
Write command hold time	t <sub>WCH</sub>	15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t <sub>WCR</sub>	50		55		ns	

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LC321664BJ, BM, BT-70/80

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Parameter	Symbol	LC321664BJ, BM, BT				Unit	Note
		-70		-80			
		min	max	min	max		
Write command pulse width	$t_{WP}$	15		15		ns	
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	20		20		ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	20		20		ns	
Data input setup time	$t_{DS}$	0		0		ns	12
Data input hold time	$t_{DH}$	15		15		ns	12
Data input hold time referenced to $\overline{RAS}$	$t_{DHR}$	50		55		ns	
Refresh time	$t_{REF}$		4		4	ms	
Write command setup time	$t_{WCS}$	0		0		ns	13
$\overline{CAS}$ to $\overline{UW}$ , $\overline{LW}$ delay time	$t_{CWD}$	45		45		ns	13
$\overline{RAS}$ to $\overline{UW}$ , $\overline{LW}$ delay time	$t_{RWD}$	90		100		ns	13
Column address to $\overline{UW}$ , $\overline{LW}$ delay time	$t_{AWD}$	60		65		ns	13
$\overline{CAS}$ precharge $\overline{UW}$ , $\overline{LW}$ delay time for fast page mode cycle only	$t_{CPWD}$	65		70		ns	13
$\overline{CAS}$ setup time for $\overline{CAS}$ -before- $\overline{RAS}$	$t_{CSR}$	10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ -before- $\overline{RAS}$	$t_{CHR}$	10		10		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ active time	$t_{RPC}$	10		10		ns	
$\overline{CAS}$ precharge time for $\overline{CAS}$ -before- $\overline{RAS}$ counter test	$t_{CPT}$	40		40		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	$t_{ROH}$	15		15		ns	
$\overline{OE}$ access time	$t_{OEA}$		25		25	ns	9
$\overline{OE}$ delay time	$t_{OED}$	15		15		ns	
$\overline{OE}$ output buffer turn-off delay time	$t_{O EZ}$	0	15	0	15	ns	10
$\overline{OE}$ command hold time	$t_{OEH}$	20		20		ns	
Data input to $\overline{CAS}$ delay time	$t_{DZC}$	0		0		ns	16
Data input to $\overline{OE}$ delay time	$t_{DZO}$	0		0		ns	16
Masked write setup time	$t_{MCS}$	0		0		ns	
Masked write hold time referenced to $\overline{RAS}$	$t_{MRH}$	0		0		ns	
Masked write hold time referenced to $\overline{CAS}$	$t_{MCH}$	0		0		ns	

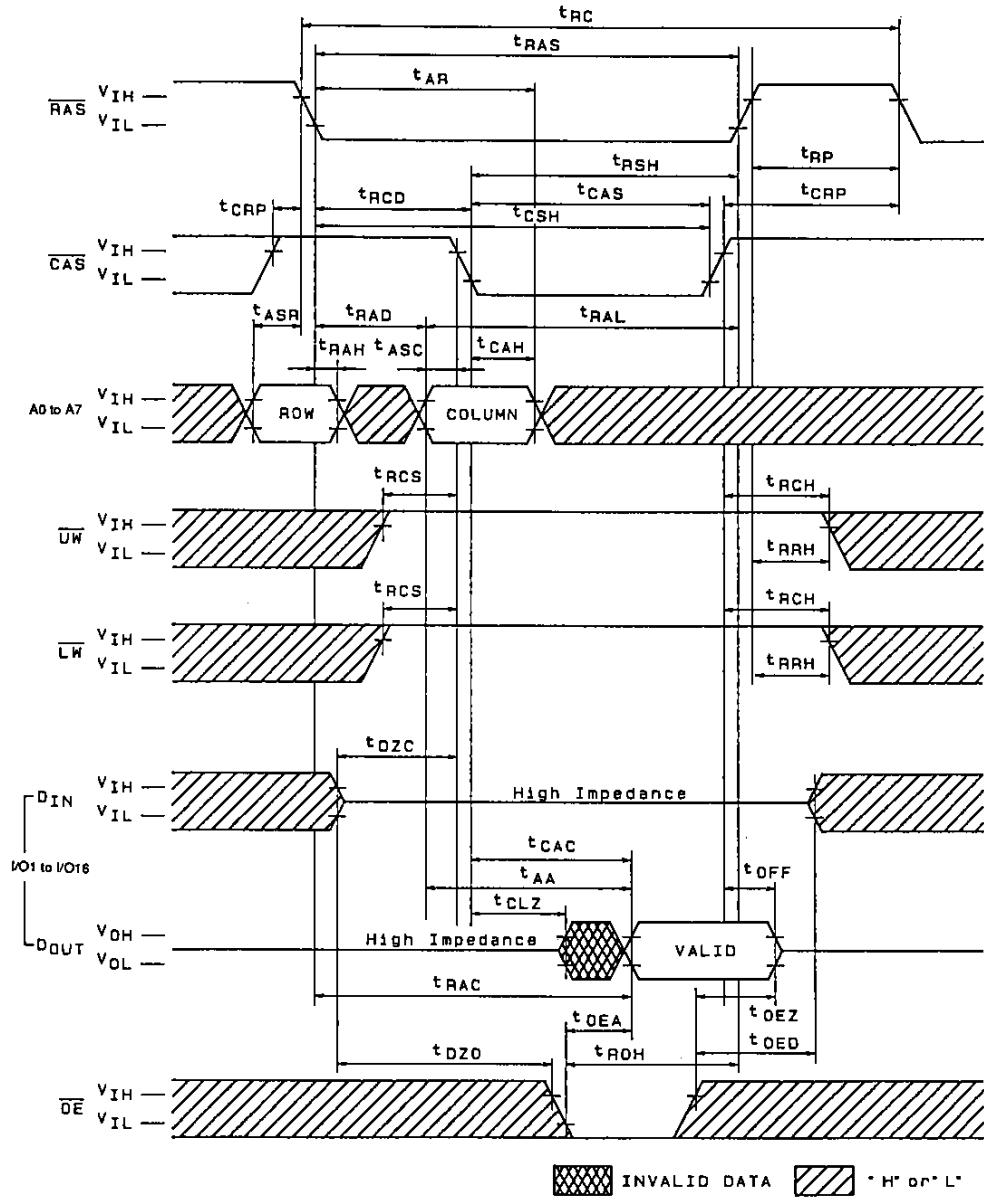
Input/Output Capacitance at  $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	min	max	Unit	Note
Input capacitance ( $A_0$ to $A_7$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{UW}$ , $\overline{LW}$ , $\overline{OE}$ )	$C_{IN}$		7	pF	
Input/Output capacitance ( $I/O_1$ to $I/O_{16}$ )	$C_{IO}$		7	pF	

- Note:
- An initial pause of 200  $\mu\text{s}$  is required after power-up followed by eight  $\overline{RAS}$ -only refresh cycles before proper device operation is achieved. In case of using refresh counter, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycles instead of eight  $\overline{RAS}$ -only refresh cycles are required.
  - Measured at  $t_T = 5\text{ ns}$ .
  - When measuring input signal timing,  $V_{IH}$  (min) and  $V_{IL}$  (max) are used for reference points. In addition, rise and fall time are defined between  $V_{IH}$  and  $V_{IL}$ .
  - Measured using an equivalent of 50 pF and one standard TTL loads.
  - $t_{OFF}$  (max) and  $t_{O EZ}$  (max) are defined as the time until output voltage can no longer be measured when output switches to a high impedance condition.
  - Operation is guaranteed if either  $t_{RRH}$  or  $t_{RCH}$  is satisfied.
  - These parameters are measured from the falling edge of  $\overline{CAS}$  for an early-write cycle, and from the falling edge of  $\overline{UW}$  and  $\overline{LW}$  for a read-write/read-modify-write cycle.
  - $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters for memory in that they specify the operating mode. If  $t_{WCS} \geq t_{WCS}$  (min), the cycle switches to an early-write cycle and output pins switch to high impedance throughout the cycle. If  $t_{CWD} \geq t_{CWD}$  (min),  $t_{RWD} \geq t_{RWD}$  (min),  $t_{AWD} \geq t_{AWD}$  (min) and  $t_{CPWD} \geq t_{CPWD}$  (min) for fast page mode cycle only, the cycle switches to a read-write/read-modify-write cycle and data output equal information in the selected cells. If neither of the above timings are satisfied, output pins are in an undefined state.
  - $t_{RCD}$  (max) is not a restrictive operating parameter but instead represents the point at which the access time  $t_{RAC}$  (max) is guaranteed. If  $t_{RCD} \geq t_{RCD}$  (max), access time is determined according to  $t_{CAC}$ .
  - $t_{RAD}$  (max) is not a restrictive operating parameter but instead represents the point at which the access time  $t_{RAD}$  (max) is guaranteed. If  $t_{RAD} \geq t_{RAD}$  (max), access time is determined according to  $t_{AA}$ .
  - Operation is guaranteed if either  $t_{DZC}$  or  $t_{DZO}$  is satisfied.

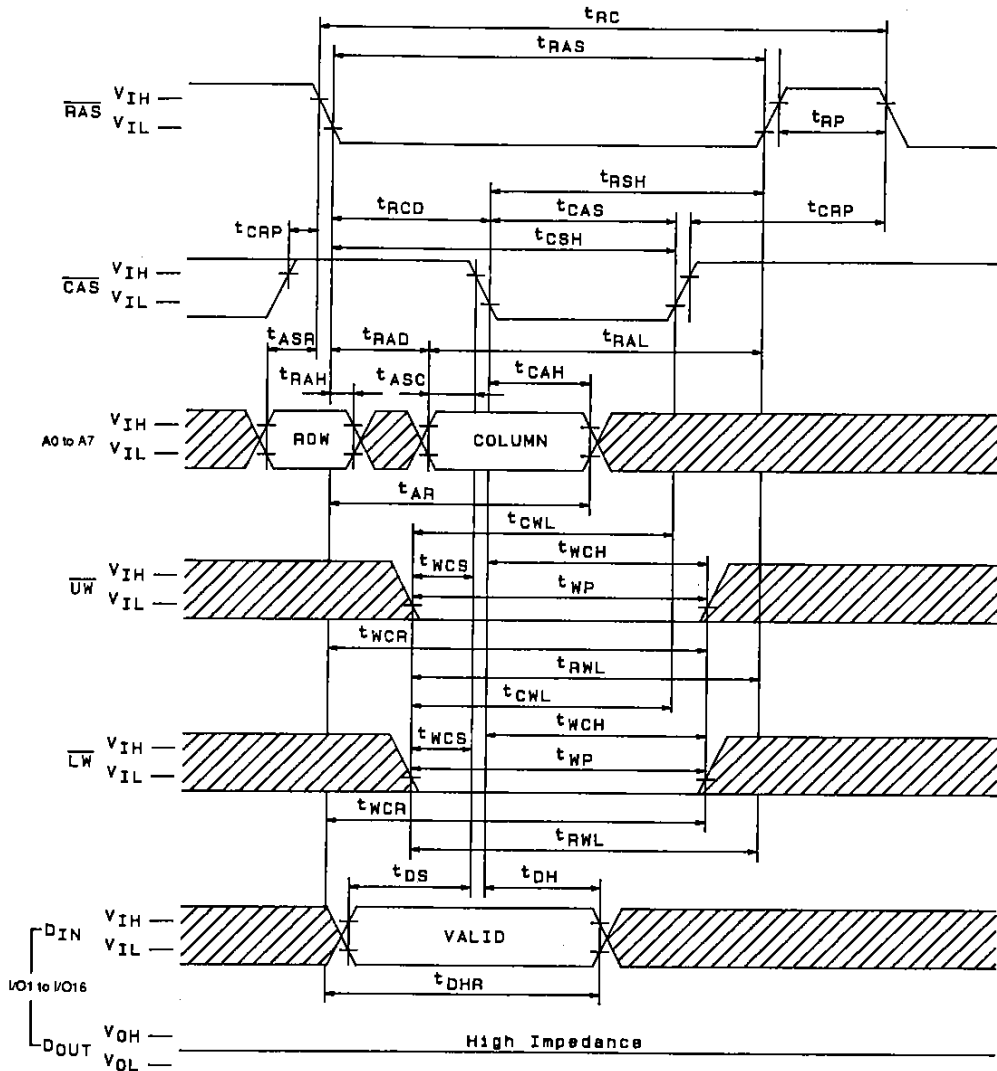
Timing Chart

Read Cycle



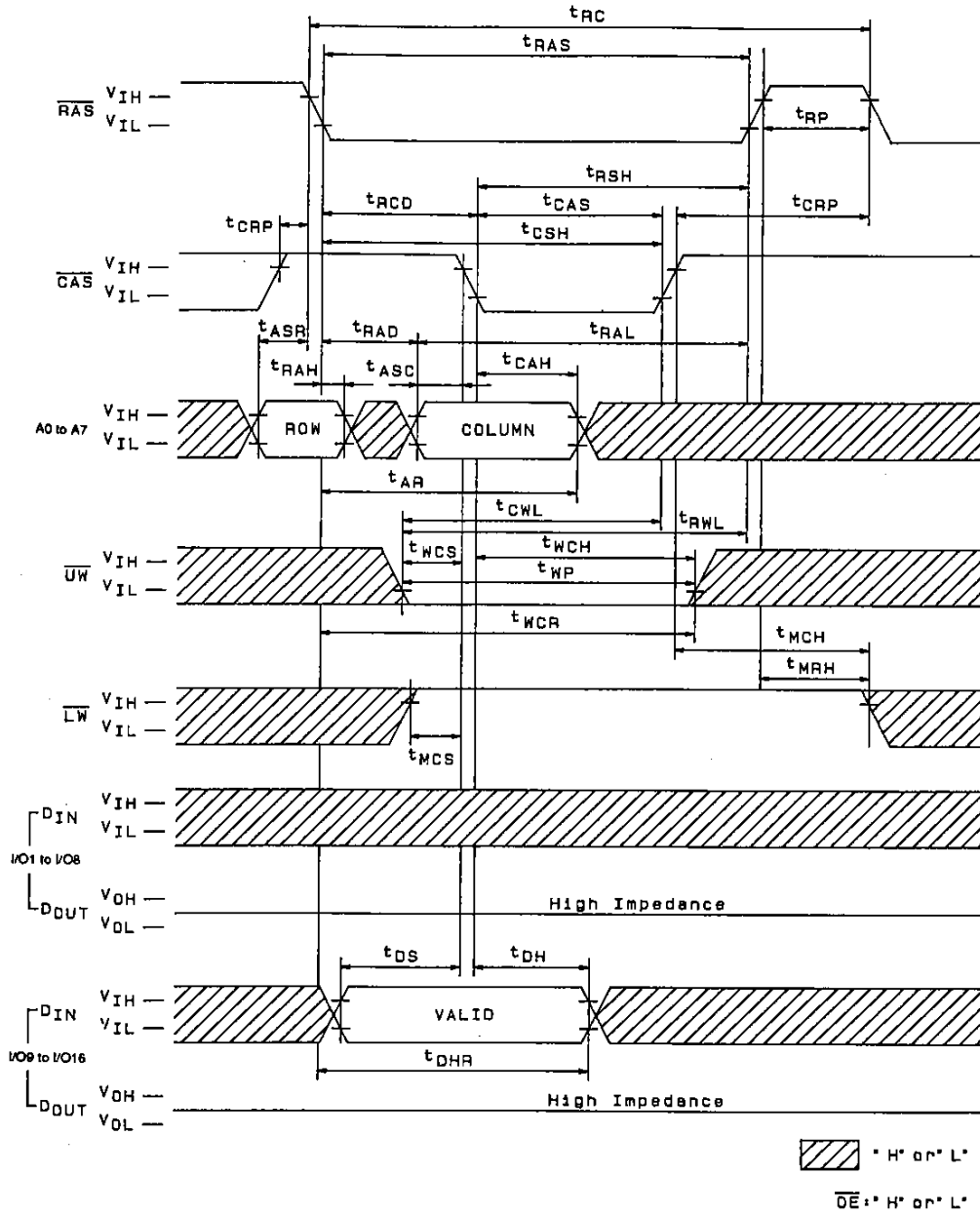
A02139

Early Write Cycle



A02140

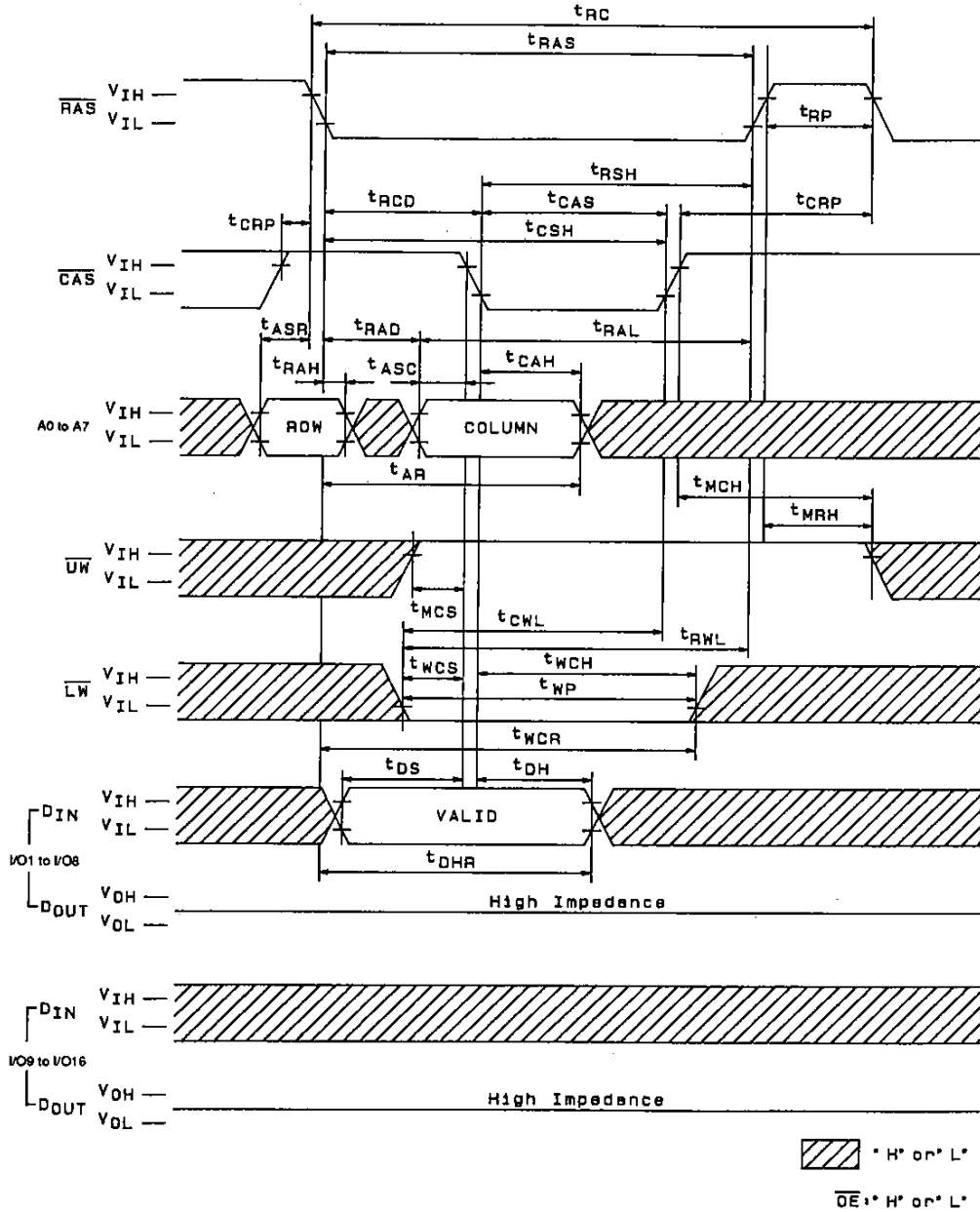
Upper Byte Early Write Cycle



A02141



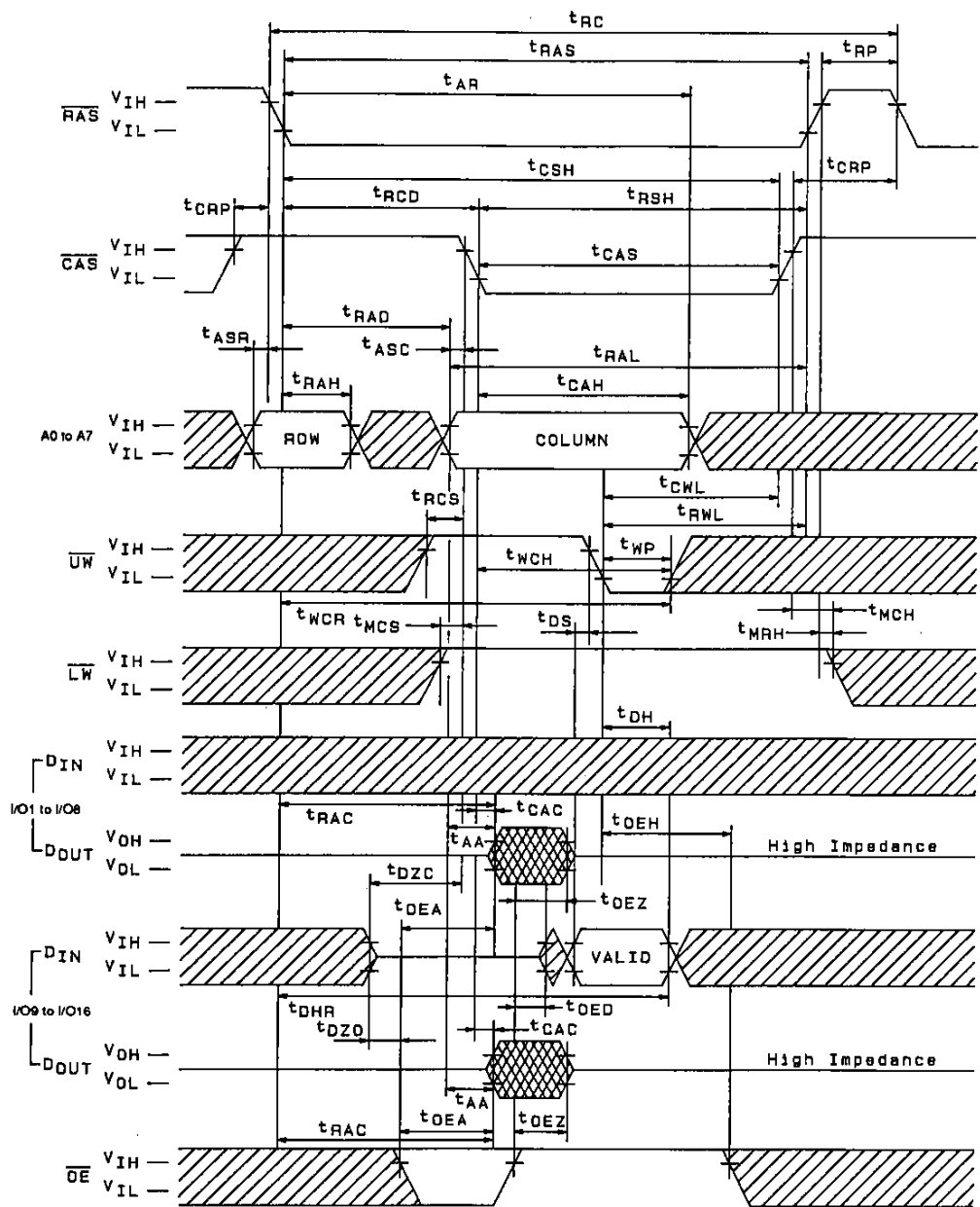
Lower Byte Early Write Cycle



A02142



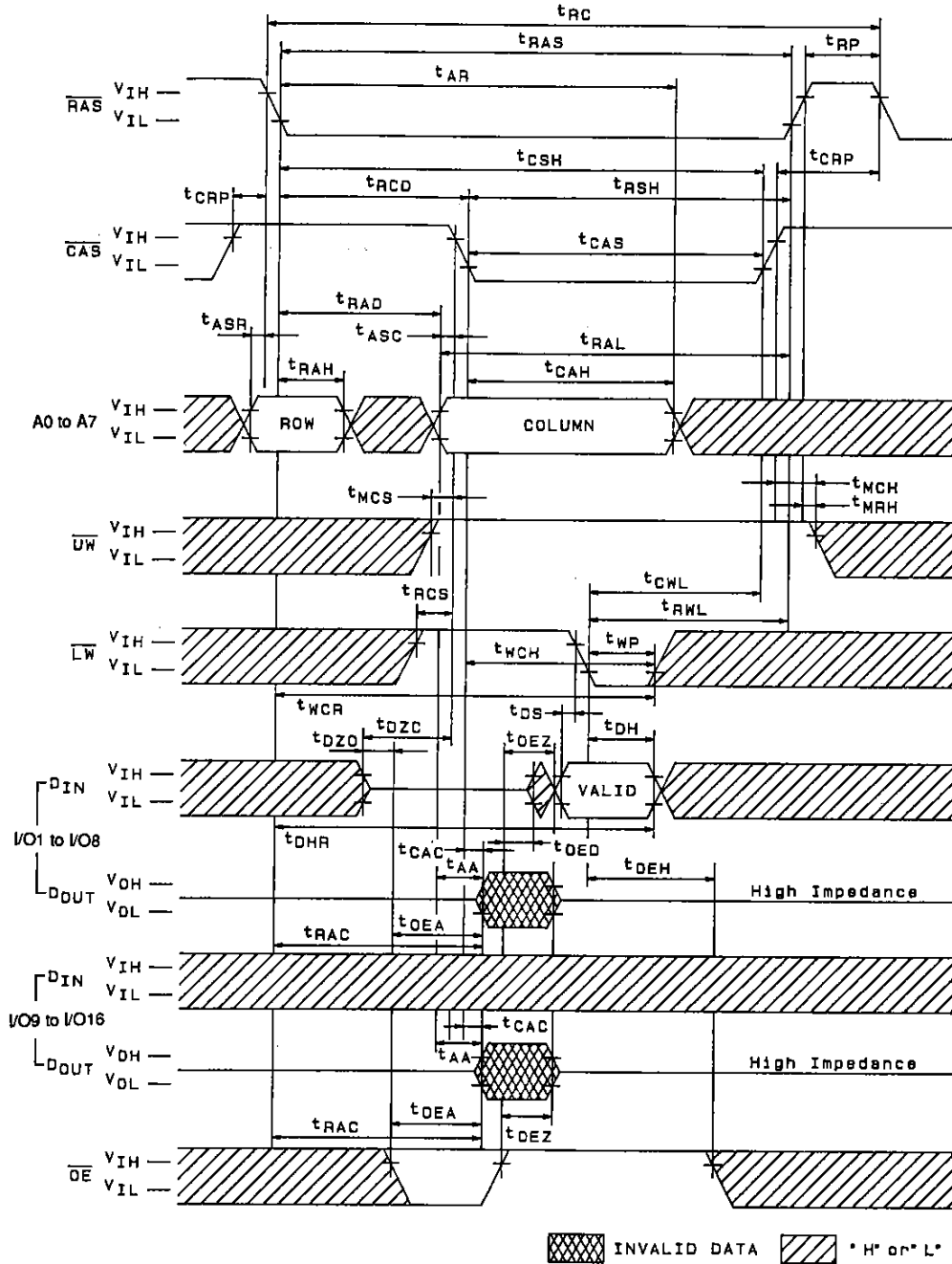
Upper Byte Write Cycle (OE Control)



INVALID DATA    " H " or " L "

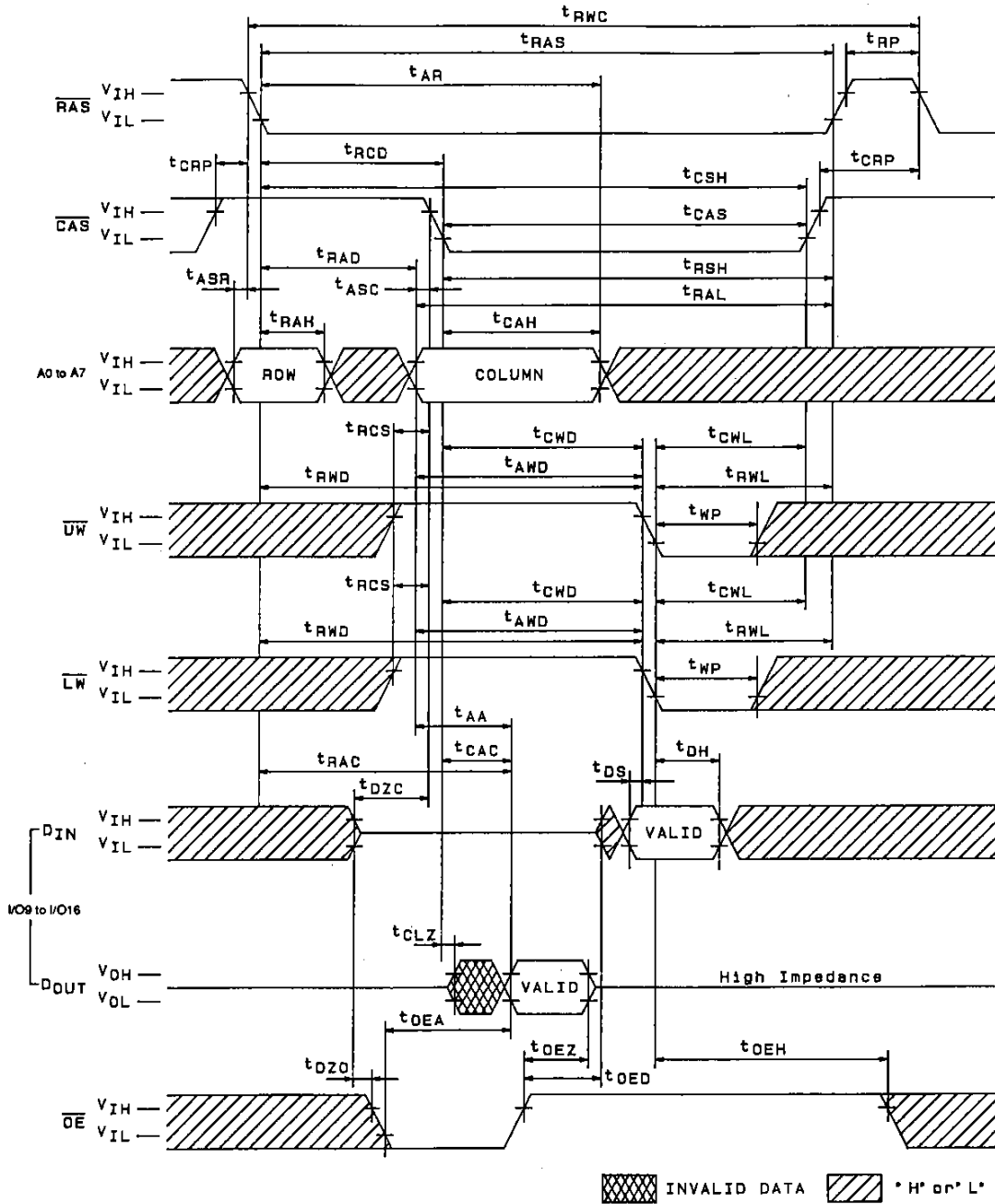
A02144

Lower Byte Write Cycle ( $\overline{OE}$  Control)



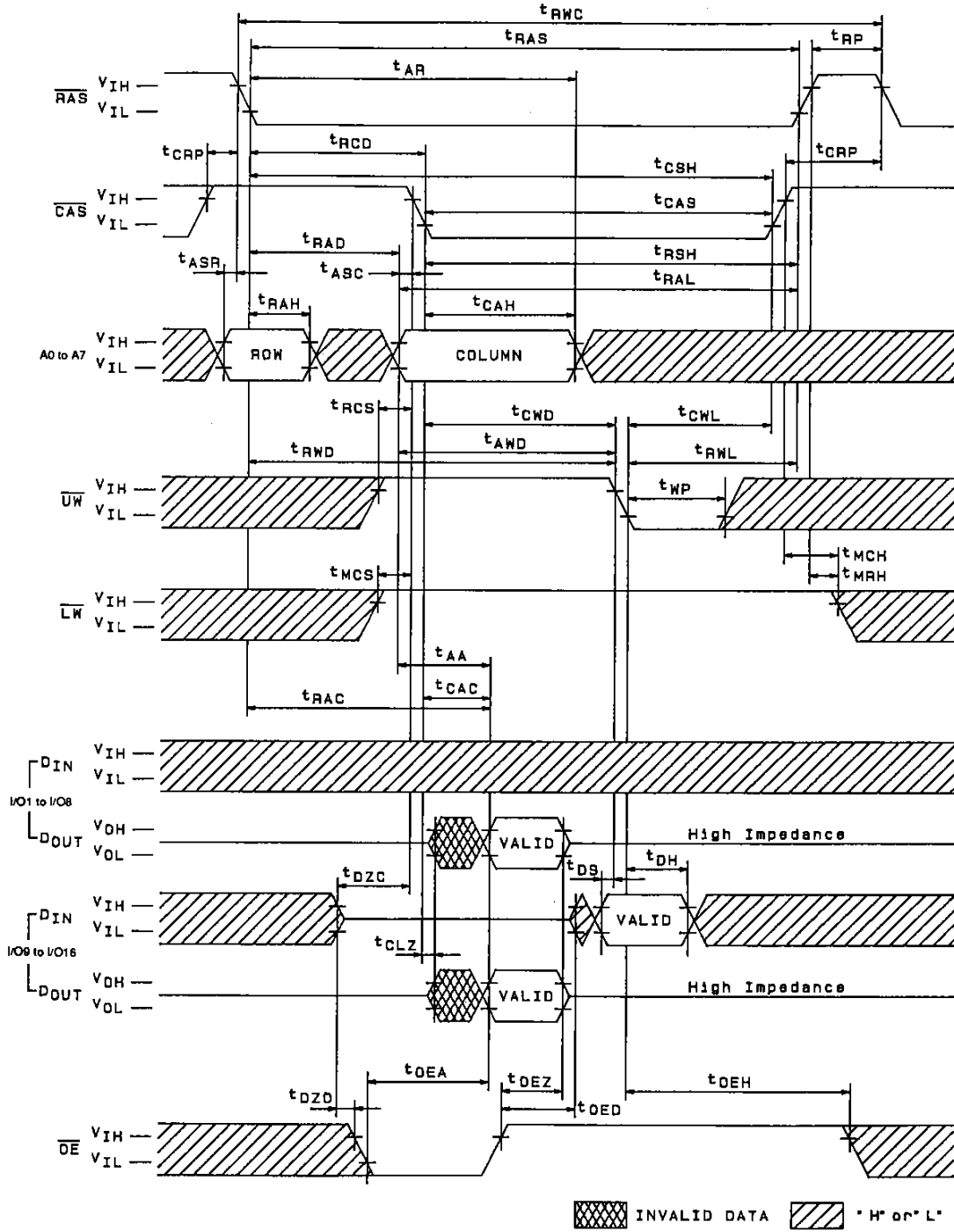
A02145

Read-Modify Write Cycle



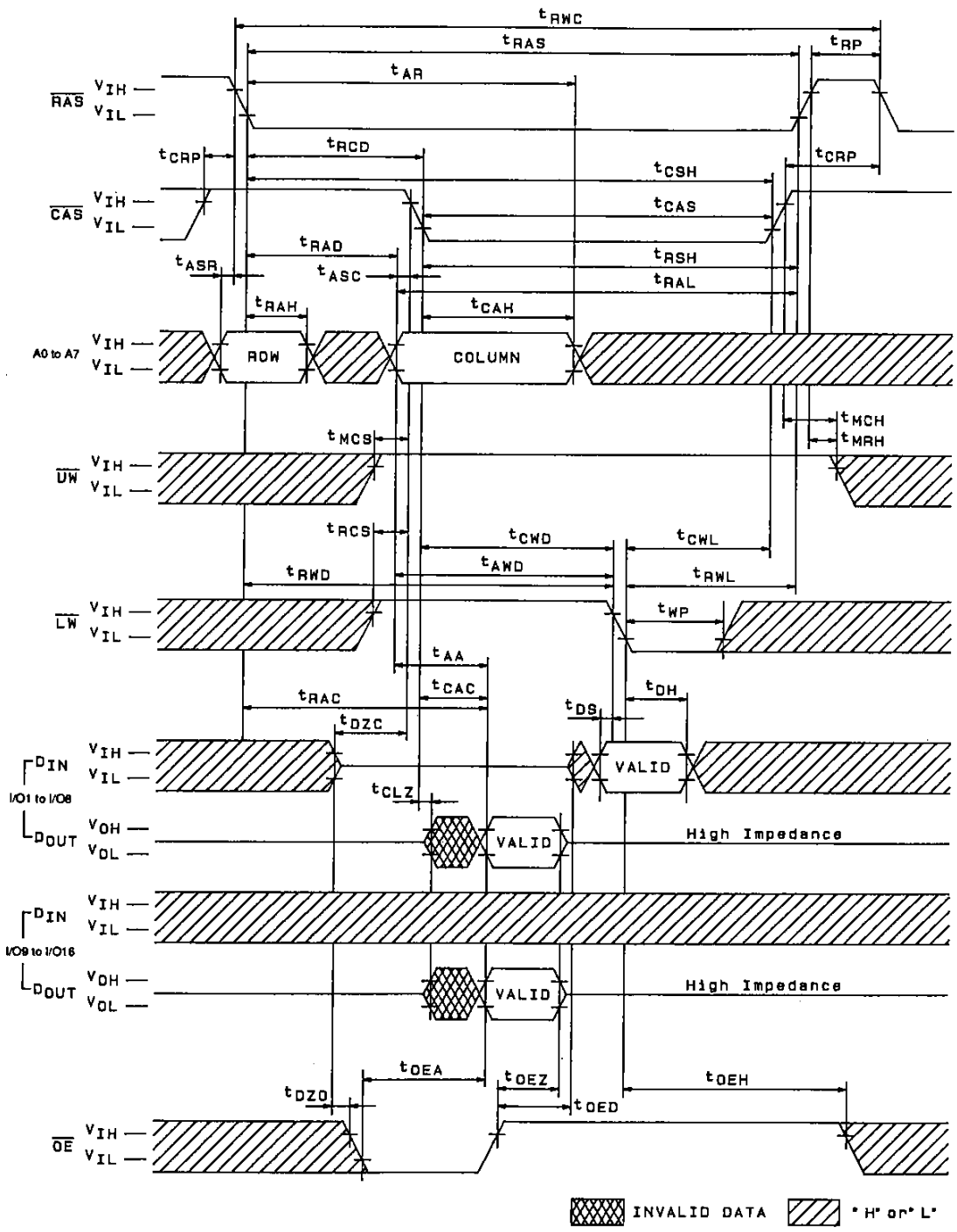
A02146

Read-Modify Upper Byte Write Cycle



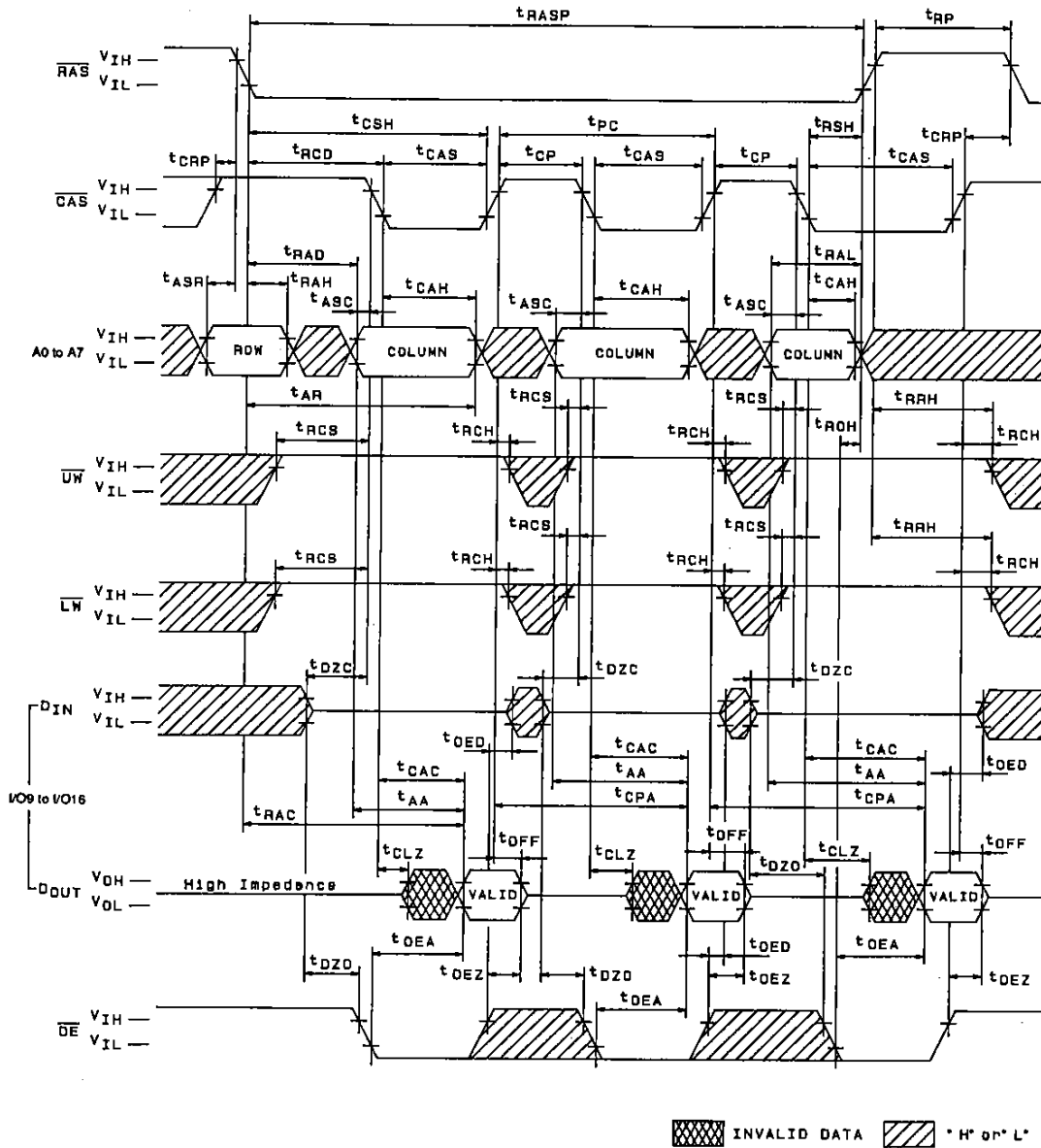
A02147

Read-Modify Lower Byte Write Cycle



A02148

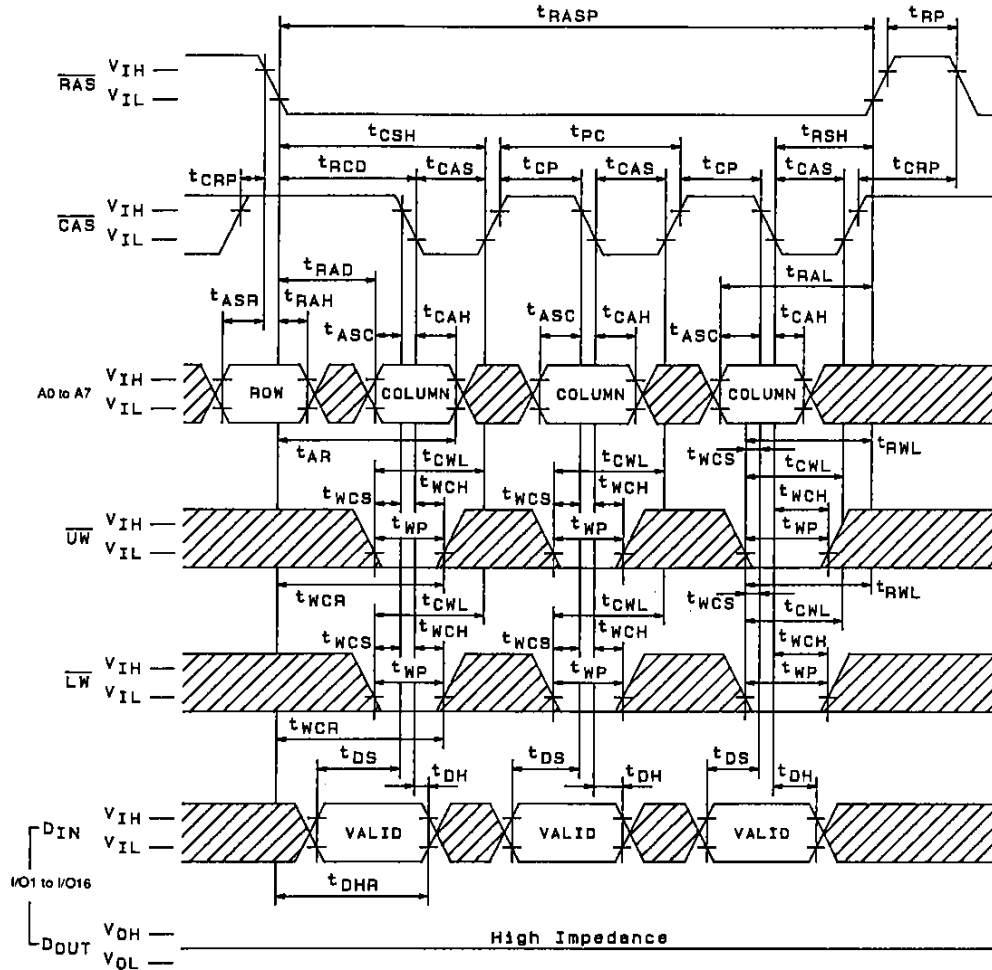
Fast Page Mode Read Cycle





A0214B



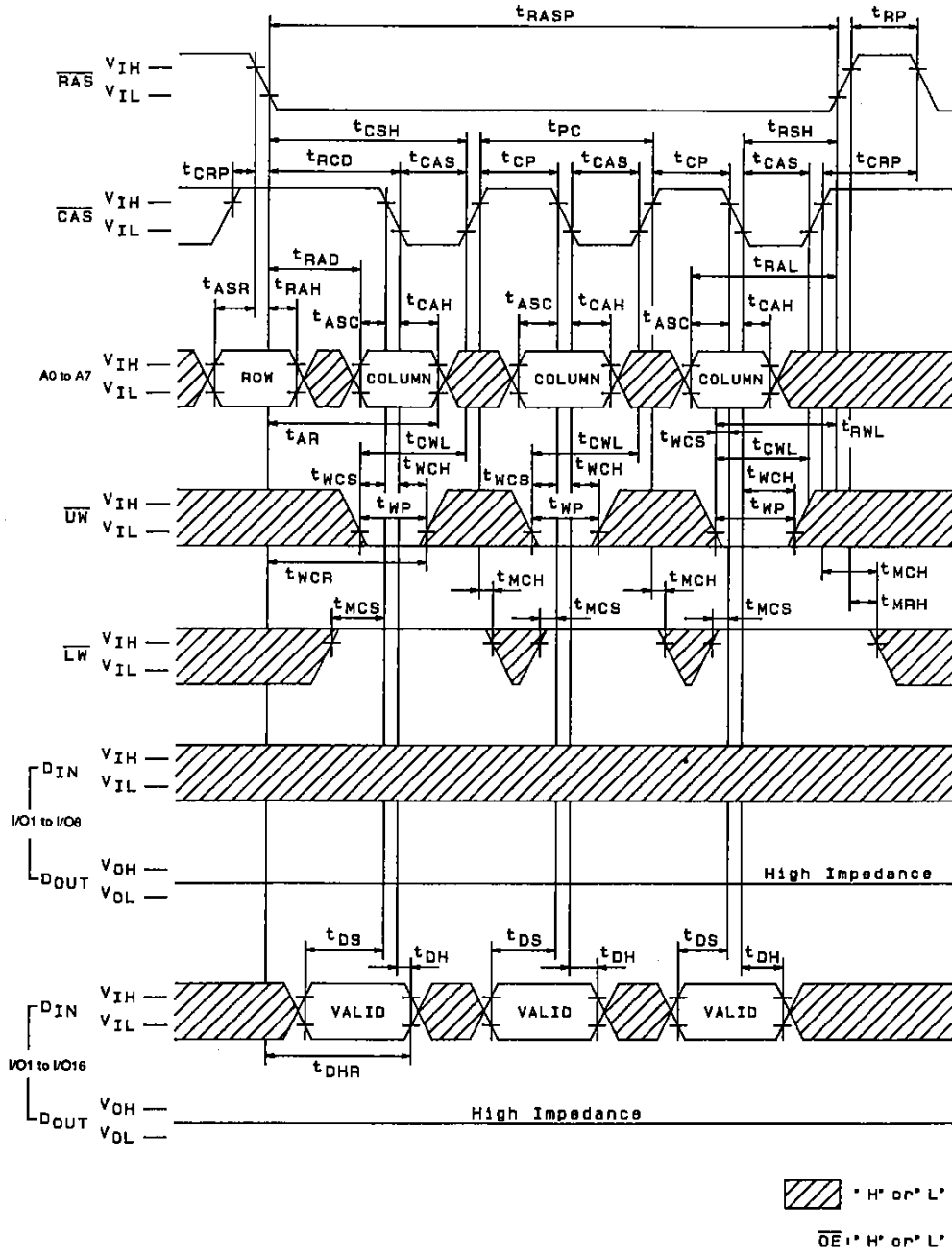
Fast Page Mode Early Write Cycle



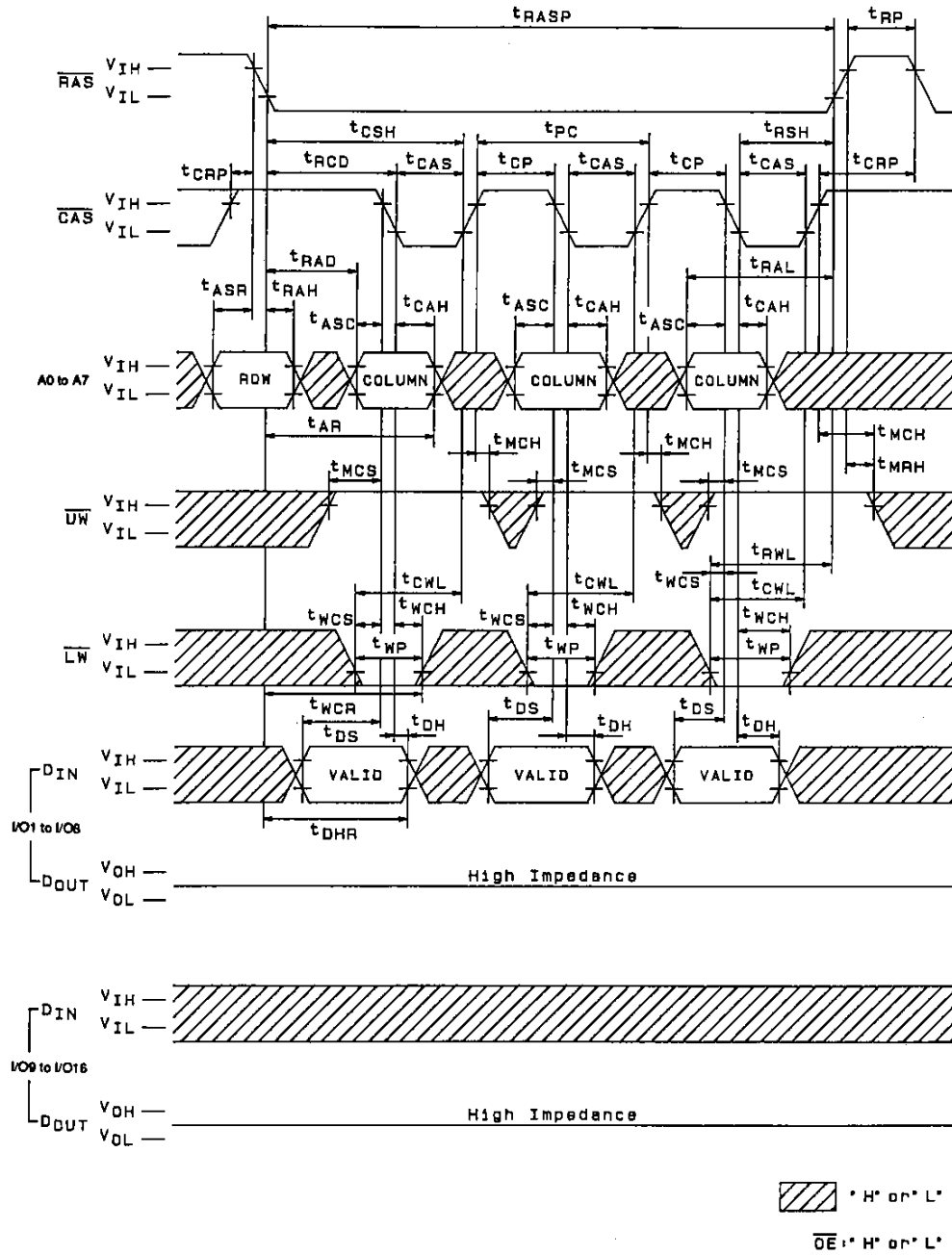
 H' or L'  
 H' or L'

A02180

Fast Page Mode Upper Byte Early Write Cycle



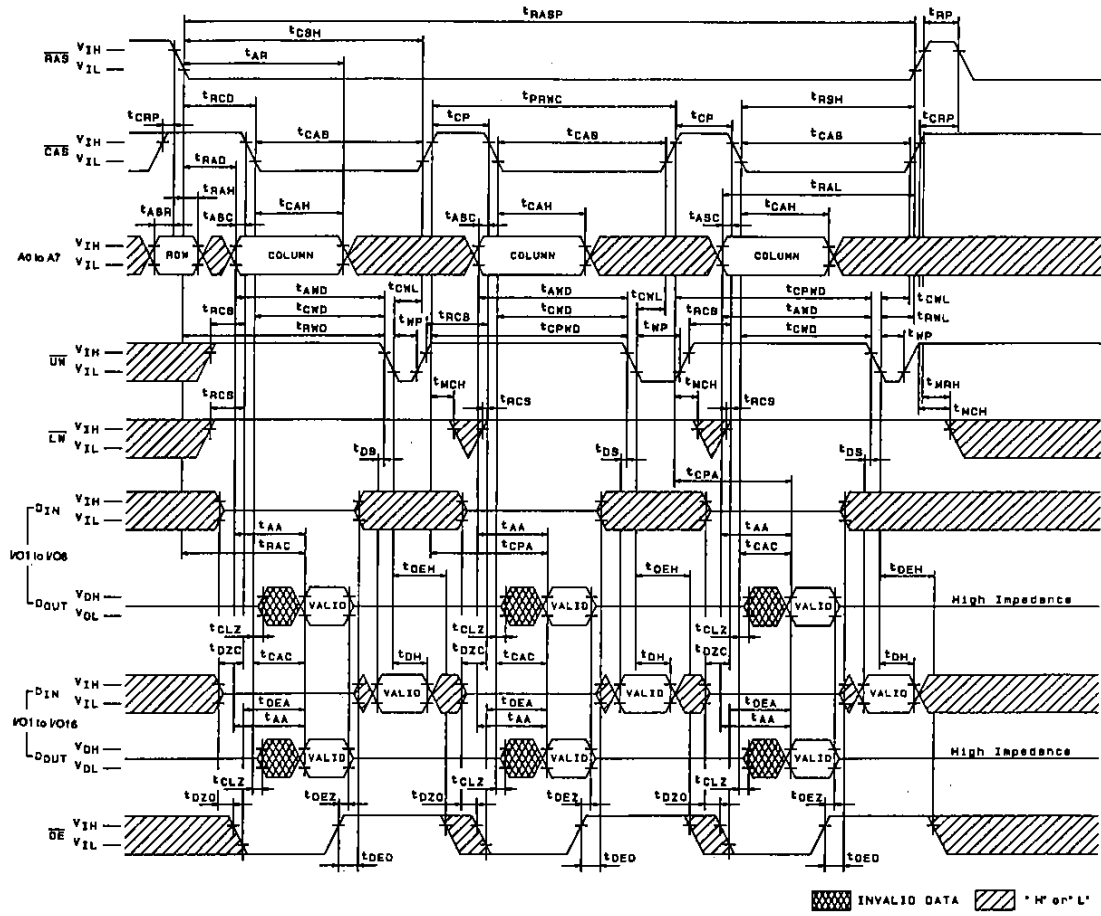
Fast Page Mode Lower Byte Early Write Cycle



A02152



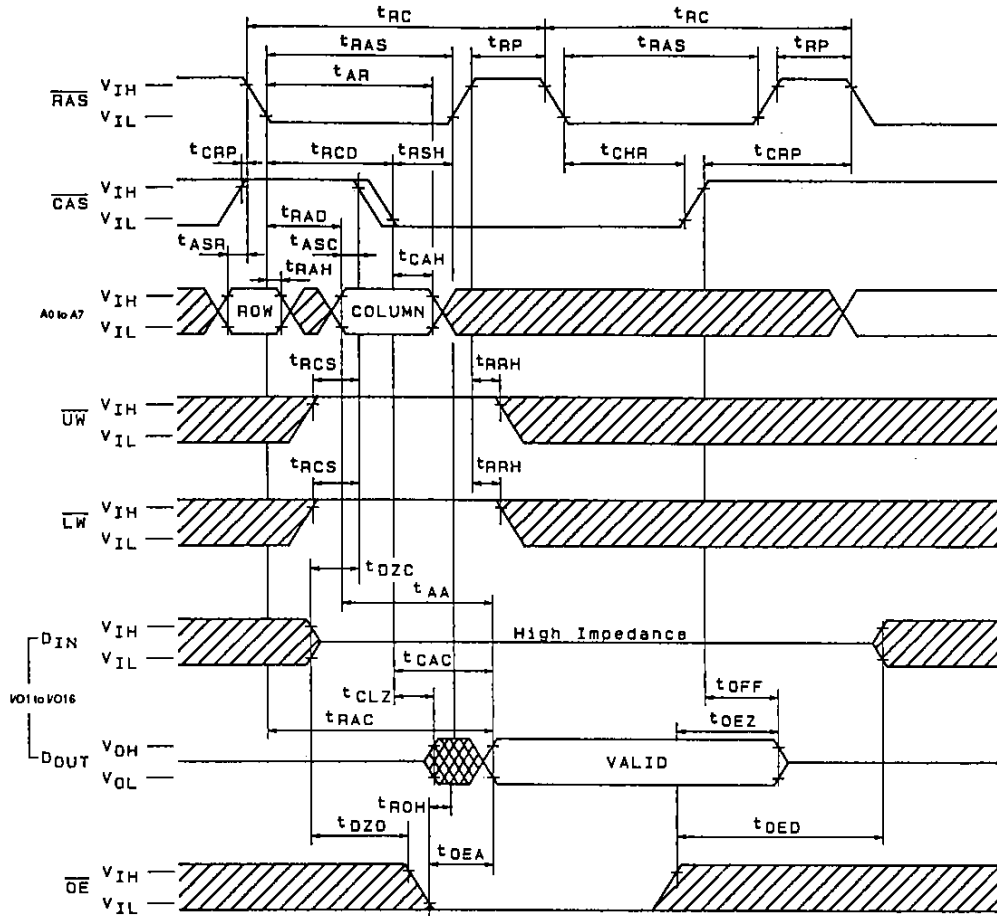
Fast Page Mode Read-Modify Upper Byte Write Cycle



A03878



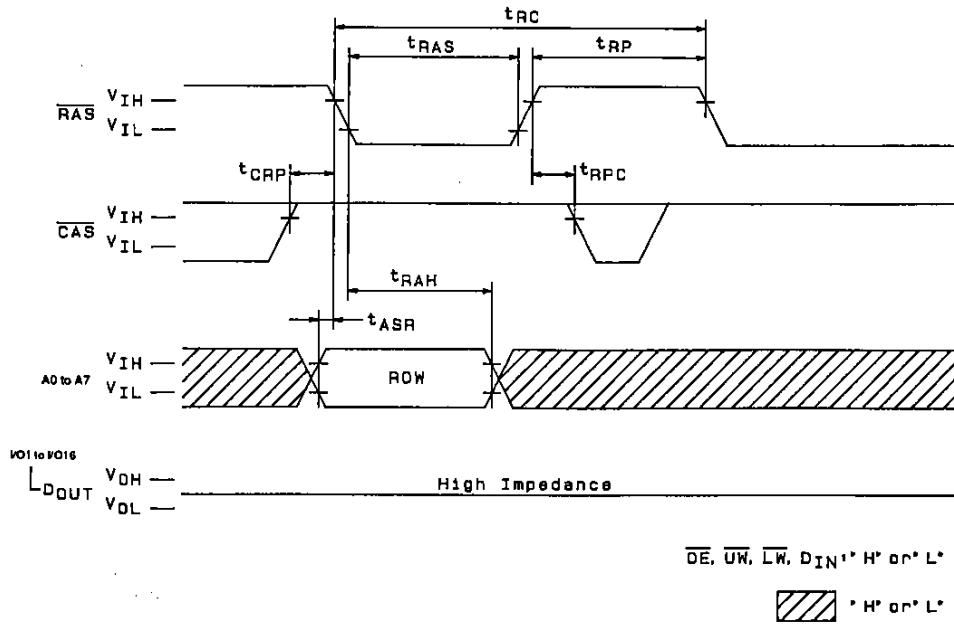
Hidden Refresh Cycle



INVALID DATA "H" or "L"

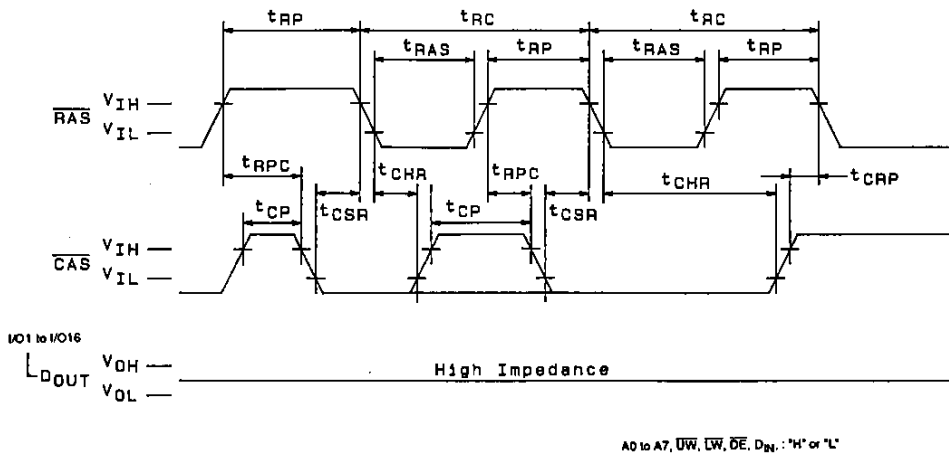
A03280

**RAS-Only Refresh Cycle**



A02157

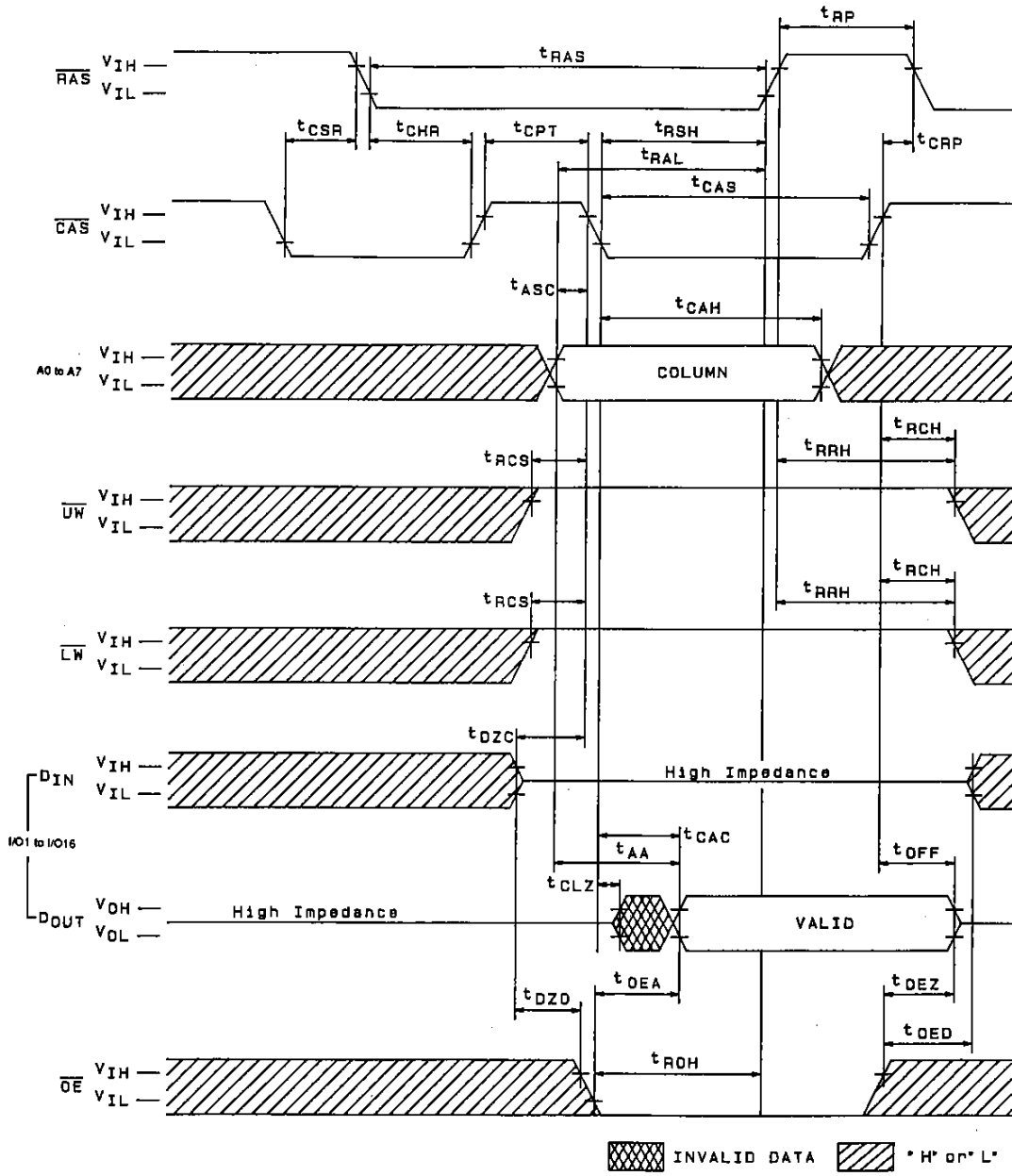
**CAS-Before-RAS Refresh Cycle**



A02158

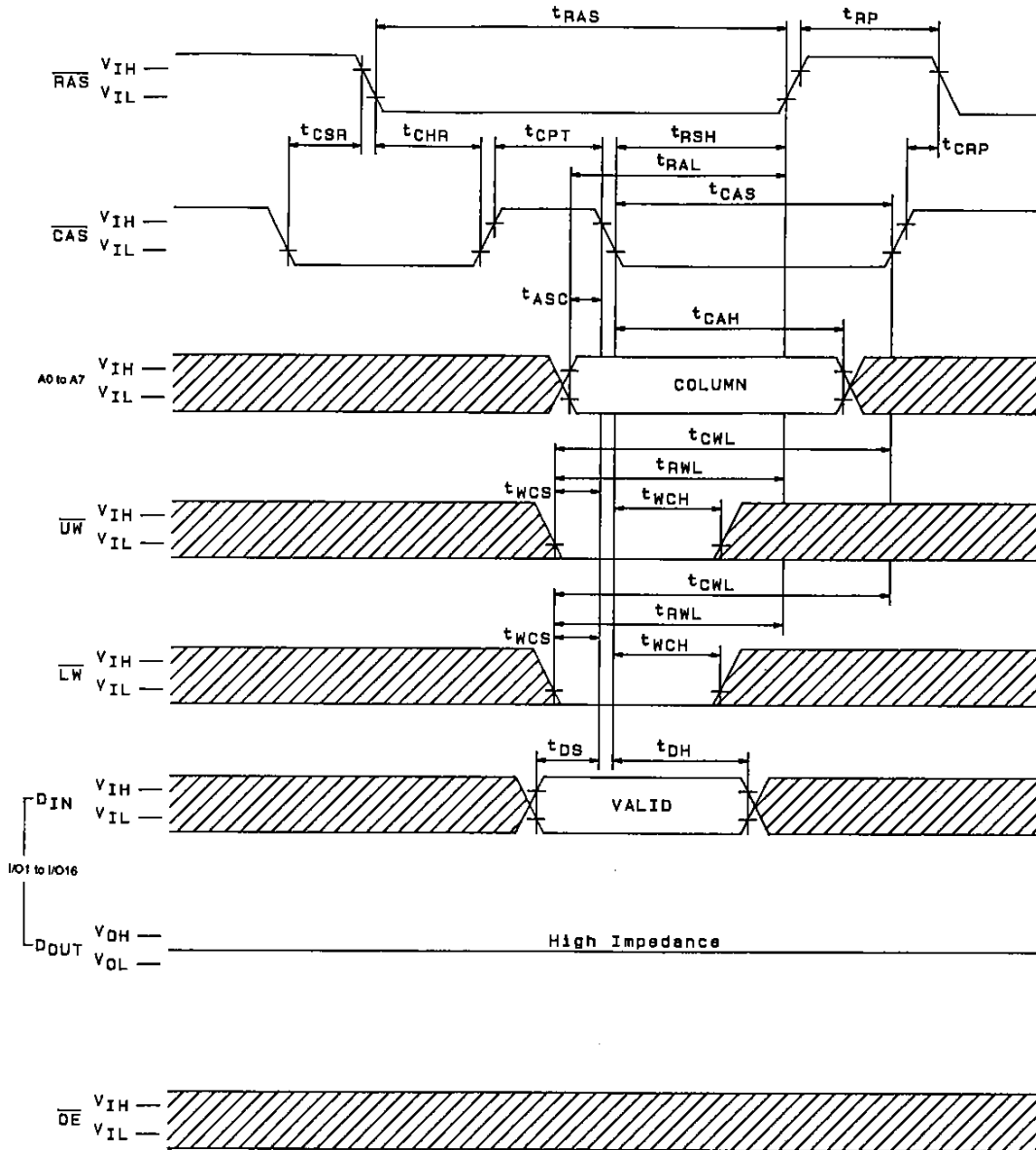


CAS-Before-RAS Refresh Counter Test Cycle (Read)



A02159

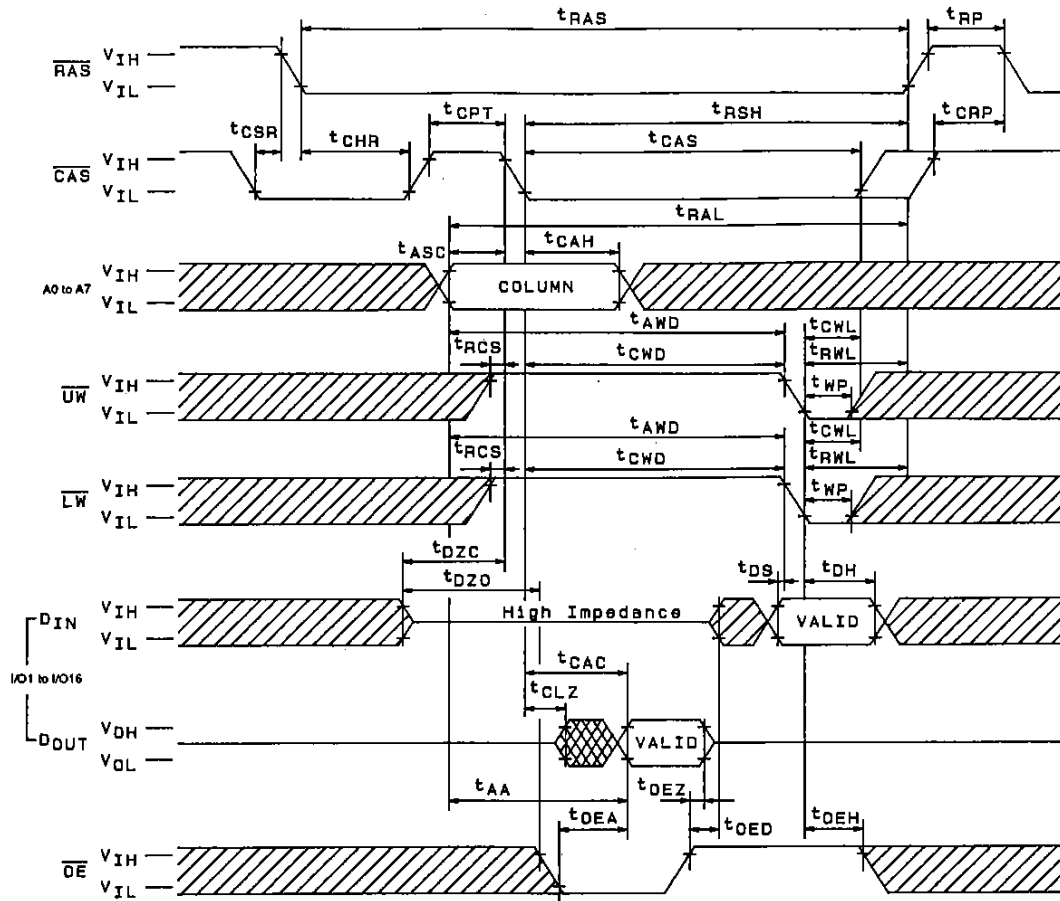
CAS-Before-RAS Refresh Counter Test Cycle (Write)



▨ \* H\* or \* L\*

A02180

CAS-Before-RAS Refresh Counter Test Cycle (Read-Modify-Write)



A021B1

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