ML9270A-xx

Preliminary

33-Segment VFD Driver

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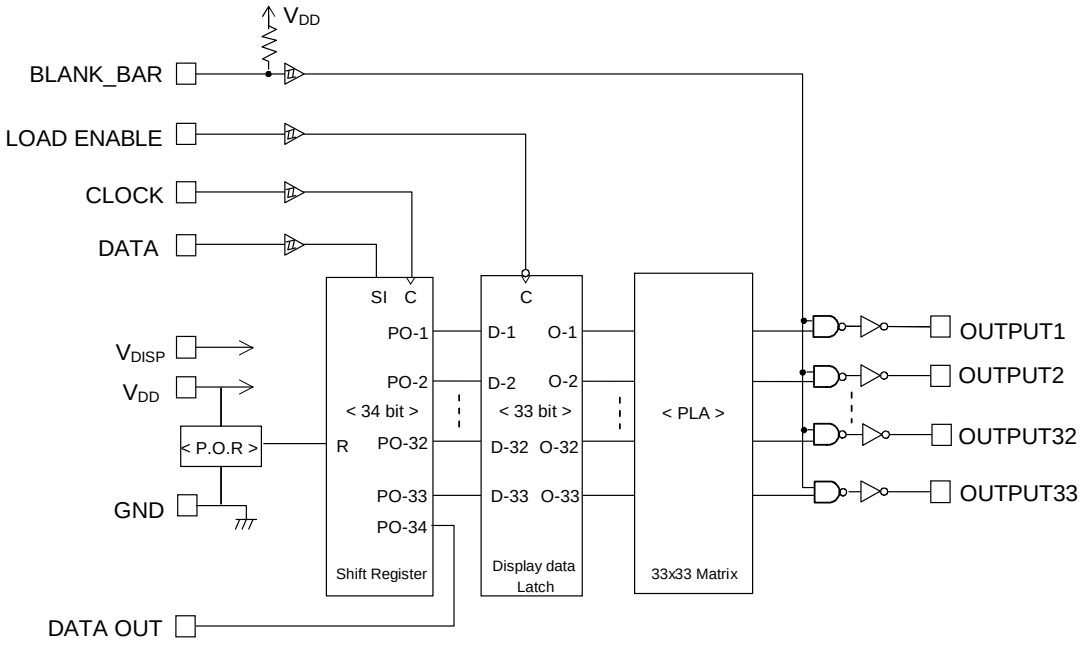
GENERAL DESCRIPTION

The ML9270A-xx is a monolithic IC designed for directly driving the anode of the vacuum fluorescent display tube.The device contains a 34-bit shift register circuit, 33-bit latch circuit, PLA (33*33 Matrix) and 33-output circuit on a single chip.
Display data is serially stored in the shift register at the rising edge of a CLOCK pulse.
Setting the BLANK_BAR pin low allows all the driver outputs to be driven low, which makes it possible to set the display blanking.
It is possible to use this device as “Self Load” by connecting DATA with LOAD ENABLE

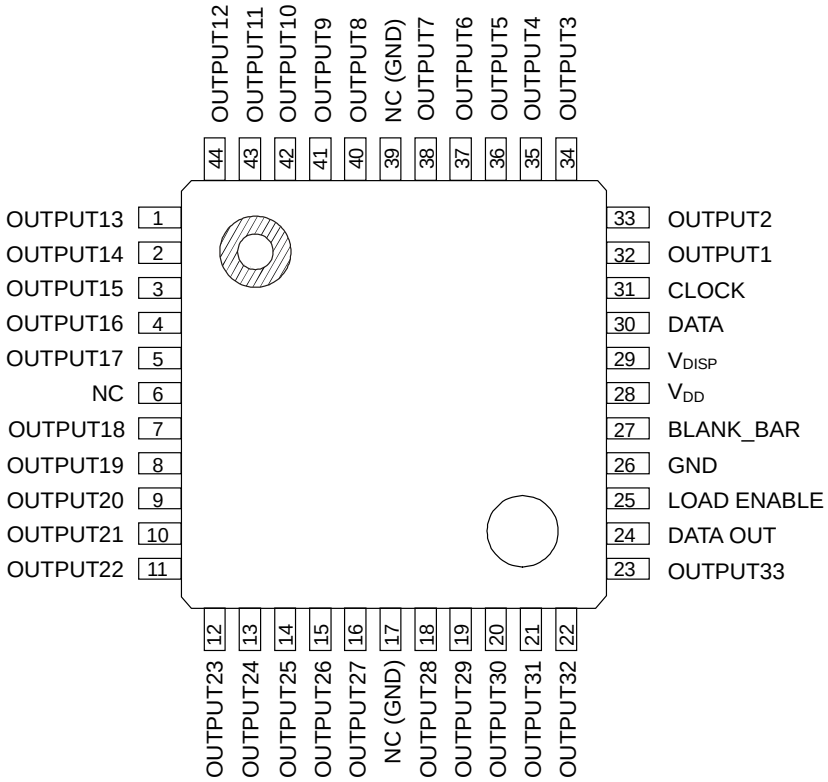
FEATURES

- Logic power supply (V_{DD}) : 3.3 V±10% or 5.0 V±10%
- VFD tube drive power supply (V_{DISP}) : 8 to 18 V
- VFD driver output can be connected directly to the VFD tube. No pull-down resistor is required.
- VFD driver output current
  - · Segment driver (OUTPUT1 to 13) : –6.0 mA (V_{DISP} = 9.5V)
  - · Segment driver (OUTPUT14 to 21) : –1.5 mA (V_{DISP} = 9.5V)
  - · Segment driver (OUTPUT22 to 33) : –6.0 mA (V_{DISP} = 9.5V)
- Data transfer speed : 5.0MHz
- Package : 44-pin plastic QFP (QFP44-P-910-0.80-2K)
- Built-in power on reset circuit

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

Pin	Symbol	Type	Connects to	Description
32 to 38, 40 to 44, 1	OUTPUT 1 to 13	O	VFD tube anode electrode	High voltage driver outputs for driving VFD tube. The driver outputs are in phase with the corresponding latch outputs. The direct connection to the anode of a VFD tube eliminates pull-down resistors. I_{OH1} > –1.5 mA
11 to 16, 18 to 23	OUTPUT 22 to 33			
2 to 5, 7 to 10	OUTPUT 14 to 21	O	VFD tube grid electrode	High voltage driver outputs for driving VFD tube. The driver outputs are in phase with the corresponding latch outputs. The direct connection to the anode of a VFD tube eliminates pull-down resistors. I_{OH1} > –6.0 mA
24	DATA OUT	O	LOAD ENABLE or Next Device	Serial data output pin of shift register. Data in output through the DATA OUT pin in synchronization with the CLOCK signal. It is possible to use this device as "Self Load" by connecting DATA with LOAD ENABLE.
28	V_{DD}	—	Power supply	V_{DD}-GND are power supplies for internal logic. V_{DISP}-GND are power supplies for driving fluorescent tubes. Apply V_{DISP} after V_{DD} is applied.
29	V_{DISP}			
26	GND			
25	LOAD ENABLE	I	Micro-Controller or DATA OUT	Latch signal input pin of display data latch logic. If the LOAD ENABLE pin is high, the data of the shift register is through. If the LOAD ENABLE pin is low, the data of the shift register does the latch.
27	BLANK_BAR	I	Micro-Controller	BLANK_BAR input pin with a built-in pull-up resistor. The BLANK_BAR pin is normally being set high. If the BLANK_BAR pin is low, the all driver outputs are "L" level.
30	DATA	I	Micro-Controller	Serial data input pin of the shift register. Display data (positive logic) is input in through the DATA pin synchronization with CLOCK.
31	CLOCK	I	Micro-Controller	Shift register clock input pin. Shift register reads data through DATA while the CLOCK pin is low state and the data in the shift register is shifted from one stage to the next stage at the rising edge of the CLOCK.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	—	–0.3 to +6.5	V
Supply Voltage (2)	V_{DISP}	—	–0.3 to +25	V
Input Voltage	V_{IN}	—	–0.3 to V_{DD}+0.3	V
Output Voltage (1)	V_{O1}	DATA OUT	–0.3 to V_{DD}+0.3	V
Output Voltage (2)	V_{O2}	OUTPUT1 to 33	–0.3 to V_{DISP}+0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C
Power Dissipation	P_D	Ta < 105°C	266	mW
Output Current	I_{O1}	OUTPUT1 to 13, OUTPUT 22 to 33	–18.0 to +2.0	mA
	I_{O2}	OUTPUT 14 to 21	–4.5 to +2.0	
	I_{O3}	DATA OUT	–2.0 to +2.0	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (1)	V_{DD}	When the power supply voltage is 5.0 V (typ.)	4.5	5.0	5.5	V
		When the power supply voltage is 3.3 V (typ.)	3.0	3.3	3.6	V
Supply Voltage (2)	V_{DISP}	—	8	—	18	V
CLOCK Frequency	f_{CLK}	—	—	—	5.0	MHz
Operating Temperature	Ta	—	–40	—	+105	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5.0 V±10% or 3.3 V±10%, V_{DISP} = 8 to 18 V, f_{CLK} = 5.0 MHz, Ta = –40 to +105°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition	Min.	Typ.	Max.	Unit
High Level Input Voltage	V_{IH}	All inputs	V_{DD} = 5.0 V ± 10 %	0.7 V_{DD}	—	—	V
			V_{DD} = 3.3 V ± 10 %	0.8 V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All inputs	V_{DD} = 5.0 V ± 10 %	—	—	0.3 V_{DD}	V
			V_{DD} = 3.3 V ± 10 %	—	—	0.2 V_{DD}	V
High Level Input Current	I_{IH1}	*1	V_{IH} = V_{DD}	–1.0	—	+1.0	µA
	I_{IH2}	BLANK_BAR	V_{IH} = V_{DD}	–1.0	—	+1.0	µA
Low Level Input Current	I_{IL1}	*1	V_{IL} = 0.0 V	–1.0	—	+1.0	µA
	I_{IL2}	BLANK_BAR *4	V_{DD} = 5.0 V, V_{IL} = 0.0 V	–120	–75	–30	µA
			V_{DD} = 3.3 V, V_{IL} = 0.0 V	–60	–38	–15	µA
High Level Output Voltage	V_{OH1}	*2	V_{DISP} = 9.5 V, I_{OH1} = –6.0 mA	V_{DISP}–0.5	—	—	V
	V_{OH2}	*3	V_{DISP} = 9.5 V, I_{OH2} = –1.5 mA	V_{DISP}–0.5	—	—	V
	V_{OH3}	DATA OUT	V_{DD} = 5.0 V, I_{OH3} = –500 uA	V_{DD}–0.4	—	—	V
			V_{DD} = 3.3 V, I_{OH3} = –500 uA	V_{DD}–0.3	—	—	V
Low Level Output Voltage	V_{OL1}	*2, *3	V_{DISP} = 9.5 V, I_{OL1} = 500 uA	—	—	2.0	V
	V_{OL2}	DATA OUT	V_{DD} = 5.0 V, I_{OL2} = 500 uA	—	—	0.4	V
			V_{DD} = 3.3 V, I_{OL2} = 500 uA	—	—	0.3	V
Supply Current (1) (Dynamic Mode)	I_{DD}	V_{DD}	V_{DD} = 5.0 V ± 10 % Input Data = ”1”0”1”..	—	—	2.5	mA
			V_{DD} = 3.3 V ± 10 % Input Data = ”1”0”1”..	—	—	2.0	mA
	I_{DISP}	V_{DISP}	Input Data = ”1”0”1”..	—	—	0.5	mA
Supply Current (2) (Static Mode)	I_{DDS}	V_{DD}	No Operation, Typ.: Ta = 25°C, Max.:Ta = 85°C	—	1.0	10.0	µA
	I_{DISPS}	V_{DISP}		—	1.0	20.0	µA

*1 : DATA, CLOCK, LOAD ENABLE terminals.
*2 : OUTPUT1 to 13, OUTPUT22 to 33 terminals.
*3 : OUTPUT14 to 21 terminals.
*4 : To BLANK_BAR input, the low level driver capability more than 600uA should be set.

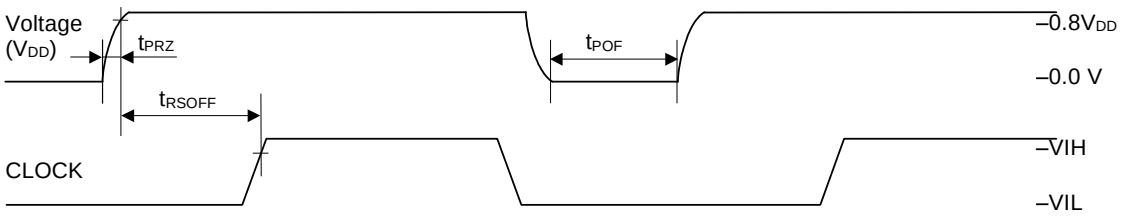
AC Characteristics

(V_{DD} = 5.0 V±10% or 3.3 V±10%, V_{DISP} = 8 to 18 V, f_{CLK} = 5.0 MHz, Ta = –40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLOCK Pulse Width	t_W(CLK)	—	100	—	—	ns
DATA Setup Time	t_{SU}(D-CLK)	—	50	—	—	ns
DATA Hold Time	t_H(CLK-D)	—	50	—	—	ns
CLOCK - LOAD ENABLE Setup Time	t_{SU}(CLK-LAT)	—	50	—	—	ns
LOAD ENABLE - CLOCK Setup Time	t_{SU}(LAT-CLK)	Normal Operation	50	—	—	ns
LOAD ENABLE Pulse Width	t_W(LAT)		400	—	—	ns
BLANK_BAR Pulse Width	t_W(BK)		5	—	—	µs
DATA OUT Delay Time	t_{PD}	$C_{l\,l}$ = 30 pF	—	25	50	ns
All Output Delay Time	t_{DLH}	$C_{l\,d}$ = 100 pF	—	1.0	2.0	µs
	t_{DHL}		—	1.0	2.0	µs
All Output Slew Rate	t_{TLH}	$C_{l\,d}$ = 100 pF t_R = 20 to 80% t_F = 80 to 20%	—	0.5	1.0	µs
	t_{THL}		—	0.5	1.0	µs
V_{DD} Rise Time	t_{PRZ}	Mounted in a unit	—	—	100	µs
V_{DD} Off Time	t_{POF}	Mounted in a unit, V_{DISP} = 0.0 V	5.0	—	—	ms
CLOCK Wait Time	t_{RSOFF}	—	300	—	—	µs

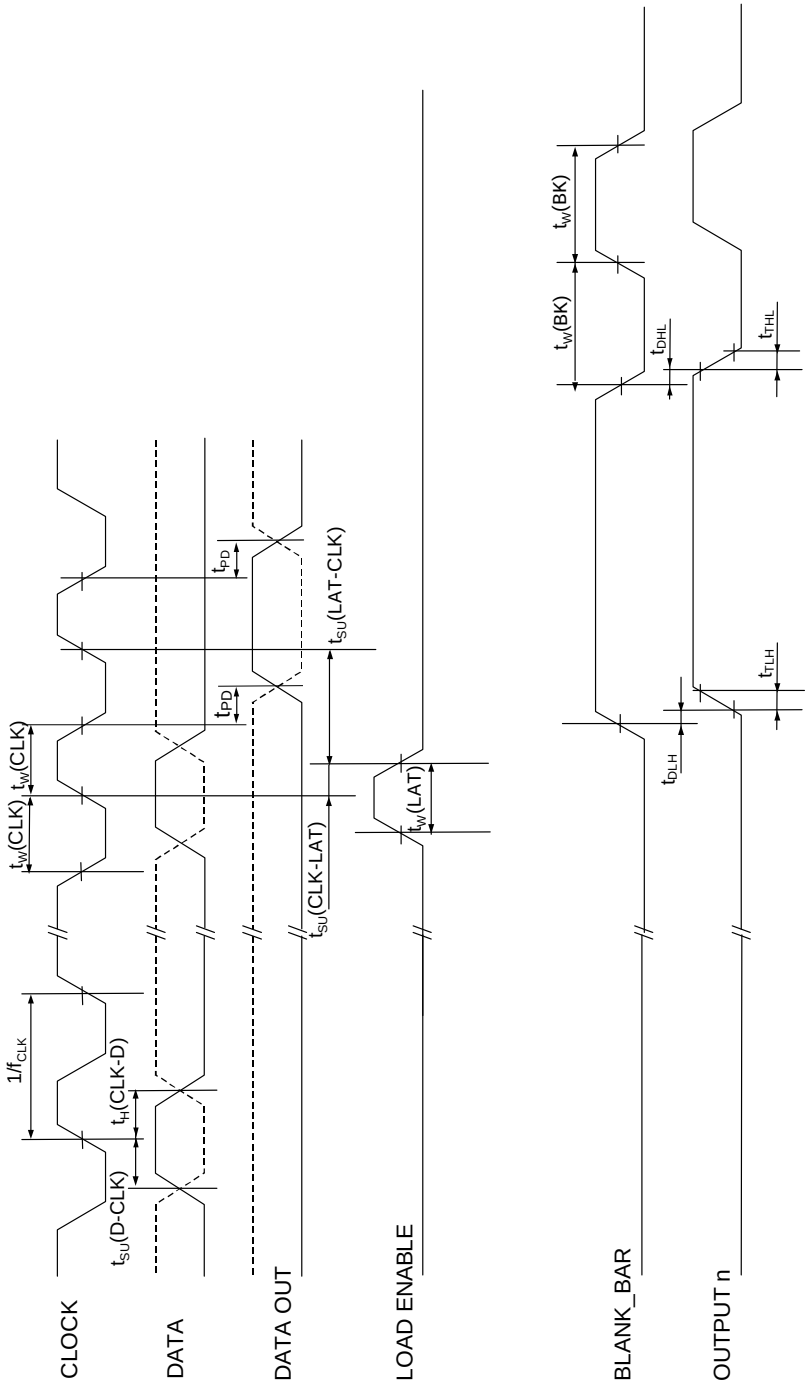
Define of Input Voltage

Symbol	V_{DD} = 3.3 V ±10%	V_{DD} = 5.0 V ±10%
V_{IH} / V_{IL}	0.8 V_{DD} / 0.2 V_{DD}	0.7 V_{DD} / 0.3 V_{DD}



TIMING DIAGRAMS

Symbol	V_{DD} = 3.3 V ±10%	V_{DD} = 5.0 V ±10%
V_{IH} / V_{IL}	0.8 V_{DD} / 0.2 V_{DD}	0.7 V_{DD} / 0.3 V_{DD}
V_{OH} / V_{OL}	0.8 V_{DISP} / 0.2 V_{DISP}	0.8 V_{DISP} / 0.2 V_{DISP}
	0.8 V_{DD} / 0.2 V_{DD}	0.8 V_{DD} / 0.2 V_{DD}



FUNCTIONAL DESCRIPTION

General Description
The ML9270A is a CMOS multi-digit display driver and consists of a 34-bit shift register, a 33-bit latch, and a 33-bit VF tube driver.

Pin Description
(1) DATA
This is a serial data input terminal of the 34-stage shift register.

(2) CLOCK
This is a Clock input terminal of the shift resister to shift an input signal at its leading edge.

(3) LOAD ENABLE
This is an input terminal to transfer the data from the shift register to the data latch circuit to hold it. After the data is held, the terminal initializes the data of the shift register.
These functions are executed at the leading edge of an input signal.

(4) BLANK_BAR
This is an input terminal to turn all the OUTPUT terminals OFF(Low), which contains a pull-up resistor.

(5) OUTPUT1 to 33
These are output terminal for the VFD tube driver.Each terminal outputs data which is transferd from the corresponding bit of the shift register and held in the data latch circuit.

(6) DATA OUT
This is a data output terminal of the shift register to output data on the last stage of the 34-stage shift register.

(7) V_{DD}
This is a Logic power supply terminal.

(8) V_{DISP}
This is a driver output power supply terminal.

(9) GND
This is a grounding terminal.

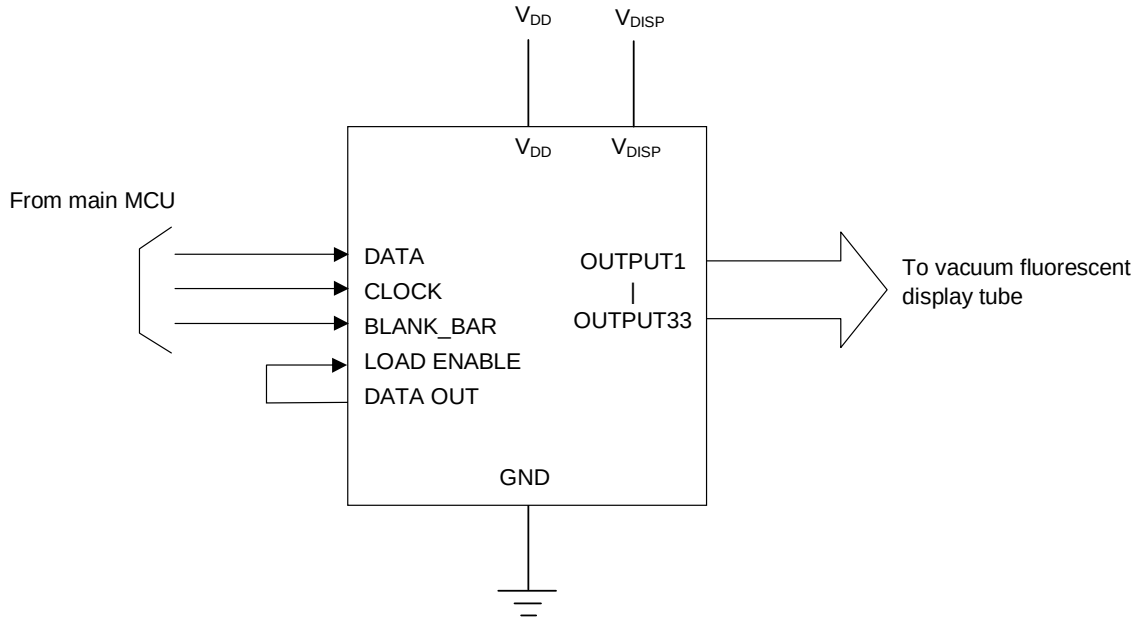
Shift Register Numbers (Bit Numbers) and Corresponding OUTPUT Pin Names (OUTPUT Numbers)(Code 01)

Register No.	33	32	31	30	29	28	27	26	25	24	23	
OUTPUT No.	33	32	31	30	29	28	27	26	25	24	23	
Register No.	22	21	20	19	18	17	16	15	14	13	12	
OUTPUT No.	22	21	20	19	18	17	16	15	14	13	12	
Register No.	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUT No.	11	10	9	8	7	6	5	4	3	2	1	DATA OUT

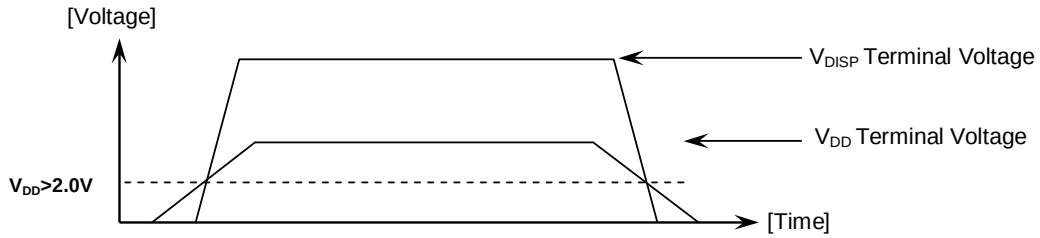
Self Loading

The self loading is a function that 33-bit display data that is sent to the shift register is loaded into the display data latch automatically.

The DATA OUT pin is connected directly to the LOAD ENABLE pin, as shown in the diagram below, and register number 0 (the final bit) is set to "1" by data sent from the MCU. This enables the contents of the shift register to be automatically loaded into the display data latch on the 34th CLOCK pulse and the shift register to be initialized (set to "0").



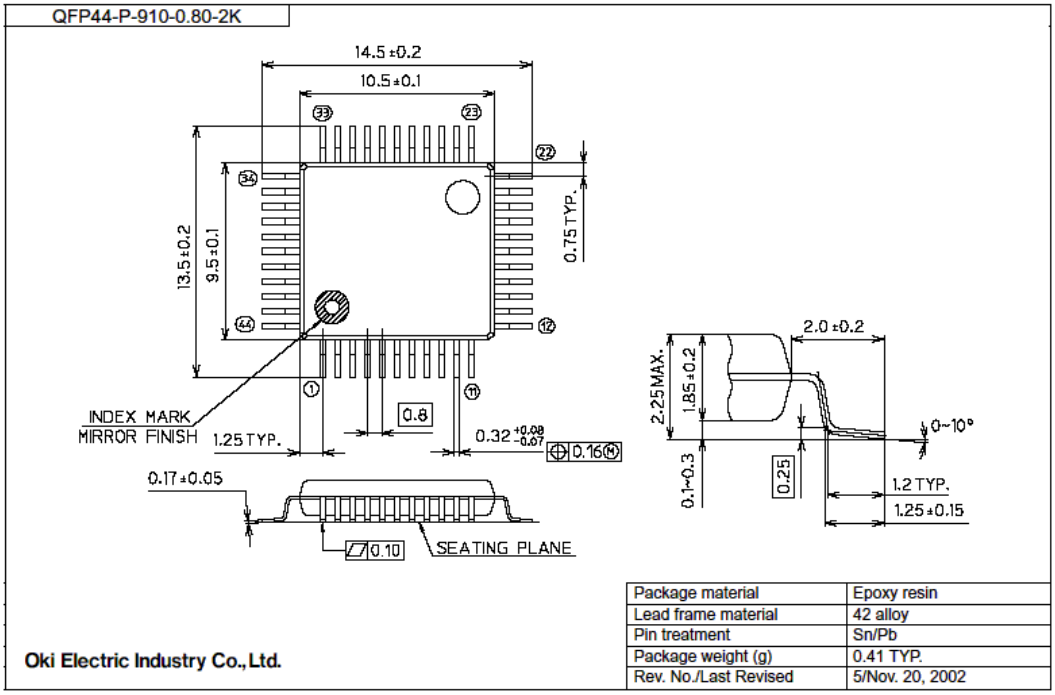
POWER-ON/OFF TIMING



To prevent IC from malfunctioning, after V_{DD} is applied as soon as possible that V_{DISP} is applied.
When turning off the power, after V_{DISP} is applied as soon as possible that V_{DD} is applied.

PACKAGE DIMENSIONS

(Unit: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Sn/Pb
Package weight (g)	0.41 TYP.
Rev. No./Last Revised	5/Nov. 20, 2002

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9270A-01	Mar. 28, 2006	–	–	Preliminary edition 1

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