

**SANYO**

No.2310A

**LA7311****VTR-Use PAL/SECAM Discriminator  
S-VHS Discriminator**

The LA7311 is a PAL/SECAM discriminator and S-VHS discriminator IC. When used as PAL/SECAM discriminator, the LA7311 is highly resistant to noise and is capable of providing high sensitive discrimination, because it uses the FM demodulation, peak detection method. Further, the LA7311 uses very few external parts, making the space-saving and low-cost discrimination block available, because it requires neither ceramic filter nor resonance coil. When used as S-VHS discriminator, the LA7311 is also capable of providing high sensitive discrimination.

**Features**

- Highly resistant to noise and burst input level variations and capable of providing high sensitive discrimination.
- Fewer external parts required (Neither ceramic filter nor resonance coil required)
- On-chip display LED drivers
- The polarity of burst gate pulse may be either positive or negative.

**Absolute Maximum Ratings at Ta = 25°C**

			unit
Maximum Supply Voltage	$V_{CCmax}$	7.0	V
Allowable Power Dissipation	$P_{dmax}$	130	mW
Operating Temperature	$T_{opr}$	-10 to +70	°C
Storage Temperature	$T_{stg}$	-40 to +125	°C

**Operating Conditions at Ta = 25°C**

			unit
Recommended Supply Voltage	$V_{CC}$	5.0	V
Operating Voltage Range	$V_{CCop}$	4.5 to 6.0	V

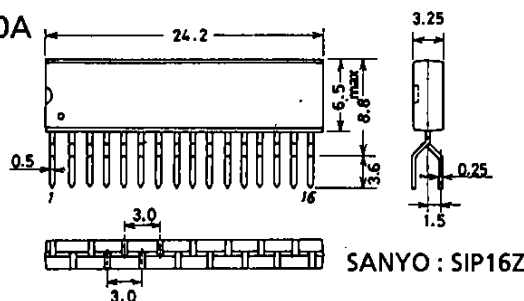
**Operating Characteristics at Ta=25°C,  $V_{CC}=5V$** 

			min	typ	max	unit
Current Dissipation	$I_{CC}$		6.7	9.6	12.4	mA
F-V Conversion Gain (PB)	$\Delta V_P$	Difference between output at 4.4MHz and output at 4.25MHz	75	105	135	mV
F-V Conversion Gain (REC)	$\Delta V_R$	Difference between output at 4.4MHz and output at 4.25MHz	75	105	135	mV
PAL → SECAM Inversion Voltage Difference	$V_{8-12}$		35	50	65	mV
R/P Switching Threshold Voltage	$V_{3TH}$		2.0	2.35	2.7	V
BG Threshold Voltage I	$V_{7TH}$		1.5	1.7	1.9	V
BG Threshold Voltage II	$V_{11TH}$		3.2	3.4	3.6	V
Forced PAL Threshold Voltage	$V_{10TH}$		1.3	1.7	2.2	V
Forced SECAM Threshold Voltage	$V_{2TH}$		1.7	2.0	2.3	V
Discrimination Output Voltage I	$V_{13}$	$I_D=5mA$	4.0	4.2	4.4	V
Discrimination Output Voltage II	$V_{15}$	$I_D=5mA$	4.0	4.2	4.4	V

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**Package Dimensions 3020A**

(unit: mm)



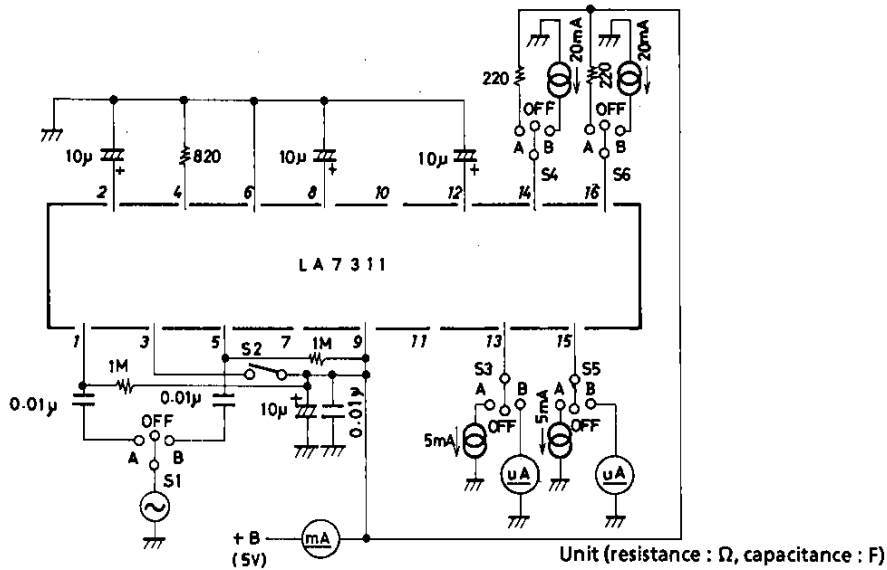
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			min	typ	max	unit
Discrimination Output Leakage Current I	$I_{13(Leak)}$			0	5	$\mu A$
Discrimination Output Leakage Current II	$I_{15(Leak)}$			0	5	$\mu A$
Pin 12 DC Voltage	$V_{12}$	4.43MHz, 100mVp-p input	2.1	2.6	3.1	V
Input Burst Level	$V_{IN}$		60	100	200	mVp-p
Driver Saturation Voltage I	$V_{14}$	$I_D=20mA$		170	400	mV
Driver Saturation Voltage II	$V_{16}$	$I_D=20mA$		170	400	mV

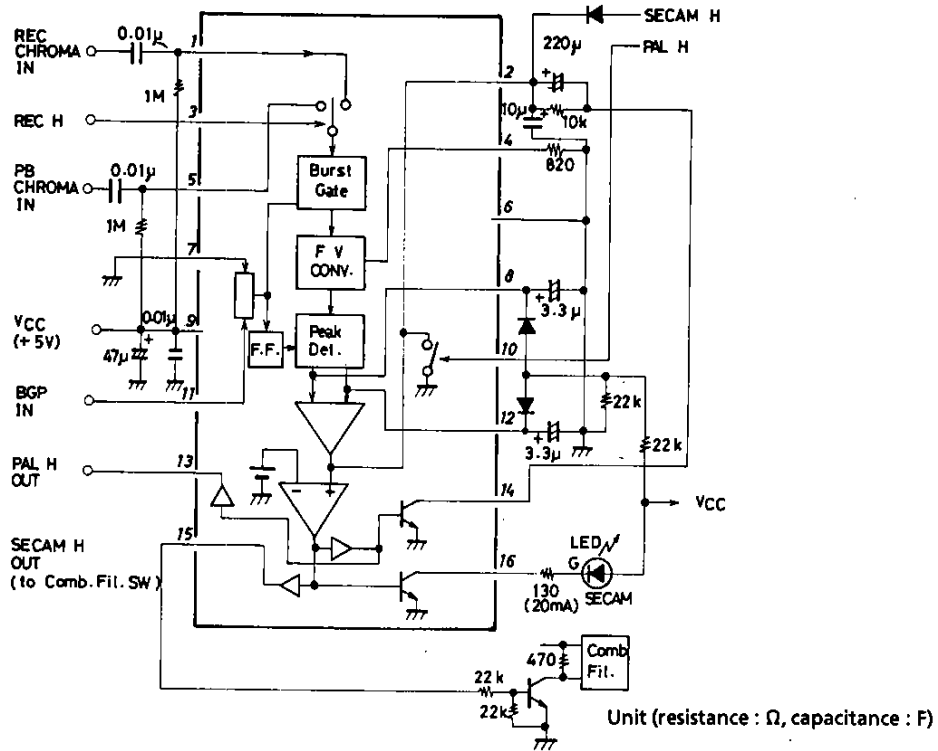
Test Circuit



Note: Remove the 1MΩ resistor connected across pins (1) and (9) and across pins (5) and (9) except when measuring  $\Delta V_P$ ,  $\Delta V_R$ ,  $V_{12}$ ,  $V_{IN}$ .

	S1	S2	S3	S4	S5	S6	Conditions
$I_{CC}$	off	off	off	off	off	off	$V_9 = 5V$
$\Delta V_P$	B	↓	↓	↓	↓	↓	100mV <sub>p-p</sub> , difference between $V_8$ (or $V_{12}$ ) potential at 4.4MHz input and $V_8$ (or $V_{12}$ ) potential at 4.25MHz input
$\Delta V_R$	A	on	↓	↓	↓	↓	100mV <sub>p-p</sub> , difference between $V_8$ (or $V_{12}$ ) potential at 4.4MHz input and $V_8$ (or $V_{12}$ ) potential at 4.25MHz input
$V_{8-12}$	off	off	↓	A	↓	↓	a (rise from 0) when $V_7=0V$ , $V_{11}=5V$ , $V_8=1.9V$ , $V_{12}=1.9V+a$ , $V_{14}>4V$
$V_{3TH}$	↓	↓	↓	off	↓	↓	$V_3$ (rise from 0) when $V_1=V_7=V_{11}=0V$ , $V_8<0.1V$
$V_{7TH}$	↓	↓	↓	↓	↓	↓	$V_7$ (rise from 0) when $V_{11}=5V$ , $V_8>1.0V$
$V_{11TH}$	↓	↓	↓	↓	↓	↓	$V_{11}$ (fall from 5V) when $V_7=0V$ , $V_8>1.0V$
$V_{10TH}$	↓	↓	↓	↓	↓	A	$V_{10}$ (rise from 0) when $V_7=V_{11}=0V$ , $V_{16}>4V$
$V_{2TH}$	↓	↓	↓	A	↓	off	$V_2$ (rise from 0) when $V_8=V_{12}=3V$ , $V_{14}>4V$
$V_{13}$	↓	↓	A	off	↓	↓	Pin 13 potential when $V_2=0V$ , drive current 5mA
$V_{15}$	↓	↓	off	↓	A	↓	Pin 15 potential when $V_2=3V$ , drive current 5mA
$I_{13(Leak)}$	↓	↓	B	↓	off	↓	$V_2=3V$ , current which flows when pin 13 is connected to GND
$I_{15(Leak)}$	↓	↓	off	↓	B	↓	$V_2=0V$ , current which flows when pin 15 is connected to GND
$V_{14(sat)}$	↓	↓	↓	B	off	↓	Pin 14 potential when $V_2=0V$ , drive current 20mA
$V_{16(sat)}$	↓	↓	↓	off	↓	B	Pin 6 potential when $V_2=3V$ , drive current 20mA
$V_{12}$	A	on	↓	↓	↓	off	100mV <sub>p-p</sub> , 4.43MHz CW input, Apply 4μs BGP input to pin 11.
$V_{IN}$	A/B	on/off	↓	↓	↓	↓	

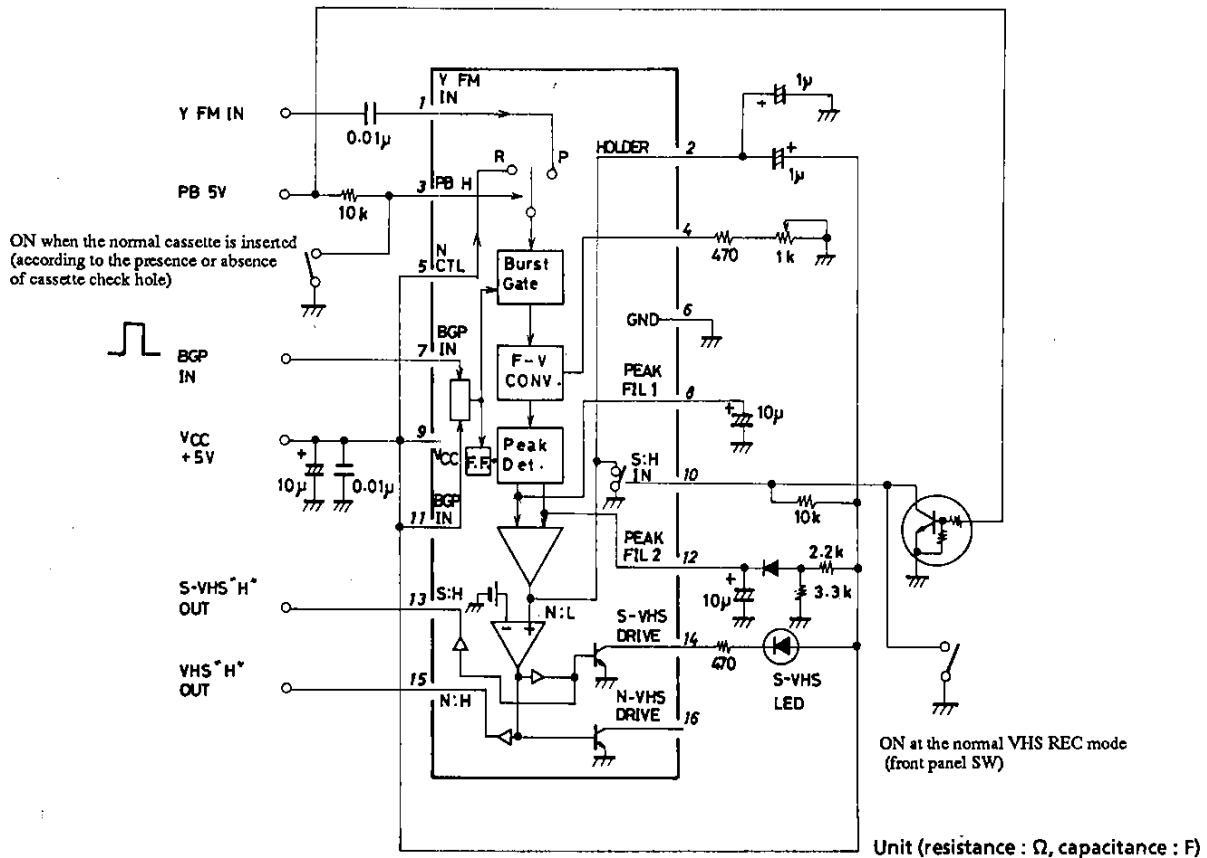
Equivalent Circuit Block Diagram and Sample Application Circuit (PAL/SECAM Discrimination)



Note 1: When the BGP is positive, apply an input to pin 7 and connect pin 11 to V<sub>CC</sub>.

Note 2: When pin 10 is not in use, bring pin 10 to the open state or connect to GND.

Sample S-VHS Discriminator



Adjustment method: Adjust the VR (from VR center position) connected to pin 4 so that the DC voltage on pin 8 becomes 2.0V when the FM-Y signal at the (normal) VHS REC tape PB mode is input.

Note 1: When the BGP is negative, apply an input to pin 11 and connect pin 7 to GND.

Note 2: Pin 5 may be connected to GND.

Mode	Type of Cassette	Panel SW	V <sub>10</sub>	V <sub>2</sub>	Display
REC	N	S	H	L	S
		N	L	H	N
	S	S	H	L	S
		N	L	H	N
PB	N	S	L	H	N
		N	L	H	N
	S	S	L	Automatic discrimination	
		N	L	Automatic discrimination	

N; NORMAL VHS, S; S-VHS

### Input/Output Configuration

Unit (resistance :  $\Omega$ )

Pin	Pin Name	I/O Impedance or I/O Configuration	DC Voltage	Remarks
1	REC CHROMA IN	10k $\Omega$	4.1V	
2	SECAM HOLDER			SECAM at 2.0V or greater
3	R/P CONTROL		0V (PB mode)	REC at 2.4V or greater
4	CURRENT SOURCE	Open emitter	410mV	
5	PB CHROMA IN	10k $\Omega$	4.1V	
6	GND		0V	
7	BGP IN	Base		Burst gate at 1.7V or greater
8	PEAK FILTER 1	Emitter follower		
9	V <sub>CC</sub>		5V	
10	PAL HIGH IN		0V	Forced PAL at 1.7V or greater
11	$\overline{\text{BGP}}$ IN	Base		Burst gate at 3.4V or less
12	PEAK FILTER 2	Emitter follower		
13	PAL HIGH OUT		4.1V (PAL mode)	Up to 5mA
14	PAL DRIVE	NPN open collector		Up to 25mA
15	SECAM HIGH OUT		4.1V (SECAM mode)	Up to 5mA
16	SECAM DRIVE	NPN open collector		Up to 25mA

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