élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4453C
Video Fader

Features

- Complete two-input fader with output amplifier—uses no extra components
- 80 MHz bandwidth
- Fast fade control speed
- Operates on ±5V to ±15V supplies
- >60 dB attenuation @ 5 MHz

Applications

- Mixing two inputs
- Picture-in-picture
- Text overlay onto video
- General gain control

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL4453CN	−40°C to +85°C	14-Pin P-DIP	MDP0031
EL4453CS	−40°C to +85°C	14-Lead SOIC	MDP0027

General Description

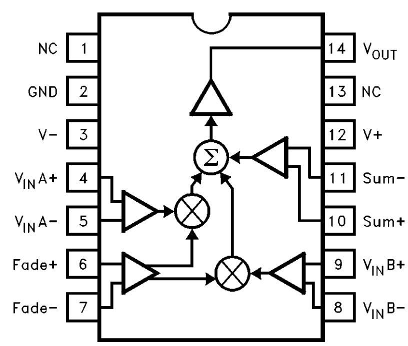
The EL4453C is a complete fader subsystem. It variably blends two inputs together for such applications as video picture-in-picture effects.

The EL4453C operates on ±5V to ±15V supplies and has an analog differential input range of ±2V. AC characteristics do not change appreciably over the supply range.

The circuit has an operational temperature of −40°C to +85°C and is packaged in 14-pin P-DIP and SO-14.

The EL4453C is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is free from latch up.

Connection Diagram



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January 1995 Rev A

Absolute Maximum Ratings $T_A = 25°C$

V+	Positive Supply Voltage	16.5V	I_{IN}	Current into any Input, or Feedback Pin	4 mA
V_S	V+ to V− Supply Voltage	33V	I_{OUT}	Output Current	30 mA
V_{IN}	Voltage at any Input or Feedback	V+ to V−	P_D	Maximum Power Dissipation	See Curves
ΔV_{IN}	Difference between Pairs of Inputs or Feedback	6V	T_A	Operating Temperature Range	−40°C to +85°C
			T_S	Storage Temperature Range	−60°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

Open-Loop DC Electrical Characteristics

Power Supplies at ±5V, Sum+ = Sum− = 0, $T_A = 25°C$

Parameter	Description		Min	Typ	Max	Test Level	Units
V_{DIFF}	V_{IN}A, V_{IN}B, or Sum Differential Input Voltage—	Clipping 0.2% Nonlinearity	1.8	2.0 0.7		I V	V V
V_{CM}	Common-Mode Range (All Inputs; $V_{DIFF} = 0$)	$V_S = \pm5V$ $V_S = \pm15V$	±2.5 ±12.5	±2.8 ±12.8		I I	V V
V_{OS}	A or B Input Offset Voltage				25	I	mV
V_{FADE}, 100%	Extrapolated Voltage for 100% Gain for V_{IN}A		0.9	1.05	1.2	I	V
V_{FADE}, 0%	Extrapolated Voltage for 0% Gain for V_{IN}A		−1.2	−1.15	−0.9	I	V
I_B	Input Bias Current (All Inputs) with all $V_{IN} = 0$			9	20	I	µA
I_{OS}	Input Offset Current between V_{IN}A+ and V_{IN}A−, V_{IN}B+ and V_{IN}B−, Fade+ and Fade−, and Sum+ and Sum−			0.2	4	I	µA
F_T	V_{IN}A Signal Feedthrough, $V_{FADE} = -1.5V$			−100	−60	I	dB
NL	A or B Input Nonlinearity, V_{IN} between +1V and −1V,	V_{IN}A or V_{IN}B Sum Input		0.2 0.5	0.5	I V	% %
R_{IN}, Signal	Input Resistance, A, B, or Sum Input			230		V	kΩ
R_{IN}, Fade	Input Resistance, Fade Input			120		V	kΩ
CMRR	Common-Mode Rejection Ratio, V_{IN}A or V_{IN}B		70	80		I	dB
PSRR	Power Supply Rejection Ratio		50	70		I	dB
E_G	Gain Error, $V_{FADE} = 1.5V$,	V_{IN}A or V_{IN}B Sum Input	−2 −4		+2 +4	I I	% %
V_O	Output Voltage Swing ($V_{IN} = 0$, V_{REF} Varied)	$V_S = \pm5V$ $V_S = \pm15V$	±2.5 ±12.5	±2.8 ±12.8		I I	V V
I_{SC}	Output Short-Circuit Current		40	85		I	mA
I_S	Supply Current, $V_S = \pm15V$			17	21	I	mA

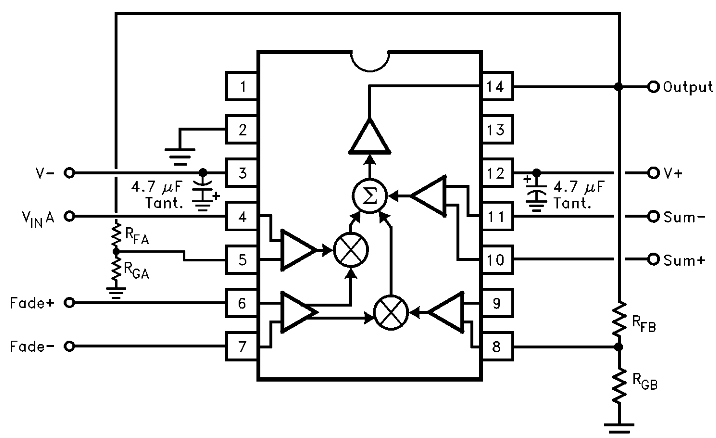
TD is 4.3in

Closed-Loop AC Electrical Characteristics

Power supplies at ±12V, T_A = 25°C, R_L = 500Ω, C_L = 15 pF, V_{FADE} = 1.5V, Sum+ = Sum− = 0

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, −3 dB	−3 dB Small-Signal Bandwidth, V_{IN}A or V_{IN}B		80		V	MHz
BW, ±0.1 dB	0.1 dB Flatness Bandwidth, V_{IN}A or V_{IN}B		9		V	MHz
Peaking	Frequency Response Peaking		1.0		V	dB
BW, Fade	−3 dB Small-Signal Bandwidth, Fade Input		80		V	MHz
SR	Slew Rate, V_{OUT} between −2V and +2V	TBD	380		I	V/µs
V_N	Input-Referred Noise Voltage Density		160		V	nV/Hz
F_T	Feedthrough of Faded-Out Channel, F = 3.58 MHz		−63		V	dB
dG	Differential Gain Error, V_{OFFSET} from 0 to ±0.714V, Fade at 100%					
	V_{IN}A or V_{IN}B		0.05		V	%
	Sum Input		0.35		V	%
dθ	Differential Phase Error, V_{OFFSET} from 0 to ±0.71V, Fade at 100%					
	V_{IN}A or V_{IN}B		0.05		V	(°)
	Sum Input		0.1		V	(°)

Test Circuit



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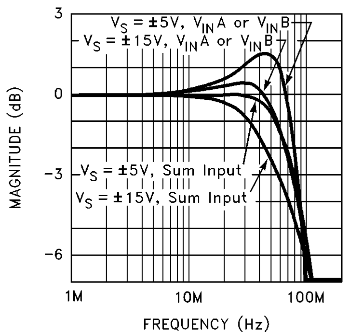
Note: For typical performance curves Sum+ = Sum− = 0, R_F = 0Ω, R_G = ∞, V_{FADE} = +1.5V, and C_L = 15 pF, unless otherwise noted.

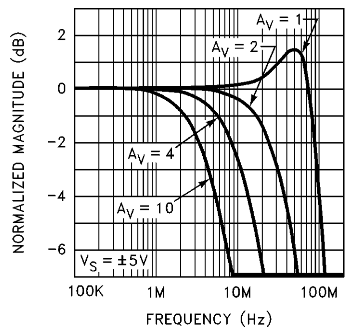
Typical Performance Curves

Frequency Response



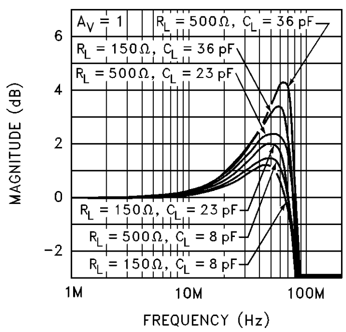
4453-3

Frequency Response vs Gain



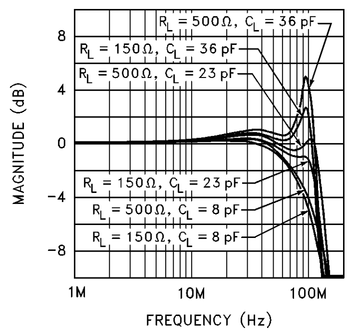
4453-4

Frequency Response for Various Loads, V_S = ±5V



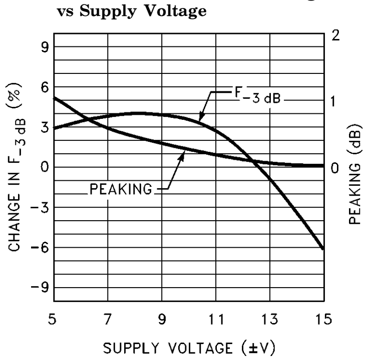
4453-6

Frequency Response for Various Loads, V_S = ±15V



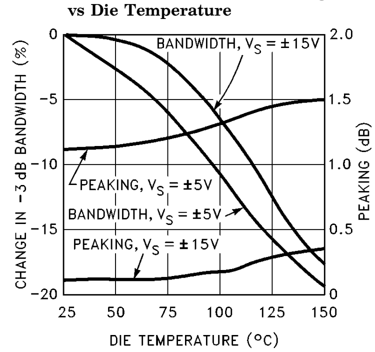
4453-7

−3 dB Bandwidth and Peaking vs Supply Voltage



4453-9

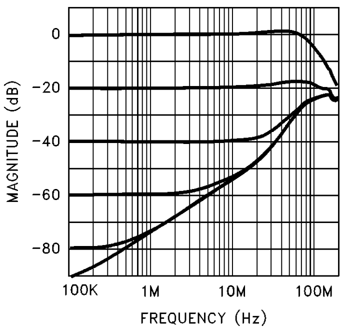
−3 dB Bandwidth and Peaking vs Die Temperature



4453-10

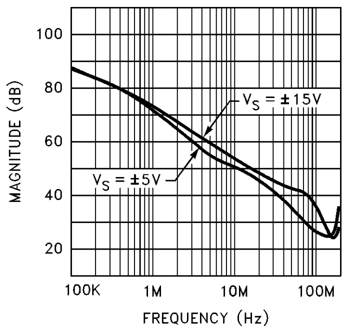
Typical Performance Curves — Contd.

Frequency Response for Different Gains, $V_S = \pm5V$



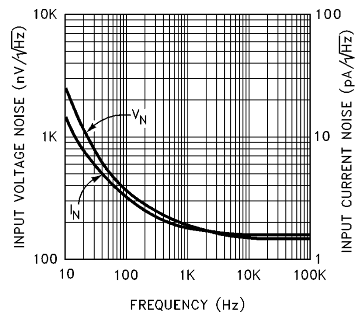
4453-5

Input Common-Mode Rejection Ratio vs Frequency



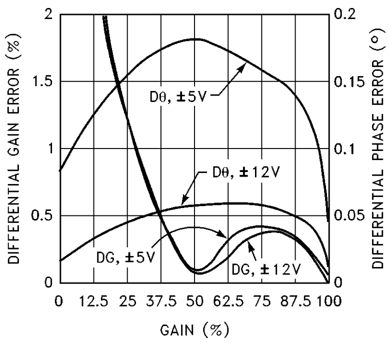
4453-8

Input Voltage and Current Noise vs Frequency



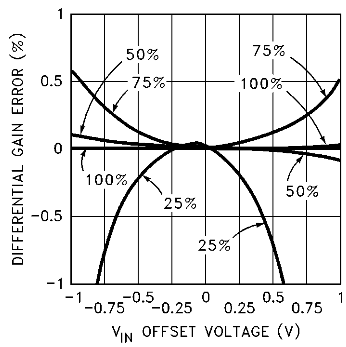
4453-11

V_{IN} Differential Gain and Phase Error vs Gain



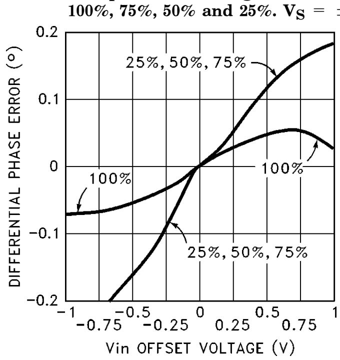
4453-14

V_{IN} Differential Gain Error vs Input Offset Voltage for Gain = 100%, 75%, 50% and 25%



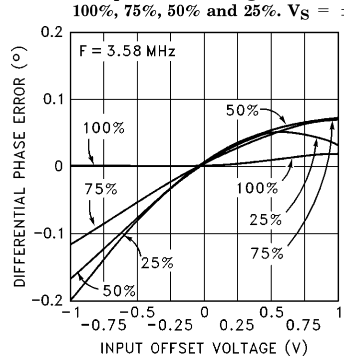
4453-15

V_{IN} Differential Phase Error vs Input Offset Voltage for Gain = 100%, 75%, 50% and 25%. $V_S = \pm5V$



4453-16

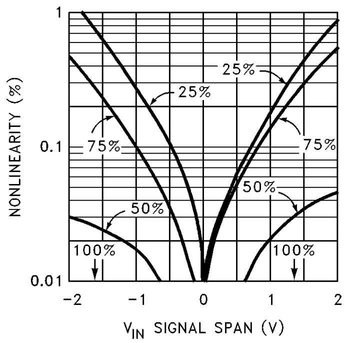
V_{IN} Differential Phase Error vs Input Offset Voltage for Gain = 100%, 75%, 50% and 25%. $V_S = \pm12V$



4453-17

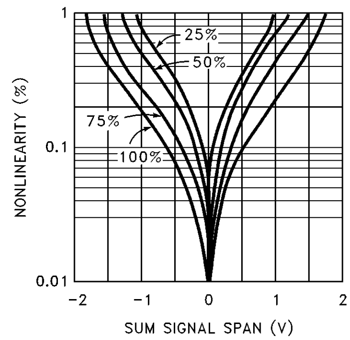
Typical Performance Curves — Contd.

Nonlinearity vs V_{IN} Signal Span



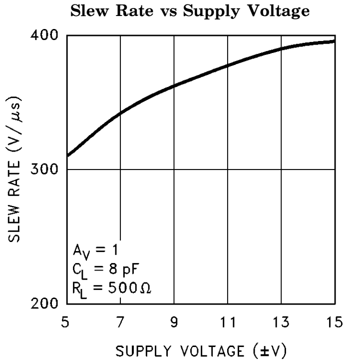
4453-12

Nonlinearity vs Sum Signal Span



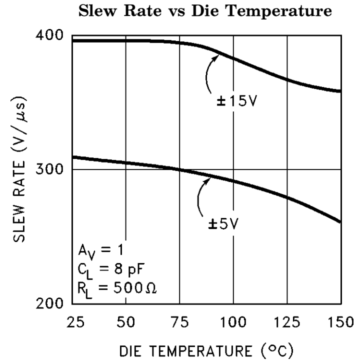
4453-13

Slew Rate vs Supply Voltage



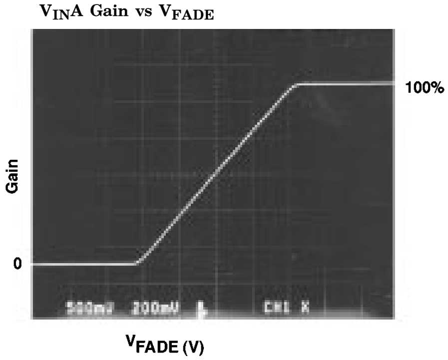
4453-18

Slew Rate vs Die Temperature



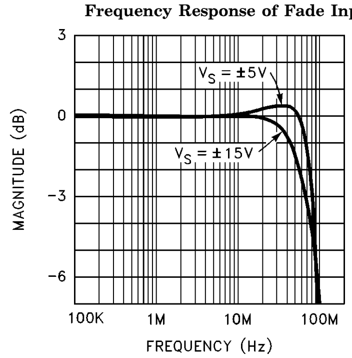
4453-19

V_{IN}A Gain vs V_{FADE}



4453-20

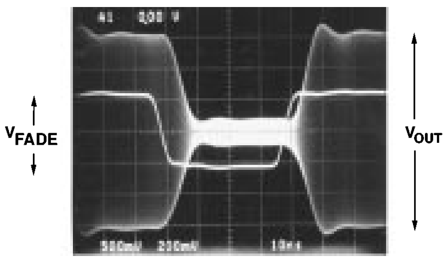
Frequency Response of Fade Input



4453-21

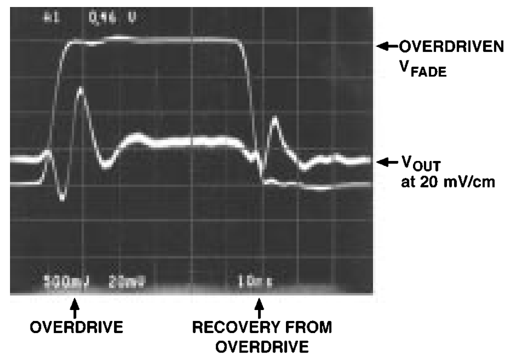
Typical Performance Curves — Contd.

Transient Response of Fade Input Constant Signal into $V_{IN}A$



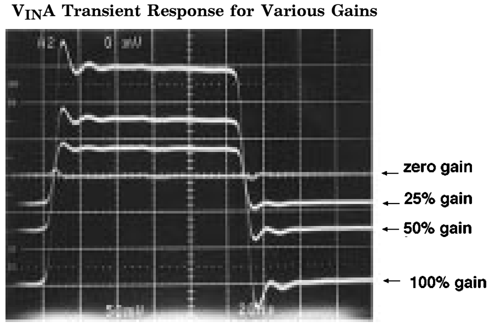
4453-22

Overdrive Recovery Glitch from V_{FADE}, No Input Signal



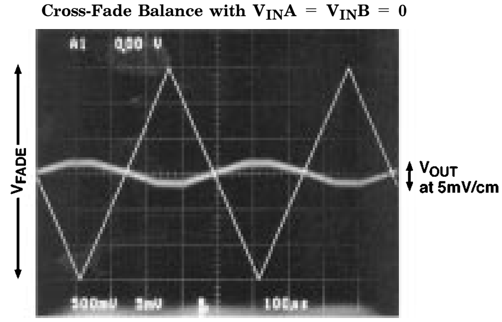
4453-23

$V_{IN}A$ Transient Response for Various Gains



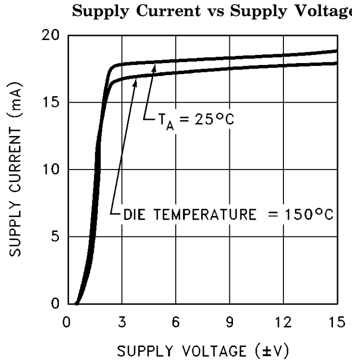
4453-24

Cross-Fade Balance with $V_{IN}A = V_{IN}B = 0$



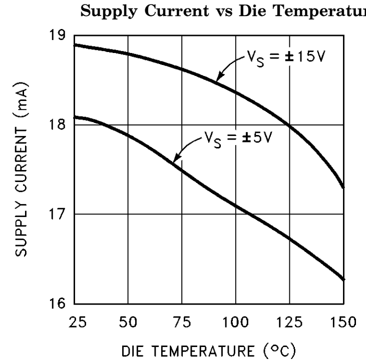
4453-25

Supply Current vs Supply Voltage



4453-26

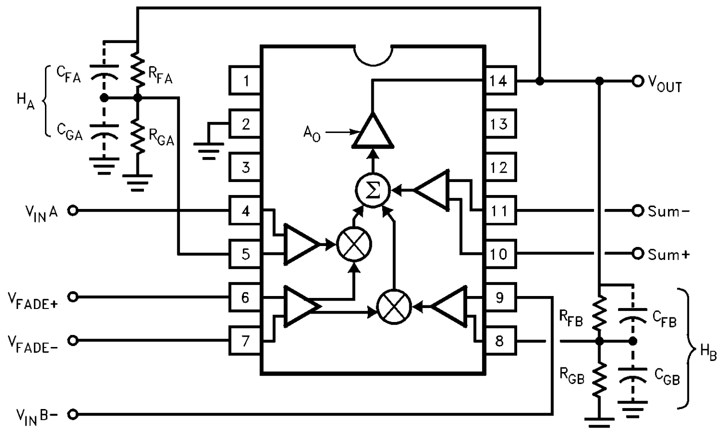
Supply Current vs Die Temperature



4453-27

Applications Information

The EL4453C is a complete two-quadrant fader/ gain control with 80 MHz bandwidth. It has four sets of inputs; a differential signal input $V_{IN}A$, a differential signal input $V_{IN}B$, a differential fade-controlling input V_{FADE}, and another differential input Sum which can be used to add in a third input at full gain. This is the general connection of the EL4453C:



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Applications Information — Contd.

The gain of the feedback dividers are H_A and H_B, and $0 \le H \le 1$. The transfer function of the part is

$$V_{OUT} = A_O \times [((V_{IN}A+) - H_A \times V_{OUT}) \times (1 + (V_{FADE+}) - (V_{FADE-}))/2 + ((V_{IN}B+) - H_B \times V_{OUT}) \times (1 - (V_{FADE+}) + (V_{FADE-}))/2 + (Sum+) - (Sum-))],$$

with $-1 \le (V_{FADE+}) - (V_{FADE-}) \le +1$ numerically.

A_O is the open-loop gain of the amplifier, and is about 600. The large value of A_O drives

$$((V_{IN}A+) - H_A \times V_{OUT}) \times (1 + (V_{FADE+}) - (V_{FADE-}))/2 + ((V_{IN}B+) - H_B \times V_{OUT}) \times (1 - (V_{FADE+}) + (V_{FADE-}))/2 + (Sum+) - (Sum-)) \longrightarrow 0.$$

Rearranging and substituting

$$V_{OUT} = \frac{F \times V_{IN}A + \overline{F} \times V_{IN}B + Sum}{F \times H_A + \overline{F} \times H_B}$$

Where $F = (1 + (V_{FADE+}) - (V_{FADE-}))/2$,
$\overline{F} = (1 - (V_{FADE+}) + (V_{FADE-}))/2$, and
$Sum = (Sum+) - (Sum-)$

In the above equations, F represents the fade amount, with $F = 1$ giving 100% gain on $V_{IN}A$ but 0% for $V_{IN}B$; $F = 0$ giving 0% gain for $V_{IN}A$ but 100% to $V_{IN}B$. $\overline{F}$ is $1 - F$, the complement of the fade gain. When $F = 1$,

$$V_{OUT} = \frac{V_{IN}A + Sum}{H_A}$$

and the amplifier passes $V_{IN}A$ and Sum with a gain of $1/H_A$. Similarly, for $F = 0$

$$V_{OUT} = \frac{V_{IN}B + Sum}{H_B}$$

and the gains vary linearly between fade extremes.

The EL4453C is stable for a direct connection between V_{OUT} and $V_{IN}A-$ or $V_{IN}B-$, yielding a gain of +1. The feedback divider may be used for higher output gain, although with the traditional loss of bandwidth. It is important to keep the feedback dividers' impedances low so that stray capacitance does not diminish the feedback loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 150 MHz; typical strays of 3 pF thus require a feedback impedance of 360Ω or less. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors across equal divider resistors for a gain of two will dominate parasitic effects and allow a higher divider resistance. Either input channel can be set up for inverting gain using traditional feedback resistor connections.

At 100% gain, an input stage operates just like an op-amp's input, and the gain error is very low, around −0.2%. Furthermore, nonlinearities are vastly improved since the gain core sees only small error signals, not full inputs. Unfortunately, distortions increase at lower fade gains for a given input channel.

The Sum pins can be used to inject an additional input signal, but it is not as linear as the V_{IN} paths. The gain error is also not as good as the main inputs, being about 1%. Both sum pins should be grounded if they are not to be used.

Fade-Control Characteristics

The quantity V_{FADE} in the above equations is bounded as $-1 \leq V_{FADE} \leq 1$, even though the externally applied voltages often exceed this range. Actually, the gain transfer function around −1V and +1V is "soft", that is, the gain does not clip abruptly below the 0%-V_{FADE} voltage or above the 100%−V_{FADE} level. An overdrive of 0.3V must be applied to V_{FADE} to obtain truly 0% or 100%. Because the 0% = or 100%-V_{FADE} levels cannot be precisely determined, they are extrapolated from two points measured inside the slope of the gain transfer curve. Generally, an applied V_{FADE} range of −1.5V to +1.5V will assure the full span of numerical $-1 \leq V_{FADE} \leq 1$ and $0 \leq F \leq 1$.

The fade control has a small-signal bandwidth equal to the V_{IN} channel bandwidth, and overload recovery resolves in about 20 ns.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80 nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or about six inches of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high frequency construction obviates any such problems, where the input source is reasonably close to the fader input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between (V−) + 2.5V and (V+) − 2.5V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. The differential signal range is ±2V in the EL4453C. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6 μA maximum DC current, and may be biased anywhere between (V−) +2.5V and (V+) − 3.5V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR and channel-to-channel isolation over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4453C works well on any supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the GND pin are observed (see the Ground Pin section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7 μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01 μF can be used if small load currents flow.

Singe-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V− to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The dissipation of the fader increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2 \times V_S, \max \times V_S + (V_S - V_O) \times V_O / R_{PAR}$$

where I_S, max is the maximum supply current
V_S is the ± supply voltage (assumed equal)
V_O is the output voltage
R_{PAR} is the parallel of all resistors loading the output

Power Supplies — Contd.

For instance, the EL4453C draws a maximum of 21 mA. With light loading, $R_{PAR} \rightarrow \infty$ and the dissipation with $\pm$5V supplies is 210 mW. The maximum supply voltage that the device can run on for a given P_D and the other parameters is

$$V_S, max = (P_D + V_O^2/R_{PAR})/(2I_S + V_O/R_{PAR})$$

The maximum dissipation a package can offer is

$$P_D, max = (T_D, max - T_A, max)/\theta_{JA}$$

where T_D, max is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performace

T_A, max is the ambient temperature, 70°C for commercial and 85°C for industrial range

θ_{JA} is the thermal resistance of the mounted package, obtained from datasheet dissipation curves

The more difficult case is the SO-14 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 70°C, the 80°C temperature rise and package thermal resistance of 110°/W gives a dissipation of 636 mW at 85 °C. This allows $\pm$15V operation over the commercial temperature range, but higher ambient temperature or output loading may require lower supply voltages.

Output Loading

The output stage of the EL4453C is very powerful. It typically can source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain changes only 0.2% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads $<$ 100Ω.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.

EL4453C

Video Fader

General Disclaimer

Specifications contained in this data sheet are in effect as of the publication date shown. Elantec, Inc. reserves the right to make changes in the circuitry or specifications contained herein at any time without notice. Elantec, Inc. assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

élantec

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WARNING — Life Support Policy

Elantec, Inc. products are not authorized for and should not be used within Life Support Systems without the specific written consent of Elantec, Inc. Life Support systems are equipment intended to support or sustain life and whose failure to perform when properly used in accordance with instructions provided can be reasonably expected to result in significant personal injury or death. Users contemplating application of Elantec, Inc. products in Life Support Systems are requested to contact Elantec, Inc. factory headquarters to establish suitable terms & conditions for these applications. Elantec, Inc.'s warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages.

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