EM78F 648/644/642/641N 548/544/542/541N

Flash Series 8-Bit Microcontroller

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial release version	2010/05/05

1 General Description

The EM78F64xN/54xN Series are 8-bit microprocessors designed and developed with low-power, high-speed CMOS technology, and high noise immunity. Each these MUCs is equipped with an on-chip 1/2/4K×13-bit and 8Kx15-bit Electrical Flash Memory, but only the EM78F64xN is embedded with 256 or 128×8-bits in-system programmable EEPROM. Each provides three protection bits to prevent intrusion of user's Flash memory code. Twelve Code option bits are also available to meet user's requirements.

With its enhanced Flash-ROM features, the EM78F64xN/54xN MUCs provide a convenient way of developing and verifying user's programs. Moreover, the Flash-ROM device offers the advantages of easy and effective program updates with development and programming tools. You can take advantage of ELAN's Writer to easily program your development codes.

2 Features

■ **CPU Configuration**

CPU	EM78F648N EM78F548N	EM78F644N EM78F544N	EM78F642N EM78F542N	EM78F641N EM78F541N
ROM	8K * 15 bits	4K * 13 bits	2K * 13 bits	1K * 13 bits
SRAM	304 * 8bits	144 * 8bits	80 * 8bits	48 * 8bits
EEPROM	256 byts (648N only)	256 byts (644N only)	128 byts (642N only)	128 byts (641N only)
STACK	8-LEVEL	8-LEVEL	8-LEVEL	8-LEVEL
LVR	4.2, 3.7, 2.7V	4.0, 3.5, 2.7V	4.0, 3.5, 2.7V	4.0, 3.5, 2.7V
LVD	2.3 / 3.3 / 4.0 / 4.5 V	x	x	x

- In-system programmable EEPROM
  Endurance: 1,000,000 write/erase cycles
- More than 10 years data retention
- Less than 1.5 mA at 5V / 4 MHz
- Typically 20 μA, at 3V / 32kHz
- Typically 1.5 μA, during Sleep mode

■ **I/O Port Configuration**

I/O Port	EM78F648N EM78F548N	EM78F644N EM78F544N	EM78F642N EM78F542N	EM78F641N EM78F541N
I/O	P5, P6, P7, P8, P9	P5, P6, P7, P8	P5, P6, P7, P8	P5, P6, P8
Pull-High	40	14	10	6
Pull-Down	40	14	7	5
Open-drain	40	8	8	6
High Sink	40	x	x	x
High Sink	40	x	x	x

- Wake-up port: P6
- External interrupt with Wake-up: P60

■ **Operating Frequency Range (Base On Two Clocks)**

Operating Frequency	EM78F648N EM78F548N	EM78F644N EM78F544N	EM78F642N EM78F542N	EM78F641N EM78F541N
Crystal Mode ERC Mode IRC Mode	DC~4MHz 2.4 ~ 5.5 V	DC~4MHz 2.2 ~ 5.5 V	DC~4MHz 2.2 ~ 5.5 V	DC~4MHz 2.2 ~ 5.5 V
	DC~8MHz 3 ~ 5.5 V	DC~8MHz 3 ~ 5.5 V	DC~8MHz 3 ~ 5.5 V	DC~8MHz 3 ~ 5.5 V
	DC~20MHz 5 ~ 5.5 V	DC~20MHz 5 ~ 5.5 V	DC~20MHz 5 ~ 5.5 V	DC~20MHz 5 ~ 5.5 V

■ **Available Interrupts**

Interrupt	EM78F648N EM78F548N	EM78F644N EM78F544N	EM78F642N EM78F542N	EM78F641N EM78F541N
Internal	15	10	4	2
External	4	3	3	3

■ **Peripheral Configuration**

Function	EM78F648N EM78F548N	EM78F644N EM78F544N	EM78F642N EM78F542N	EM78F641N EM78F541N
Two channel PWM	10-bits resolution	10-bits resolution	x	x
One 8-bit Timer/counter (TC1)	Timer Counter Capture	Timer Counter Capture	Timer Counter Capture	x
One 16-bit Timer/counter (TC2)	Timer Counter Window	Timer Counter Window	Timer only	x
One 8-bit Timer/counter (TC3)	Timer Counter PWM / PDO	Timer Counter PWM / PDO	Timer Counter PWM / PDO	Timer Counter PWM / PDO
One-set Comparator	10mv offset voltage	10mv offset voltage	5mv offset voltage	5mv offset voltage

- 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
- External interrupt input pin
- 2/4/8/16 clocks per instruction cycle selected by code option
- Power down (Sleep) mode
- High EFT immunity

■ **Operating Voltage Range**

Operating Voltage	EM78F648N EM78F548N	EM78F644N EM78F544N	EM78F642N EM78F542N	EM78F641N EM78F541N
Commercial 0°C~70°C	2.4 ~ 5.5 V	2.2 ~ 5.5 V	2.2 ~ 5.5 V	2.2 ~ 5.5 V
Industrial -40°C~85°C	2.6 ~ 5.5 V	2.4 ~ 5.5 V	2.4 ~ 5.5 V	2.4 ~ 5.5 V

■ **Communciation Peripheral Configuration**

Function	EM78F648N EM78F548N	EM78F644N EM78F544N	EM78F642N EM78F542N	EM78F641N EM78F541N
SPI	Three wire synchronous communication	Three wire synchronous communication	x	x
UART	Two wire Asynchronous communication	Two wire Asynchronous communication	x	x
I2C	7 / 10 bits Address & 8 bits data	x	x	x

■ **Internal RC Drift Rate**

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.2V~5.5V)	Process	Total
4 MHz	±3%	±5%	±2.5%	±10.5%
16 MHz	±3%	±5%	±2.5%	±10.5%
8 MHz	±3%	±5%	±2.5%	±10.5%
*455kHz	±3%	±5%	±2.5%	±10.5%

**NOT applicable to EM78F541N & EM78F641N*

■ **Special Features**

- Programmable free running Watchdog Timer
- Power-on voltage detector available (2.0V ~ 2.1V)

■ **EM78F648N/548N Package Types**

- 44-pin QFP 10x10 mm: EM78Fx48NQ44J/S
- 40-pin DIP 600 mil: EM78Fx48ND40J/S
- 28-pin SKDIP 300 mil: EM78Fx48NK28J/S
- 28-pin SOP 300 mil: EM78Fx48NSO28J/S

■ **EM78F644N/544N Package Types**

- 28-pin SKDIP 300 mil: EM78Fx44NK28J/S
- 28-pin SOP 300 mil: EM78Fx44NSO28J/S
- 24-pin SKDIP 300 mil: EM78Fx44NK24J/S
- 24-pin SOP 300 mil: EM78Fx44NSO24J/S

■ **EM78F642N/542N Package Types**

- 20-pin DIP 300 mil: EM78Fx42ND20J/S
- 20-pin SOP 300 mil: EM78Fx42NSO20J/S
- 20-pin SSOP 209 mil: EM78Fx42NSS20J/S
- 18-pin DIP 300 mil: EM78Fx42ND18J/S
- 18-pin SOP 300 mil: EM78Fx42NSO20J/S

■ **EM78F641N/541N Package Types**

- 16-pin DIP 300 mil: EM78Fx41NAD16J/S
- 16-pin SOP 150 mil: EM78Fx41NASO16J/S
- 10-pin MSOP 118 mil: EM78Fx41NMS10J/S

NOTE

These are Green Products which do not contain hazardous substances.

2.1 Features Selection Guide

Part No.	VDD	Program Memory	Data Memory	I/O	Timer		PWM	UART	SPI	I2C	Package Type
					8-bit	16-bit					
EM78Fx48N	2.4 ~ 5.5 V	8K x 15 bits	304 x 8 bits	40	2	1	2 ch x 10 bits	Two wire synchronous communication	Three wire Asynchronous communication	7 / 10 bits Address & 8 bits data	44 QFP 40 DIP 28 SKDIP/SOP
EM78Fx44N	2.2 ~ 5.5 V	4K x 13 bits	144 x 8 bits	25	2	1	2 ch x 10 bits	Two wire synchronous communication	Three wire Asynchronous communication	x	28 SKDIP/SOP 24 SKDIP/SOP
EM78Fx42N	2.2 ~ 5.5 V	2K x 13 bits	80 x 8 bits	18	2	1	x	x	x	x	20 DIP/SOP 18 DIP/SOP
EM78Fx41N	2.2 ~ 5.5 V	1K x 13 bits	48 x 8 bits	14	1	0	x	x	x	x	16 DIP/SOP 10 MSOP

3 Pin Assignment

3.1 EM78F648N / 548N Pin Assignment

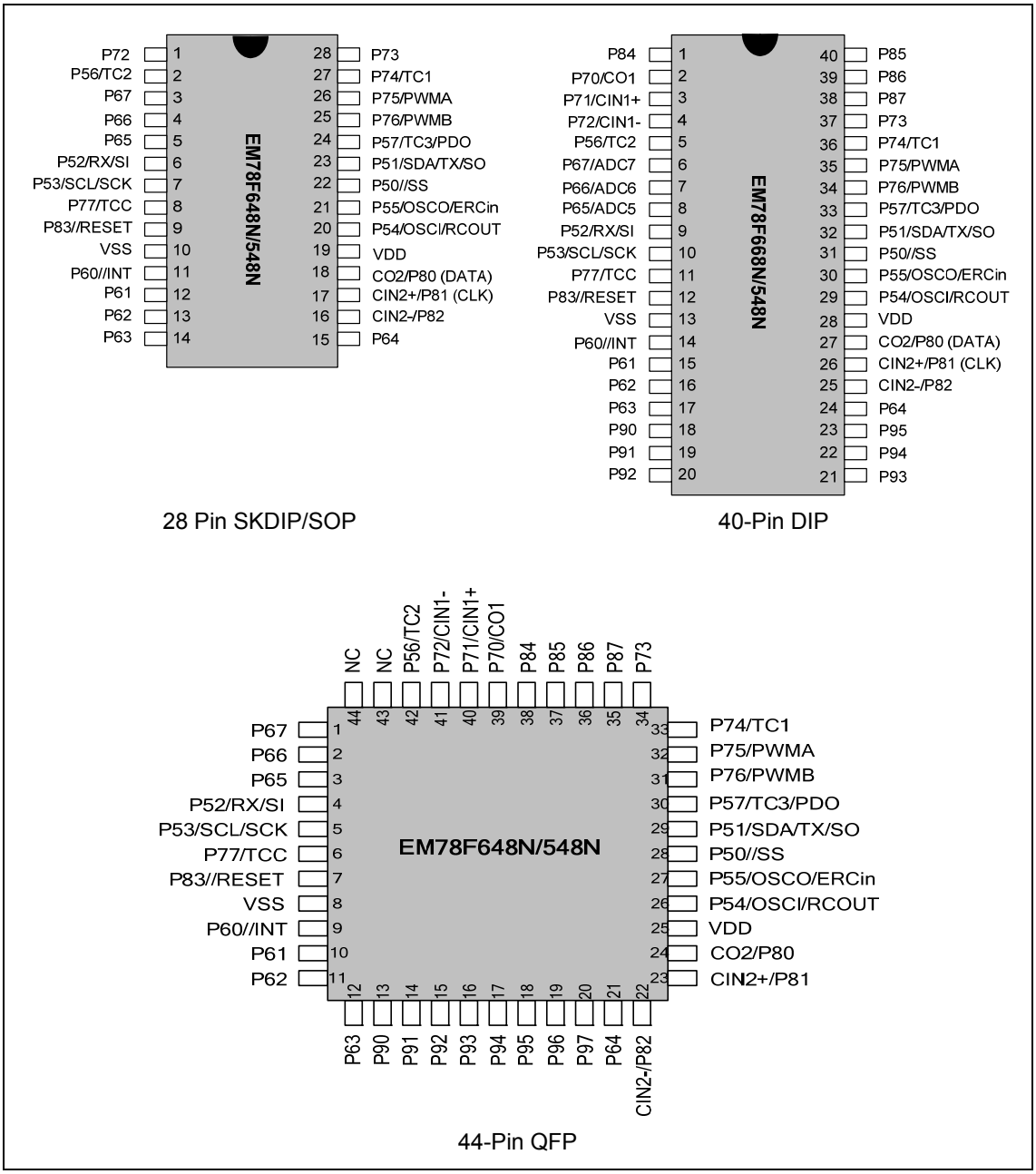


Figure 3-1 EM78F648N / 548N Pin Assignment

3.2 EM78F644N / 544N Pin Assignment

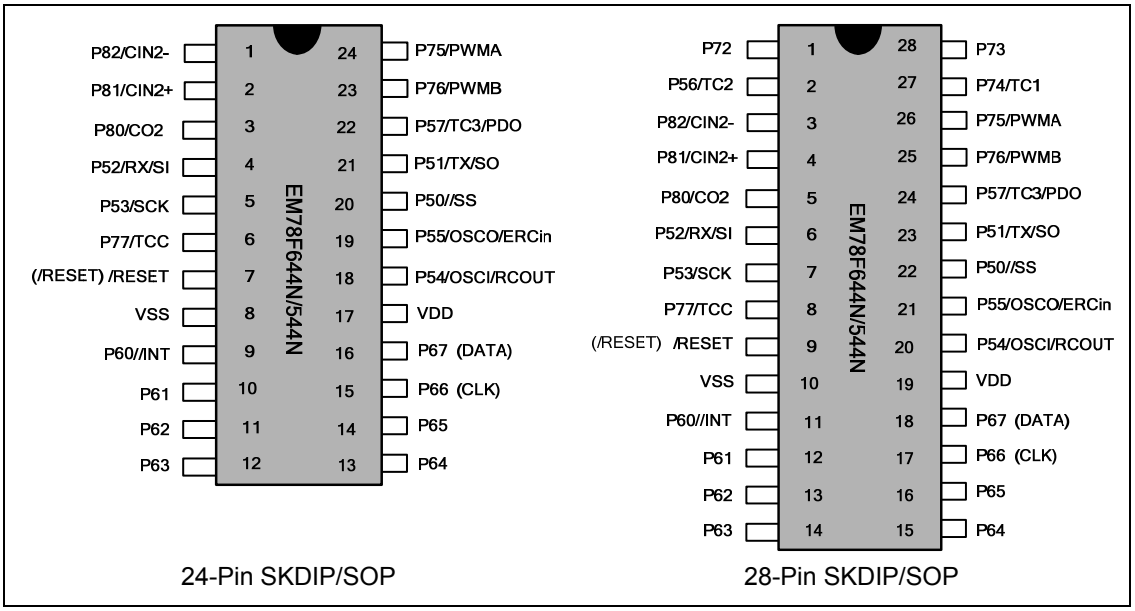


Figure 3-2 EM78F644N / 544N Pin Assignment

3.3 EM78F642N / 542N Pin Assignment

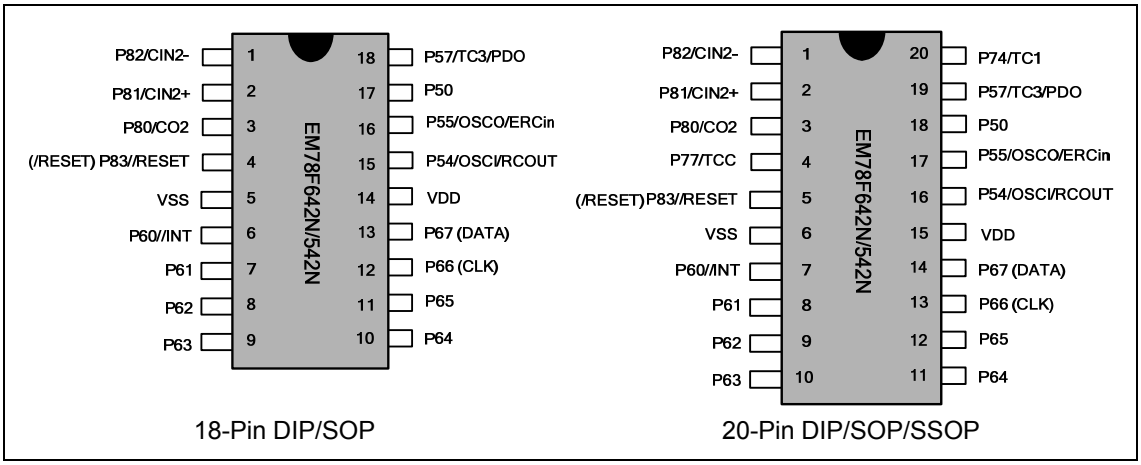


Figure 3-3 EM78F642N / 542N Pin Assignment

3.4 EM78F641N / 541N Pin Assignment

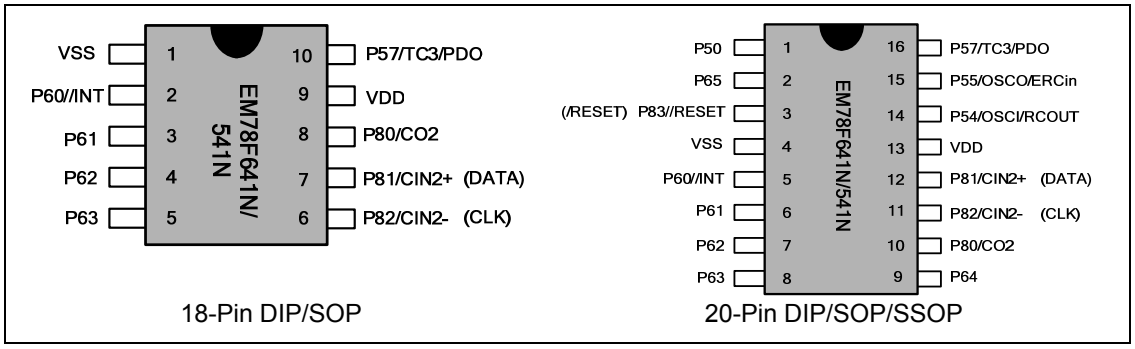


Figure 3-4 EM78F641N / 541N Pin Assignment

4 Pin Description

4.1 EM78F648N / 548N Pin Description

Name	Function	Input Type	Output Type	Description
P50//SS	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	/SS	ST		SPI slave select pin
P51/SDA/TX/SO	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	TX		CMOS	UART TX output
	SO		CMOS	SPI serial data output
	SDA	ST	CMOS	I2C serial data(open-drain)
P52/RX/SI	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	RX	ST		UART RX input
	SI	ST		SPI serial data input
P53/SCK/SCL	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	SCK	ST	CMOS	SPI serial clock input/output
	SCL	ST	CMOS	I2C serial clock (open-drain)

(Continuation)

Name	Function	Input Type	Output Type	Description
P54/OSCI/RCOUT	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	OSCI	XTAL		Clock input of crystal/ resonator oscillator
	RCOUT		CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator(open-drain)
P55/OSCO/ERCin	P55	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	OSCO		XTAL	Clock output of crystal/ resonator oscillator
	ERCin	AN		External RC input pin
P56/TC2	P56	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	TC2	ST		Timer2 clock input
P57/TC3/PDO	P57	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	TC3	ST		Timer3 clock input
	PDO		CMOS	Programmable divider output
P60//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink, high drive and pin change wakeup.
	/INT	ST		external interrupt pin
P61~P67	P61~P67	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink, high drive and pin change wakeup.
P70/CO1	P70	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	CO1		CMOS	Output of comparator1
P71/CIN1+	P71	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	CIN1+	AN		Non-inverting end of comparator1
P72/CIN1-	P72	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	CIN1-	AN		Inverting end of comparator1
P73	P73	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
P74/TC1	P74	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	TC1		CMOS	Timer1 clock input
P75/PWMA	P75	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	PWMA		CMOS	PWMA output
P76/PWMB	P76	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	PWMB		CMOS	PWMB output

(Continuation)

Name	Function	Input Type	Output Type	Description
P77/TCC	P77	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	TCC	ST		Real Time Clock/Counter clock input
P80/CO2	P80	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	CO2		CMOS	Output of comparator2
(DATA)	**(DATA)**	ST	CMOS	DATA pin for Writer programming
P81/CIN2+	P81	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	CIN2+	AN		Non-inverting end of comparator2
(CLK)	**(CLK)**	ST		CLOCK pin for Writer programming
P82/CIN2-	P82	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	CIN2-	AN		Inverting end of Comparator 2
P83/RESET	P83	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
	/RESET	ST		Internal pull-high reset pin
(/RESET)	**(/RESET)**	ST		/RESET pin for Writer programming
P84~P87	P84~P87	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
P90~P97	P90~P97	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high, high sink and high drive.
VDD	VDD	power		Power
VSS	VSS	power		Ground

Legend: ST: *Schmitt Trigger input*, **AN:** *analog pin*, **CMOS:** *CMOS output*,
XTAL: *oscillation pin for crystal/ resonator*

4.2 EM78F644N / 544N Pin Description

Name	Function	Input Type	Output Type	Description
P50//SS	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down
	/SS	ST		SPI slave select pin
P51/TX/SO	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down
	TX		CMOS	UART TX output
	SO		CMOS	SPI serial data output
P52/RX/SI	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down
	RX	ST		UART RX input
	SI	ST		SPI serial data input
P53/SCK	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down
	SCK	ST	CMOS	SPI serial clock input/output
P54/OSCI/RCOUT	P54	ST	CMOS	Bidirectional I/O pin
	OSCI	XTAL		Clock input of crystal/ resonator oscillator
	RCOUT		CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator(open-drain)
P55/OSCO/ERCin	P55	ST	CMOS	Bidirectional I/O pin
	OSCO		XTAL	Clock output of crystal/ resonator oscillator
	ERCin	AN		External RC input pin
P56/TC2	P56	ST	CMOS	Bidirectional I/O pin
	TC2	ST		Timer2 clock input
P57/TC3/PDO	P57	ST	CMOS	Bidirectional I/O pin
	TC3	ST		Timer3 clock input
	PDO		CMOS	Programmable divider output
P60//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open drain, pull-high and pin change wakeup.
	/INT	ST		External interrupt pin
P61~P63	P61~P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open drain, pull-high and pin change wakeup.
P64~P65	P64~P65	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pin change wakeup.
P66	P66	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pin change wakeup.
(CLK)	**(CLK)**	ST		CLOCK pin for Writer programming
P67	P67	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pin change wakeup.
(DATA)	**(DATA)**	ST	CMOS	DATA pin for Writer programming

(Continuation)

Name	Function	Input Type	Output Type	Description
P72 ~ P73	P72~P73	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pull-high.
P74/TC1	P74	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pull-high.
	TC1		CMOS	Timer1 clock input
P75/PWMA	P75	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pull-high.
	PWMA		CMOS	PWMA output
P76/PWMB	P76	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pull-high.
	PWMB		CMOS	PWMB output
P77/TCC	P77	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pull-high.
	TCC	ST		Real Time Clock/Counter clock input
P80/CO2	P80	ST	CMOS	Bidirectional I/O pin
	CO2		CMOS	Bidirectional I/O pin with programmable pull-down and pull-high.
P81/CIN2+	P81	ST	CMOS	Bidirectional I/O pin
	CIN2+	AN		Non-Inverting end of Comparator 2
P82/CIN2-	P82	ST	CMOS	Bidirectional I/O pin
	CIN2-	AN		Inverting end of comparator2
/RESET	/RESET	ST		Internal pull-high reset pin
(/RESET)	**(/RESET)**	ST		/RESET pin for Writer programming
VDD	VDD	power		Power
VSS	VSS	power		Ground

Legend: ST: *Schmitt Trigger input*, **AN:** *analog pin*, **CMOS:** *CMOS output*,
XTAL: *oscillation pin for crystal/ resonator*

4.3 EM78F642N / 542N Pin Description

Name	Function	Input Type	Output Type	Description
P50	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down
P54/OSCI/RCOUT	P54	ST	CMOS	Bidirectional I/O pin
	OSCI	XTAL		Clock input of crystal/ resonator oscillator
	RCOUT		CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator(open-drain)
P55/OSCO/ERCin	P55	ST	CMOS	Bidirectional I/O pin
	OSCO		XTAL	Clock output of crystal/ resonator oscillator
	ERCin	AN		External RC input pin
P57/TC3/PDO	P57	ST	CMOS	Bidirectional I/O pin
	TC3	ST		Timer3 clock input
	PDO		CMOS	Programmable divider output
P60//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wakeup.
	/INT	ST		External interrupt pin
P61~P63	P61~P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wakeup.
P64~P65	P64~P65	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pinchange wakeup.
P66	P66	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pinchange wakeup.
(CLK)	**(CLK)**	ST		CLOCK pin for Writer programming
P67	P67	ST	CMOS	Bidirectional I/O pin with programmable open-drain and pull-high.
(DATA)	**(DATA)**	ST	CMOS	DATA pin for Writer programming
P74/TC1	P74	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pull-high.
	TC1		CMOS	Timer1 clock input
P77/TCC	P77	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pull-high.
	TCC	ST		Real Time Clock/Counter clock input
P80/CO2	P80	ST	CMOS	Bidirectional I/O pin
	CO2		CMOS	Output of comparator2
P81/CIN2+	P81	ST	CMOS	Bidirectional I/O pin
	CIN2+	AN		Non-inverting end of comparator2
P82/CIN2-	P82	ST	CMOS	Bidirectional I/O pin
	CIN2-	AN		Inverting end of Comparator 2

(Continuation)

Name	Function	Input Type	Output Type	Description
P83/RESET	P83	ST	CMOS	Bidirectional I/O pin
	/RESET	ST		Internal pull-high reset pin
(/RESET)	**(/RESET)**	ST		/RESET pin for Writer programming
VDD	VDD	power		Power
VSS	VSS	power		Ground

Legend: ST: *Schmitt Trigger input*, **AN:** *analog pin*, **CMOS:** *CMOS output*,
XTAL: *oscillation pin for crystal/ resonator*

4.4 EM78F641N / 541N Pin Description

Name	Function	Input Type	Output Type	Description
P50	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down
P54/OSCI/RCOUT	P54	ST	CMOS	Bidirectional I/O pin
	OSCI	XTAL		Clock input of crystal/ resonator oscillator
	RCOUT		CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator(open-drain)
P55/OSCO/ERCin	P55	ST	CMOS	Bidirectional I/O pin
	OSCO		XTAL	Clock output of crystal/ resonator oscillator
	ERCin	AN		External RC input pin
P57/TC3/PDO	P57	ST	CMOS	Bidirectional I/O pin
	TC3	ST		Timer3 clock input
	PDO		CMOS	Programmable divider output
P60//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wakeup.
	/INT	ST		External interrupt pin
P61~P63	P61~P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wakeup.
P64~P65	P64~P65	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pin change wakeup.
P80/CO2	P80	ST	CMOS	Bidirectional I/O pin
	CO2		CMOS	Output of comparator2
P81/CIN2+	P81	ST	CMOS	Bidirectional I/O pin
	CIN2+	AN		Non-inverting end of comparator2
(DATA)	**(DATA)**	ST	CMOS	DATA pin for Writer programming

(Continuation)

Name	Function	Input Type	Output Type	Description
P82/CIN2-	P82	ST	CMOS	Bidirectional I/O pin
	CIN2-	AN		Inverting end of comparator2
(CLK)	**(CLK)**	ST		CLOCK pin for Writer programming
P83/RESET	P83	ST	CMOS	Bidirectional I/O pin
	/RESET	ST		Internal pull-high reset pin
(/RESET)	**(/RESET)**	ST		/RESET pin for Writer programming
VDD	VDD	power		Power
VSS	VSS	power		Ground

Legend: ST: *Schmitt Trigger input*, **AN:** *analog pin*, **CMOS:** *CMOS output*,
XTAL: *oscillation pin for crystal/ resonator*

5 Block Diagram

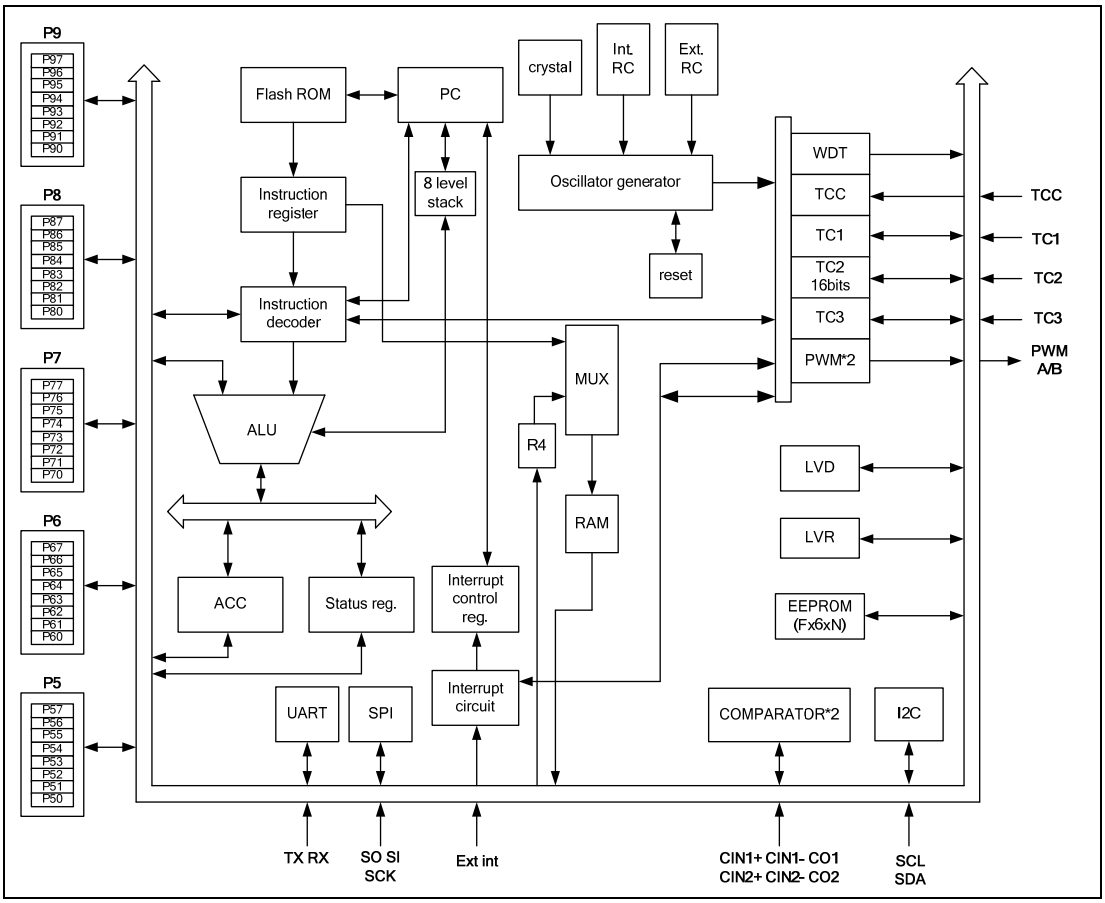


Figure 5-1 Functional Block Diagram

6 Functional Description

6.1 Operational Registers for EM78F64xN/54xN

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction that uses R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock/Counter)

R1 is incremented by an external signal edge, which is defined by the TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock. It is writable and readable as any other registers. It is defined by resetting PSTE (CONT-3).

The prescaler is assigned to TCC, if the PSTE bit (CONT-3) is reset. The content of the prescaler counter is cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter and Stack)

- Depending on the device type, R2 and hardware stack are 12-bit wide. The structure is depicted in Figure 6-1a below.
- The configuration structure generates 4K×13 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all "**0**"s when under a reset condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the program counter bits (A0~A11). Therefore, "LJMP" allows the PC to jump to any location within 4K (2^{12}).
- "LCALL" instruction loads the program counter bits (A0 ~A11), and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 4K (2^{12})
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.

- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows loading an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC remain unchanged.
- Any instruction except “ADD R2, A” that is written to R2 (e.g., "MOV R2, A", "BC R2, 6") will cause the ninth bit and the tenth bit (A8~A9) of the PC to remain unchanged.
- All instructions are single instruction cycle (fclk/2, fclk/4, fclk/8 or fclk/16) except for instructions that would change the contents of R2 and “LCALL”, “LJMP”, “TBRD” instructions. The “LCALL”, “LJMP” and “TBRD” instructions need two instructions cycle.

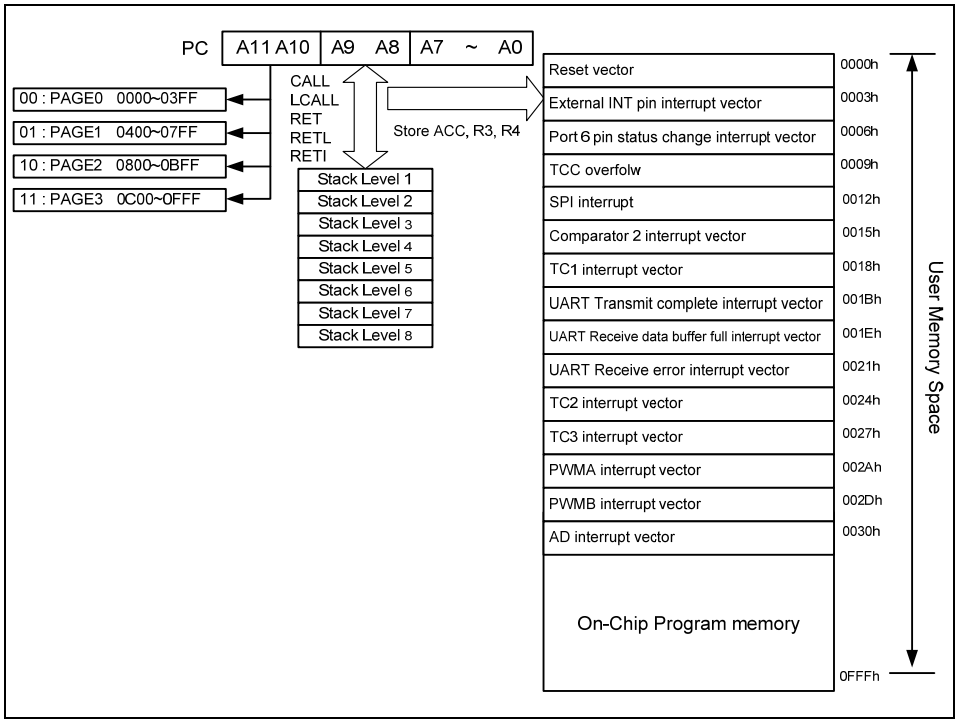


Figure 6-1 Program Counter Organization

■ Data Memory Configuration

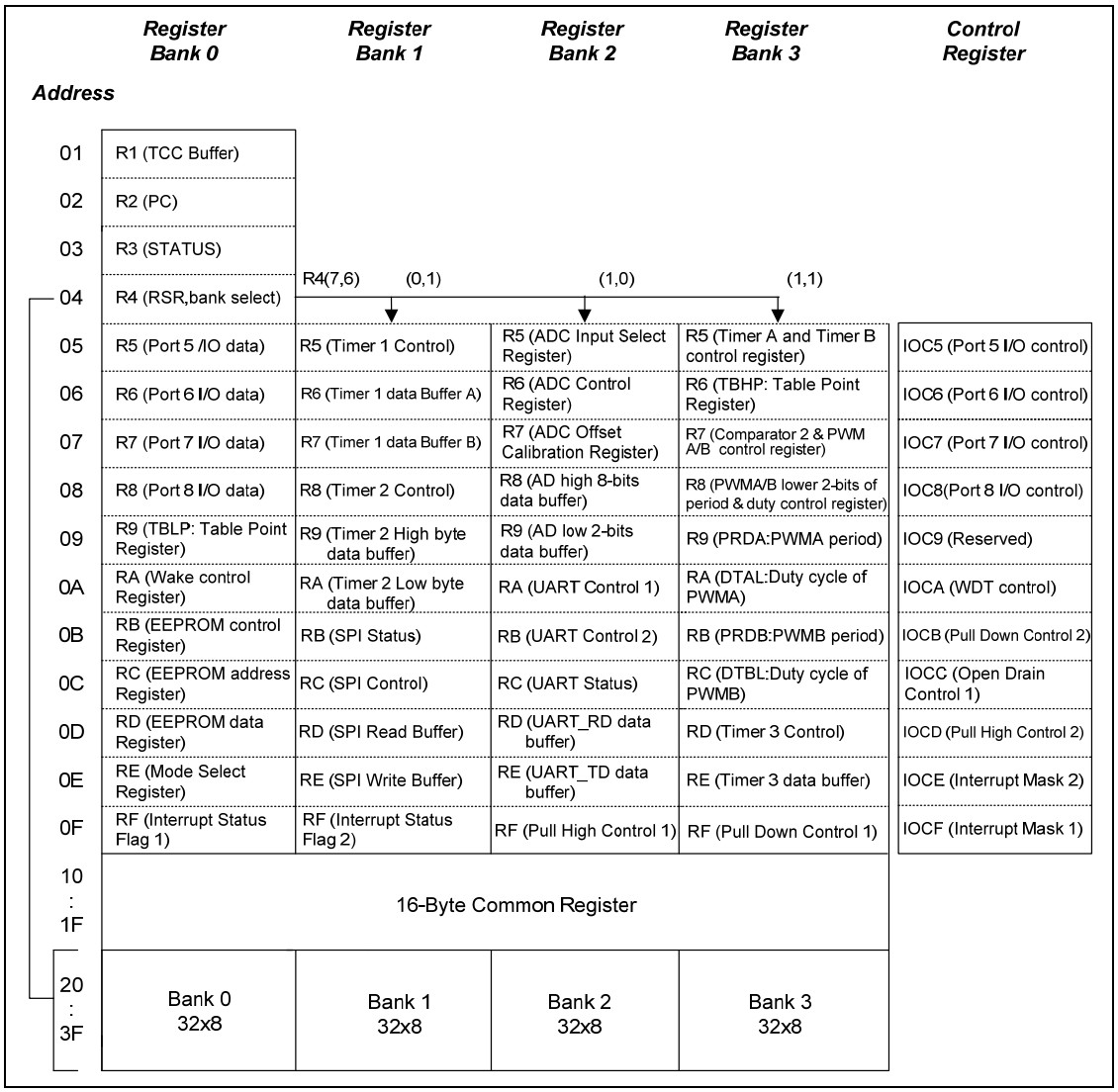


Figure 6-1b Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	T	P	Z	DC	C

Bits 7 ~ 5: Not used, set to "**0**" all the time.

Bit 4 (T): Time-out bit

Set to "**1**" with the "SLEP" and "WDTC" commands, or during power up and reset to "**0**" by WDT time-out.

Bit 3 (P): Power down bit

Set to "**1**" during power-on or by a "WDTC" command and reset to "**0**" by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bits 7 ~ 6: Used to select Bank 0 ~ Bank 3

NOTE

- *For F642/542N, Bit 7 is unused. Set to "**0**" all the time.*
- *For F641/541N, Bit 7 ~ Bit 6 are unused. Set to "**0**" all the time.*

Bits 5 ~ 0: Used to select registers (Address: 00~3F) in indirect addressing mode.

See the data Memory Configuration in Figure 6-1b above.

6.1.6 Bank 0 R5 (PORT5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	P53	P52	P51	P50

Bit 7 ~ 0 (P57 ~ P50): 8-bit Port5 I/O data register

NOTE

- *For F642/542N, Bit 6, Bit 3 ~ Bit 1 are unused. Set to "**0**" all the time.*
- *For F641/541N, Bit 6, Bit 3 ~ Bit 1 are unused. Set to "**0**" all the time.*

You can use IOC5 register to define each bit as input or output.

6.1.7 Bank 0 R6 (PORT6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

Bit 7 ~ 0 (P67 ~ P60): 8-bit Port6 I/O data register

NOTE

*For F641/541N, Bit 7 & Bit 6 are unused. Set to "**0**" all the time.*

You can use IOC6 register to define each bit as input or output.

6.1.8 Bank 0 R7 (PORT7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	-	-

Bits 7 ~ 2 (P77 ~ P72): 6-bit Port7 I/O data register

Bits 1 ~ 0: Not used, set to "**0**" all the time.

NOTE

- *For F642/542N, Bit 6 & Bit 5, Bit 3 ~ Bit 0 are unused. Set to "**0**" all the time.*
- *For F641/541N, Bit 7 ~ Bit 0 are unused. Set to "**0**" all the time.*

User can use IOC7 register to define each bit as input or output.

6.1.9 Bank 0 R8 (PORT8)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	P83	P82	P81	P80

Bit 3 ~ 0 (P83 ~ P80): 4-bit Port8 I/O data register

NOTE

*For F644/544N, Bit 3 is unused. Set to "**0**" all the time.*

User can use IOC8 register to define each bit as input or output.

6.1.10 Bank 0 R9 (TBLP: Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0

Bits 7 ~ 0: This is the least 8 significant bits of address for program code.

NOTE

- *Bank 0 R9 overflow will carry to Bank 3 R6.*
- *Bank 0 R9 underflow will borrow from Bank 3 R6.*

6.1.11 Bank 0 RA (Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2WE	ICWE	-	EXWE	SPIWE	-	-	-

Bit 7 (CMP2WE): Comparator 2 wake-up enable bit

0: Disable Comparator 2 Wake-up

1: Enable Comparator 2 Wake-up

When the Comparator 2 Output Status Change is used to enter an interrupt vector or to Wake-up the IC from Sleep, the CMP2WE bit must be set to "Enable".

Bit 6 (ICWE): Port 6 input status change wake-up enable bit

0: Disable Port 6 input status change Wake-up

1: Enable Port 6 input status change Wake-up

Bit 5: Not used, set to "**0**" all the time

Bit 4 (EXWE): External /INT wake-up enable bit

0: Disable External /INT pin Wake-up

1: Enable External /INT pin Wake-up

Bit 3 (SPIWE): SPI Wake-up enable bit when SPI acts as Slave device

0: Disable SPI Wake-up when SPI acts as Slave device

1: Enable SPI Wake-up when SPI acts as Slave device

NOTE

- *F642/542N, Bit 3 is unused. Set to "**0**" all the time.*
- *For F641/541N, Bit 3 is unused. Set to "**0**" all the time.*

Bits 2 ~ 0: Not used, set to "**0**" all the time.

6.1.12 Bank 0 RB (EEPROM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7 (RD): Read control register

0: Disable EEPROM read execution

1: Read EEPROM contents (RD can be set by software. RD is cleared by hardware after Read instruction is completed).

Bit 6 (WR): Write control register

0: Write cycle to the EEPROM is completed.

1: Initiate a write cycle (WR can be set by software. WR is cleared by hardware after Write cycle is completed).

Bit 5 (EEWE): EEPROM Write Enable bit

0: Prohibit write to the EEPROM

1: Allows EEPROM write cycles

Bit 4 (EEDF): EEPROM Detect Flag

0: Write cycle is completed

1: Write cycle is unfinished

Bit 3 (EEPC): EEPROM power-down control bit

0: Switch OFF the EEPROM

1: Switch ON the EEPROM

Bits 2 ~ 0: Not used, set to "**0**" all the time.

NOTE

EM78F548/544/542/541N series ICs do NOT support EEPROM function. Therefore, the corresponding control registers (Bank0 RB~RD) are reserved.

6.1.13 Bank 0 RC (256 Bytes EEPROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_A7	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bits 7 ~ 0: 256 bytes EEPROM address

NOTE

- *EM78F548/544/542/541N series ICs do NOT support EEPROM function. Therefore, the corresponding control registers (Bank0 RB~RD) are reserved.*
- *For F642/542N, Bit 7 is unused. Set to "**0**" all the time*
- *For F641/541N, Bit 7 is unused. Set to "**0**" all the time.*

6.1.14 Bank 0 RD (256 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: 256 bytes EEPROM data

NOTE

EM78F548/544/542/541N series ICs do NOT support EEPROM function. Therefore, the corresponding control registers (Bank0 RB~RD) are reserved.

6.1.15 Bank 0 RE (Mode Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	-	-	-	-

Bit 7: Not used, set to "**0**" all the time

Bit 6 (TIMERSC): TCC, TC1, TC2, TC3, Timer A, & Timer B clock source select

0: Fs is used as Fc

1: Fm is used as Fc

Bit 5 (CPUS): CPU Oscillator Source Select.

0: Fs**:** Sub frequency for WDT internal RC time base

1: Fm**:** Main-oscillator clock

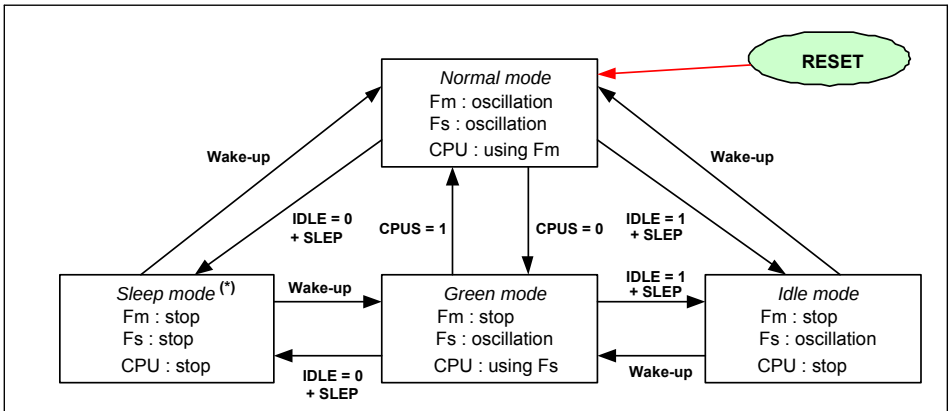
When CPUS=0, the CPU oscillator selects the Sub-oscillator and the Main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit.

0: IDLE="0" + SLEP instruction → Sleep mode

1: IDLE="1" + SLEP instruction → Idle mode

■ **CPU Operation Mode**



Note: * *only when WDT IRC is Fs.*

If the watchdog function is enabled before going into sleep mode, Fs does not stop. Hence, some circuits like timer/counter (of which clock source is Fs) must be disabled before going into sleep mode, especially when the corresponding interrupt is enabled.

Figure 6-2 CPU Operation Mode Block Diagram

Oscillator (Normal Mode Source)	CPU Mode Status	Oscillator Stable Time (S)[1]	Count from Normal/Green (CLK)[2]
Crystal ; 1M ~ 16 MHz	Sleep/Idle → Normal	0.5 ms ~ 2 ms	254 CLK
	Green → Normal		254 CLK
	Sleep/Idle → Green	< 100 µs	32 CLK
ERC ; 3.5 MHz	Sleep/Idle → Normal	< 5 µs	32 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	
IRC ; 455K, 4M, 8M, 16 MHz	Sleep/Idle → Normal	< 2 µs	32 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	

[1] *The oscillator stable time depends on the oscillator characteristics*

[2] *After the oscillator has stabilized, the CPU will count 254/32 CLK in Normal/Green mode and continue to work in Normal/Green mode.*

Ex 1: *The 4 MHz IRC Wakes-up from Sleep mode to Normal mode. The total Wake-up time is 2 µs + 32 CLK @ 4 MHz*

Ex 2: *The 4 MHz IRC Wakes-up from Sleep mode to Green mode. The total wake-up time is 100 µs + 32 CLK @ 16kHz*

Bits 3 ~ 0: Not used, set to "**0**" all the time.

6.1.16 Bank 0 RF (Interrupt Status Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	SPIIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF

NOTE: *Set to "**1**" to enable Interrupt Request, "**0**" to disable interrupt execution.*

Bits 7 ~ 6: Not used, set to "**0**" all the time.

Bit 5 (SPIIF): SPI mode Interrupt flag. Flag is cleared by software.

Bit 4 (PWMBIF): PWMB (Pulse Width Modulation) Interrupt flag
Set when a selected period is reached. Reset by software.

Bit 3 (PWMAIF): PWMA (Pulse Width Modulation) interrupt flag.
Set when a selected period is reached. Reset by software.

NOTE

- *For F642/542N, Bit 5 ~ Bit 3 are unused. Set to "**0**" all the time.*
- *For F641/541N, Bit 5 ~ Bit 3 are unused. Set to "**0**" all the time*

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

NOTE

- *RF can be cleared by instruction but cannot be set.*
- *IOCF is the interrupt mask register.*
- *The result of reading RF is the "logic AND" of RF and IOCF.*

6.1.17 R10 ~ R3F

These are all 8-bit general-purpose registers.

6.1.18 Bank 1 R5 TC1CR (Timer 1 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1CAP	TC1S	TC1CK1	TC1CK0	TC1M	TC1ES	-	-

NOTE

For F641/541N, this register is reserved.

Bit 7 (TC1CAP): Software capture control

0: Disable software capture

1: Enable software capture

Bit 6 (TC1S): Timer/Counter 1 start control

0: Stop and clear counter

1: Start Timer/Counter 1

Bit 5~Bit 4 (TC1CK1~TC1CK0): Timer/Counter 1 clock source selection

TC1CK1	TC1CK0	Clock Source	Resolution (4 MHz)	Max. Time (4 MHz)	Resolution (16kHz)	Max. Time (16kHz)
		Normal, Idle	Fc=4M	Fc=4M	Fc=16K	Fc=16K
0	0	$Fc/2^{12}$	1024 µs	262144 µs	256 ms	65536 ms
0	1	$Fc/2^{10}$	256 µs	65536 µs	64 ms	16384 ms
1	0	$Fc/2^{7}$	32 µs	8192 µs	8 ms	2048 ms
1	1	External clock (TC1 pin)	-	-	-	-

Bit 3 (TC1M): Timer/Counter 1 mode select

0: Timer/Counter 1 mode

1: Capture mode

Bit 2 (TC1ES): TC1 signal edge

0: Increment if the transition from low to high (rising edge) takes place on the TC1 pin.

1: Increment if the transition from high to low (falling edge) takes place on TC1 pin.

Bits 1 ~ 0: Not used, set to "**0**" all the time.

■ **Timer/Counter 1 Configuration**

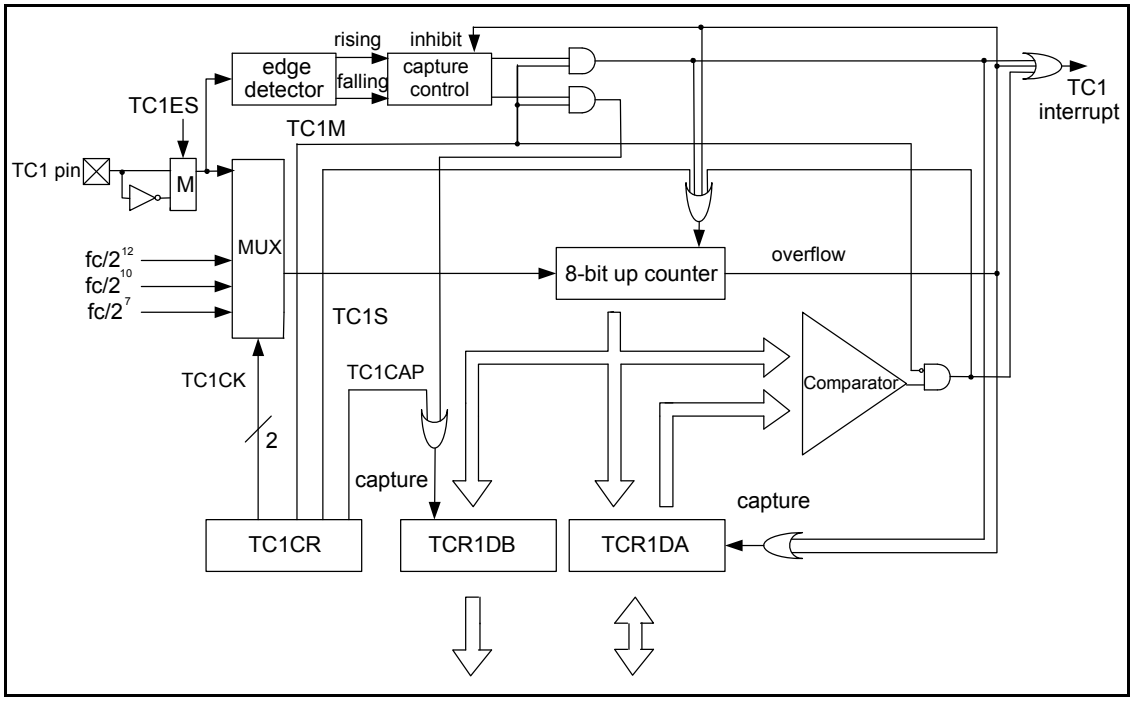


Figure 6-3a Timer/Counter 1 Configuration Block Diagram

In Timer mode, counting up is performed using the internal clock. When the contents of the up-counter matched with the TCR1DA, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TCR1DB by setting TC1CAP to "**1**" and the TC1CAP is automatically cleared to "**0**" after capture is completed.

In Counter mode, counting up is performed using the external clock input pin (TC1 pin) and either rising or falling edge can be selected by TC1ES, **but both edges cannot be used**. When the contents of the up-counter matched with the TCR1DA, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into the TCR1DB by setting TC1CAP to "**1**" and the TC1CAP is automatically cleared to "**0**" after capture is completed.

In Capture mode, the pulse width, period and duty of the TC1 input pin are measured under this mode to decode the remote control signal. The counter is set as free running by the internal clock. On a rising (falling) edge of TC1 pin input, the contents of the counter is loaded into TCR1DA, then the counter is cleared and interrupt is generated. On a falling (rising) edge of the TC1 pin input, the contents of the counter are loaded into TCR1DB. At the next rising edge of the TC1 pin input while the counter is still counting, the contents of the counter are loaded into TCR1DA. Then, the counter is cleared and interrupt is generated again. If an overflow occurs before an edge is detected, the FFH is loaded into TCR1DA and the overflow interrupt is generated. During interrupt processing, you can determine whether an overflow has occurred by checking the TCR1DA value is FFH. After an interrupt (capture to TCR1DA or overflow detection) is generated, capture and overflow detection are halted until TCR1DA is read out.

■ **Capture Mode Timing**

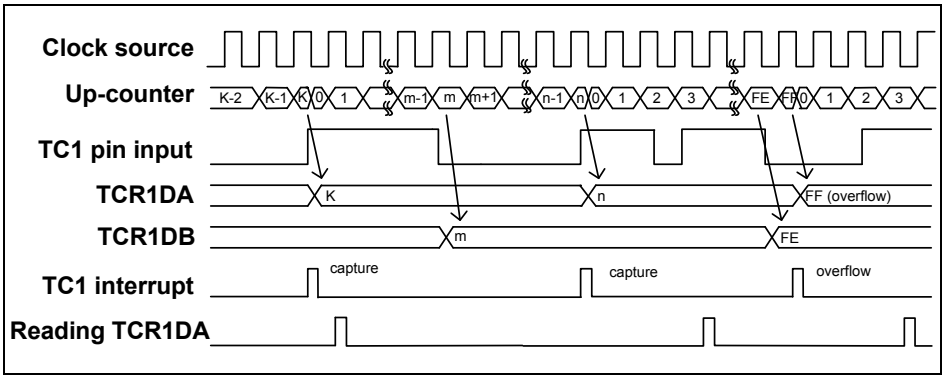


Figure 6-3b Capture Mode Timing Diagram

6.1.19 Bank 1 R6 TCR1DA (Timer 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR1DA7	TCR1DA6	TCR1DA5	TCR1DA4	TCR1DA3	TCR1DA2	TCR1DA1	TCR1DA0

Bit 7 ~ Bit 0 (TCR1DA7 ~ TCR1DA0): Data buffer of 8-bit Timer/Counter 1.

NOTE
For F641/541N, this register is reserved.

6.1.20 Bank 1 R7 TCR1DB (Timer 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR1DB7	TCR1DB6	TCR1DB5	TCR1DB4	TCR1DB3	TCR1DB2	TCR1DB1	TCR1DB0

Bit 7 ~ Bit 0 (TCR1DB7 ~ TCR1DB0): Data buffer of 8-bit Timer/Counter 1.

NOTE
For F641/541N, this register is reserved.

6.1.21 Bank 1 R8 TC2CR (Timer 2 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCM1	RCM0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0

Bits 7 ~ 6 (RCM1 ~ RCM0): IRC mode selection bits. The Bank 1 R8<7,6> is enabled when Word 1<12> COBS0 = "**1**".

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	0	0	4 MHz ± 2.5%	2.2V ~ 5.5V	< 5 µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	1	1	455kHz ± 10%	2.2V ~ 5.5V	< 50 µs
16 MHz	0	0	4 MHz ± 10%	2.2V ~ 5.5V	< 6 µs
	0	1	16 MHz ± 2.5%	4.5V ~ 5.5V	< 1.25 µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	1	1	455kHz ± 10%	2.2V ~ 5.5V	< 50 µs
8 MHz	0	0	4 MHz ± 10%	2.2V ~ 5.5V	< 6 µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	1	0	8 MHz ± 2.5%	3.0V ~ 5.5V	< 2.5 µs
	1	1	455kHz ± 10%	2.2V ~ 5.5V	< 50 µs
455kHz	0	0	4 MHz ± 10%	2.2V ~ 5.5V	< 6 µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	1	1	455kHz ± 2.5%	2.2V ~ 5.5V	< 45 µs

NOTE

- *The initial values of Bank 1 R8<7,6> will be kept the same as Word 1<3,2>.*
- *If the IRC frequency is changed from A-frequency to B-frequency, the MCU needs to wait for some time for it to work. The waiting time corresponds to the B-frequency.*

Example:

1st Step When user selects the 4 MHz at the Writer, the initial values of Bank 1 R8<7,6> would be "00", the same as the value of Word 1<3,2>. If the MCU is free-running, it will work at 4 MHz ± 2.5%. Refer to the table below.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**0**	**0**	**4 MHz ± 2.5%**	2.2V ~ 5.5V	< 5 µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	1	1	455kHz ± 10%	2.2V ~ 5.5V	< 50 µs

2nd Step If it is desired to set Bank 1 R8<7,6> = "01" while the MCU is working at 4 MHz ± 2.5%, the MCU needs to hold for 1.5 μs, then it will continue to work at 16 MHz ± 10%.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	0	0	4 MHz ± 2.5%	2.2V ~ 5.5V	< 5 μs
	0	**1**	**16 MHz ± 10%**	4.5V ~ 5.5V	< 1.5 μs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs
	1	1	455kHz ± 10%	2.2V ~ 5.5V	< 50 μs

3rd Step If it is desired to set Bank 1 R8<7,6> = "11" while the MCU is working at 16 MHz ± 10%, the MCU needs to hold for 50 μs, then it will continue to work at 455kHz ± 10%.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	0	0	4 MHz ± 2.5%	2.2V ~ 5.5V	< 5 μs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 μs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs
	1	**1**	**455kHz ± 10%**	2.2V ~ 5.5V	< 50 μs

4th Step If it is desired to set Bank 1 R8<7,6> = "00" while the MCU is working at 455kHz ± 10%, the MCU needs to hold for 5 μs, then it will continue to work at 4 MHz ± 2.5%.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**0**	**0**	**4 MHz ± 2.5%**	2.2V ~ 5.5V	< 5 μs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 μs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs
	1	1	455kHz ± 10%	2.2V ~ 5.5V	< 50 μs

Bit 5 (TC2ES TC2 signal edge

0: Increment if a transition from low to high (rising edge) takes place on the TC2 pin.

1: increment if a transition from high to low (falling edge) takes place on the TC2 pin.

Bit 4 (TC2M): Timer/Counter 2 mode select

0: Timer/counter mode

1: Window mode

NOTE

*For F642/542N, Bit 5 ~ Bit 4 are unused. Set to "**0**" all the time.*

Bit 3 (TC2S): Timer/Counter 2 start control

0: Stop and clear the counter

1: Start Timer/Counter 2

Bit 2~Bit 0 (TC2CK2~TC2CK0): Timer/Counter 2 clock source select

TC2CK2	TC2CK1	TC2CK0	Clock Source	Resolution	Max. Time	Resolution	Max. Time
			Normal, Idle	Fc=4M	Fc=4M	Fc=16K	Fc=16K
0	0	0	$Fc/2^{23}$	2.1 sec	38.2 hr	524.3 s	9544 hr
0	0	1	$Fc/2^{13}$	2.048 ms	134.22 sec	512 ms	33554.432 s
0	1	0	$Fc/2^{8}$	64 μs	4.194 sec	16 ms	1048.576 s
0	1	1	$Fc/2^{3}$	2 μs	131.072 ms	0.5 ms	32768 ms
1	0	0	Fc	250 ns	16.384 ms	0.0625 ms	4096 ms
1	0	1	–	–	–	–	–
1	1	0	–	–	–	–	–
1	1	1	External clock (TC2 pin)	–	–	–	–

NOTE

*For F641/541N, Bit 7 ~ Bit 6 can't set as "11" Bit 5 ~ Bit 0 are unused. Set to "**0**" all the time.*

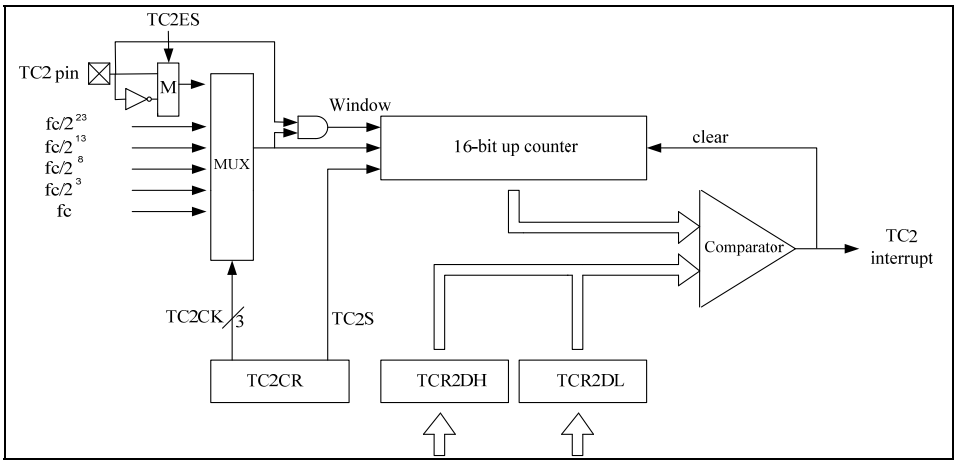


Figure 6-4a Timer/Counter 2 Configuration Block Diagram

In Timer mode, counting up is performed using internal clock. When the contents of the up-counter match the TCR2 (TCR2DH+TCR2DL), the interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared.

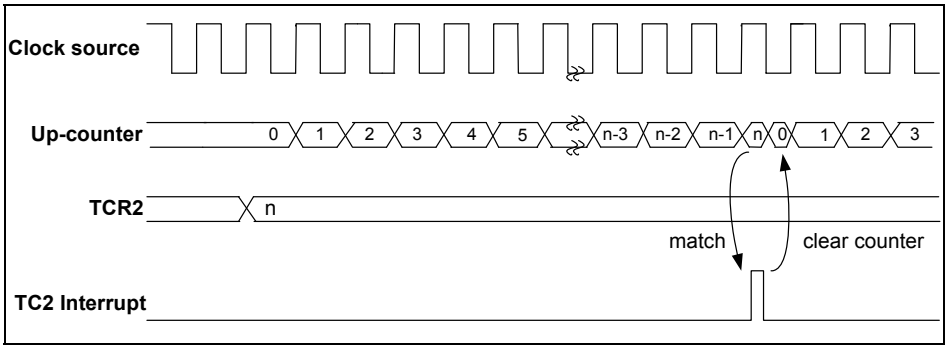


Figure 6-4b Timer Mode Timing Diagram

In Counter mode, counting up is performed using external clock input pin (TC2) and either rising or falling can be selected by setting TC2ES. When the contents of the up-counter match the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

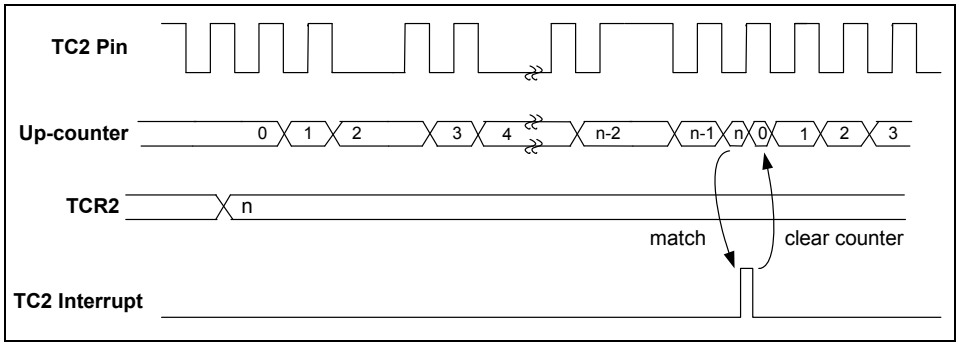


Figure 6-4c Counter Mode Timing Diagram

In Window mode, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TC2 pin (window pulse). When the contents of up-counter match with the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. **The frequency (window pulse) must be slower than the selected internal clock**.

In Writing to the TCR2DL, comparison is inhibited until TCR2DH is written.

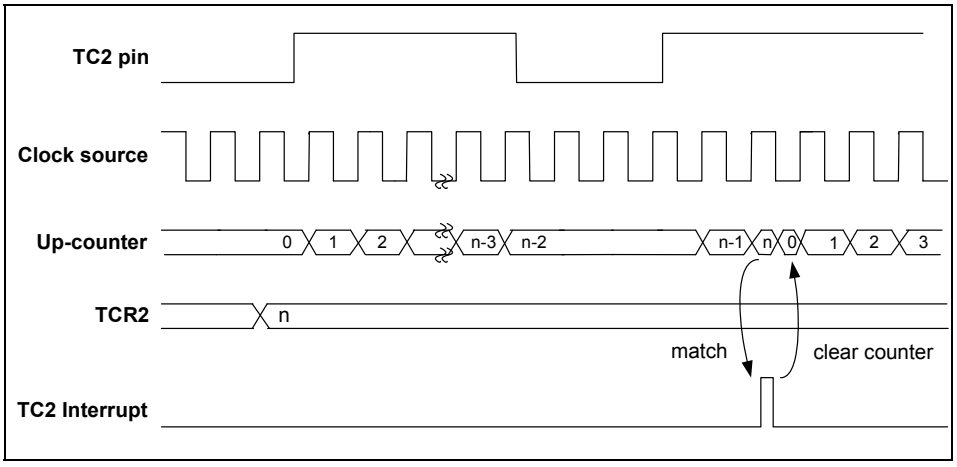


Figure 6-4d Window Mode Timing Diagram

6.1.22 Bank 1 R9 TC2DH (Timer 2 High Byte Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2D15	TC2D14	TC2D13	TC2D12	TC2D11	TC2D10	TC2D9	TC2D8

Bit 7 ~ Bit 0 (TCR2D15 ~ TCR2D8): High byte data buffer of 16-bit Timer/Counter 2

NOTE
For F641/541N, this register is reserved.

6.1.23 Bank 1 RA TC2DL (Timer 2 Low Byte Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2D7	TC2D6	TC2D5	TC2D4	TC2D3	TC2D2	TC2D1	TC2D0

Bit 7 ~ Bit 0 (TC2D7 ~ TC2D0): Low byte data buffer of 16-bit Timer/Counter 2

NOTE
For F641/541N, this register is reserved.

6.1.24 Bank 1 RB SPIS (SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	-	OD3	OD4	-	RBF

NOTE
For F642/542N, F641/541N, this register is reserved.

Bit 7 (DORD): Data transmission order

0: Shift left (MSB first)

1: Shift right (LSB first)

Bit 6~Bit 5 (TD1 ~ TD0): SDO status output delay time options

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4: Not used, set to "**0**" all the time.

Bit 3 (OD3): Open-Drain control bit

0: Open-drain disable for SDO

1: Open-drain enable for SDO

Bit 2 (OD4): Open-Drain control bit

0: Open-drain disable for SCK

1: Open-drain enable for SCK

Bit 1: Not used, set to "**0**" all the time

Bit 0 (RBF): Read Buffer Full flag

0: Receiving is not completed. SPIRB has not fully exchanged data.

1: Receiving completed; SPIRB has fully exchanged data.

6.1.25 Bank 1 RC SPIC (SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0

NOTE

For F642/542N, F641/541N, this register is reserved.

Bit 7 (CES): Clock Edge Select bit

0: Data shifts out on a rising edge, and shifts in on a falling edge. Data is on hold during low-level.

1: Data shifts out on a falling edge, and shifts in on a rising edge. Data is on hold during high-level.

Bit 6 (SPIE): SPI Enable bit

0: Disable SPI mode

1: Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0: No overflow

1: A new data is received while the previous data is still being held in the SPIRB register. Under this condition, the data in the SPI Shift register will be destroyed. To avoid setting this bit, users are required to read the SPIRB register although only transmission is implemented. This can only occur in Slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0: Reset as soon as the shifting is completed and the next byte is ready to shift.

1: Start to shift, and keep at "**1**" while the current byte is still being transmitted.

This bit will reset to "**0**" at every 1-byte transmission by the hardware.

Bit 3 (SDOC): SDO output status control bit

0: After Serial data output, the SDO remains high.

1: After Serial data output, the SDO remains low.

Bit 2 ~ Bit 0 (SBRS 2 ~ SBRS0): SPI Baud Rate Select bits

SBRS2 (Bit 2)	SBRS1 (Bit 1)	SBRS0 (Bit 0)	Mode	Baud Rate
0	**0**	**0**	Master	Fosc/2
0	**0**	**1**	Master	Fosc/4
0	**1**	**0**	Master	Fosc/8
0	**1**	**1**	Master	Fosc/16
1	**0**	**0**	Master	Fosc/32
1	**0**	**1**	Master	Fosc/64
1	**1**	**0**	Slave	/SS enable
1	**1**	**1**	Slave	/SS disable

6.1.26 Bank 1 RD SPIRB (SPI Read Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0

Bit 7 ~ Bit 0 (SPID7 ~ SPID0): SPI Read data buffer

NOTE

For F642/542N, F641/541N, this register is reserved.

6.1.27 Bank 1 RE SPIWB (SPI Write Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0

Bit 7 ~ Bit 0 (SWB7 ~ SWB0): SPI Write data buffer

NOTE

For F642/542N, F641/541N, this register is reserved.

6.1.28 Bank 1 RF (Interrupt Status Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IF	-	TC3IF	TC2IF	TC1IF	UERRIF	RBFF	TBEF

Bit 7 (CMP2IF): Comparator 2 Interrupt flag. Set when a change occurs in the Comparator 2 output. Reset by software.

Bit 6: Not used, set to "**0**" all the time.

Bit 5 (TC3IF): 8-bit Timer/Counter 3 Interrupt flag

Bit 4 (TC2IF): 16-bit Timer/Counter 2 Interrupt flag

Bit 3 (TC1IF): 8-bit Timer/Counter 1 Interrupt flag

Bit 2 (UERRIF): UART receiving error interrupt flag

Bit 1 (RBFF): UART receive mode data buffer full interrupt flag

Bit 0 (TBEF): UART transmit mode data buffer empty interrupt flag

NOTE

- *The Interrupt flag is automatically set by hardware. It must be cleared by software.*
- *For F642/542N, Bit 2 ~ Bit 0 are unused. Set to "**0**" all the time.*
- *For F641/541N, Bit 4 ~ Bit 0 are unused. Set to "**0**" all the time*

6.1.29 Bank 2 RA URC1 (UART Control 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE

NOTE

For F642/542N, F641/541N, this register is reserved.

Bit 7 (URTD8): Transmission Data Bit 8

Bit 6 ~ Bit 5 (UMODE1 ~ UMODE0): UART mode select

UMODE1	UMODE0	UART Mode
0	**0**	Mode 1: 7-bit
0	**1**	Mode 1: 8-bit
1	**0**	Mode 1: 9-bit
1	**1**	Reserved

Bit 4 ~ Bit 2 (BRATE2 ~ BRATE0): Transmit Baud Rate select

BRATE2	BRATE1	BRATE0	Baud Rate	4 MHz	8 MHz
0	**0**	**0**	Fc/13	19200	38400
0	**0**	**1**	Fc/26	9600	19200
0	**1**	**0**	Fc/52	4800	9600
0	**1**	**1**	Fc/104	2400	4800
1	**0**	**0**	Fc/208	1200	2400
1	**0**	**1**	Fc/416	600	1200
1	**1**	**0**	TC3	–	–
1	**1**	**1**	Reserved		

Bit 1 (UTBE): UART transfer buffer empty flag. Set to "**1**" when transfer buffer is empty. Automatically reset to "**0**" when writing to the URTD register. The **UTBE** bit will be cleared by hardware when transmission is enabled. The **UTBE** bit is read-only. Therefore, writing to the URTD register is necessary when you want to start shift transmission.

Bit 0 (TXE): Enable transmission

0: Disable

1: Enable

6.1.30 Bank 2 RB URC2 (UART Control 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	SBIM1	SBIM0	UINVEN	-	-	-

NOTE

For F642/542N, F641/541N, this register is reserved.

Bits 7 ~ 6: Not used, set to "**0**" all the time.

Bit 5 ~ Bit 4 (SBIM1 ~ SBIM0): Serial bus interface operating mode select

SBIM1	SBIM0	Operating Mode
0	0	I/O mode
0	1	SPI mode
1	0	UART mode
1	1	Reserved

Bit 3 (UNIVEN): Enable UART TXD and RXD port inverse output.

0: Disable **TXD** and **RXD** port inverse output

1: Enable **TXD** and **RXD** port inverse output

Bits 2 ~ 0: Not used, set to "**0**" all the time

6.1.31 Bank 2 RC URS (UART Status)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE

NOTE

For F642/542N, F641/541N, this register is reserved.

Bit 7 (URRD8): Receiving Data Bit 8

Bit 6 (EVEN): Select parity check

0: Odd parity

1: Even parity

Bit 5 (PRE): Enable parity addition

0: Disable

1: Enable

Bit 4 (PRERR): Parity error flag. Set to "**1**" when parity error occurred.

Bit 3 (OVERR): Over running error flag. Set to "**1**" when an overrun error occurred.

Bit 2 (FMERR): Framing error flag. Set to "**1**" when framing error occurred.

NOTE

The Interrupt flag is automatically set by hardware. It must be cleared by software.

Bit 1 (URBF): UART read buffer full flag. Set to "**1**" when one character is received. Reset to 0 automatically when read from URS and URRD register. The **URBF** will be cleared by hardware when enabling receiving. The URBF bit is read-only. Therefore, reading the URS register is necessary to avoid overrun error.

Bit 0 (RXE): Enable receiving

0: Disable

1: Enable

6.1.32 Bank 2 RD URRD (UART_RD Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0

Bits 7 ~ 0 (URRD7 ~ URRD0): UART receive data buffer. **Read only.**

NOTE

For F642/542N, F641/541N, this register is reserved.

6.1.33 Bank 2 RE URTD (UART_TD Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0

Bits 7 ~ 0 (URTD7 ~ URTD0): UART transmit data buffer. **Write only.**

NOTE

For F642/542N, F641/541N, this register is reserved.

6.1.34 Bank 2 RF (Pull-high Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	"1"	"1"

Bit 7 (/PH77): Control bit used to enable pull-high on the P77 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH76): Control bit used to enable pull-high on the P76 pin.

Bit 5 (/PH75): Control bit used to enable pull-high on the P75 pin.

Bit 4 (/PH74): Control bit used to enable pull-high on the P74 pin.

Bit 3 (/PH73): Control bit used to enable pull-high on the P73 pin.

Bit 2 (/PH72): Control bit used to enable pull-high on the P72 pin.

Bits 1 ~ 0: Not used, set to "**1**" all the time.

NOTE

- *The RF Register is both readable and writable.*
- *For F642/542N, Bit 6 ~ Bit 5, Bit 3 ~ Bit 0 are unused. Set to "**1**" all the time.*
- *For F641/541N, Bit 7 ~ Bit 0 are unused. Set to "**1**" all the time.*

6.1.35 Bank 3 R5 (TMRCON: Timer A and Timer B Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TAEN	TAP2	TAP1	TAP0	TBEN	TBP2	TBP1	TBP0

NOTE

For F642/542N, F641/541N, this register is reserved.

Bit 7 (TAEN): Timer A enable bit

0: Disable Timer A (default)

1: Enable Timer A

Bits 6 ~ 4 (TAP2 ~ TAP0): Timer A clock prescaler option bits.

Bit 3 (TBEN): Timer B enable bit

0: Disable Timer A (default)

1: Enable Timer A

Bits 2 ~ 0 (TBP2 ~ TBP0): Timer B clock prescaler option bits

TAP2/TBP2	TAP1/TBP1	TAP0/TBP0	Prescale
0	**0**	**0**	1:2 (Default)
0	**0**	**1**	1:4
0	**1**	**0**	1:8
0	**1**	**1**	1:16
1	**0**	**0**	1:32
1	**0**	**1**	1:64
1	**1**	**0**	1:128
1	**1**	**1**	1:256

6.1.36 Bank 3 R6 (TBHP: Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	-	-	-	RBit11	RBit10	RBit9	RBit8

Bit 7 (MLB): Select MSB or LSB machine code to be moved to the register.
The machine code is pointed by the TBLP and TBHP registers.

Bits 6 ~ 4: Not used, set to "**0**" all the time.

Bits 3 ~ 0: These are the 4 most significant bits of program code address

NOTE

- *For F642/542N, Bit 3 is unused. Set to "**0**" all the time.*
- *For F641/541N, Bit 3 & Bit 2 are unused. Set to "**0**" all the time.*

6.1.37 Bank 3 R7 (CMPCON: Comparator 2 Control Register and PWMA/B Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	CPOUT2	COS21	COS20	PWMAE	PWMBE

Bit 7 ~ Bit 5: Not used, set to "**0**" all the time

Bit 4 (CPOUT2): The result of Comparator 2 output

Bit 3 ~ Bit 2 (COS21 ~ COS20): Comparator 2 select bits

COS21	COS20	Function Description
0	**0**	Comparator 2 is not used. P80 acts as normal I/O pin
0	**1**	Act as a Comparator 2 and P80 acts as normal I/O pin
1	**0**	Act as a Comparator 2 and P80 acts as Comparator 2 output pin (CO)
1	**1**	Not used

Bit 1 (PWMAE): PWMA enable bit.

0: PWMA is off and its related pin carries out the P75 function (default).

1: PWMA is on, and its related pin is automatically set to output.

Bit 0 (PWMBE): PWMB enable bit.

0: PWMB is off and its related pin carries out the P76 function (default).

1: PWMB is on, and its related pin is automatically set to output.

NOTE

- *For F642/542N, Bit 1 & Bit 0 are unused. Set to "**0**" all the time.*
- *For F641/541N, Bit 1 & Bit 0 are unused. Set to "**0**" all the time.*

6.1.38 Bank 3 R8 (PWMCON: PWMA/B Lower 2 Bits of the Period and Duty Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA [1]	PRDA [0]	DTA [1]	DTA [0]	PRDB [1]	PRDB [0]	DTB [1]	DTB [0]

NOTE

For F642/542N, F641/541N, this register is reserved.

Bits 7 ~ 6 (PRDA [1], PRDA [0]): Least Significant Bits of PWMA Period Cycle.

Bits 5 ~ 4 (DTA [1], DTA [0]): Least Significant Bits of PWMA Duty Cycle.

Bits 3 ~ 2 (PRDB [1], PRDB [0]): Least Significant Bits of PWMB Period Cycle.

Bits 1 ~ 0 (DTB [1], DTB [0]): Least Significant Bits of PWMB Duty Cycle.

6.1.39 Bank 3 R9 (PRDAH: Most Significant Byte (Bit 9 ~ Bit 2) of PWMA)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA [9]	PRDA [8]	PRDA [7]	PRDA [6]	PRDA[5]	PRDA [4]	PRDA [3]	PRDA [2]

The content of Bank 3 of R9 is a period (time base) of PWMA Bit 9~Bit 2. The frequency of PWMA is the reverse of the period.

NOTE

For F642/542N, F641/541N, this register is reserved.

6.1.40 Bank 3 RA (DTAH: Most Significant Byte (Bit 9 ~ Bit 2) of PWMA Duty Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA[9]	DTA[8]	DTA[7]	DTA[6]	DTA[5]	DTA[4]	DTA[3]	DTA[2]

A specified value keeps the PWMA output to remain high until the value matches with TMRA.

NOTE

For F642/542N, F641/541N, this register is reserved.

6.1.41 Bank 3 RB (PRDBH: Most Significant Byte (Bit 9~Bit 2) of PWMB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB[9]	PRDB[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]

The content of Bank 3 of R9 is a period (time base) of PWMB Bit 9~Bit 2. The frequency of PWMB is the reverse of the period.

NOTE

For F642/542N, F641/541N, this register is reserved.

6.1.42 Bank 3 RC (DTBH: Least Significant Byte (Bit 9 ~ Bit 2) of PWMB Duty Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB[9]	DTB[8]	DTB[7]	DTB[6]	DTB[5]	DTB[4]	DTB[3]	DTB[2]

A specified value keeps the PWMB output to remain high until the value matches with TMRB.

NOTE

For F642/542N, F641/541N, this register is reserved.

6.1.43 Bank 3 RD TC3CR (Timer 3 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bits 7 ~ 6 (TC3FF1 ~ TC3FF0): Timer/Counter 3 flip-flop control

TC3FF1	TC3FF0	Operating Mode
0	0	Clear
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5 (TC3S): Timer/Counter 3 start control

0: Stop and clear the counter

1: Start Timer/Counter 3

Bits 4 ~ 2 (TC3CK2 ~ TC3CK0): Timer/Counter 3 clock source select

TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution	Max. Time	Resolution	Max. Time
			Normal, Idle	Fc=4M	Fc=4M	Fc=16K	Fc=16K
0	**0**	**0**	$Fc/2^{11}$	512 µs	131072 µs	128 ms	32768 ms
0	**0**	**1**	$Fc/2^{7}$	32 µs	8192 µs	8 ms	2048 ms
0	**1**	**0**	$Fc/2^{5}$	8 µs	2048 µs	2 ms	512 ms
0	**1**	**1**	$Fc/2^{3}$	2 µs	512 µs	500 µs	128 ms
1	**0**	**0**	$Fc/2^{2}$	1 µs	256 µs	250 µs	64 ms
1	**0**	**1**	$Fc/2^{1}$	500 ns	128 µs	125 µs	32 ms
1	**1**	**0**	Fc	250 ns	64 µs	62.5 µs	16 ms
1	**1**	**1**	External clock (TC3 pin)	-	-	-	-

Bits 1 ~ 0 (TC3M1 ~ TC3M0): Timer/Counter 3 operating mode select

TC3M1	TC3M0	Operating Mode
0	0	Timer/Counter
0	1	Reserved
1	0	Programmable Divider Output
1	1	Pulse Width Modulation Output

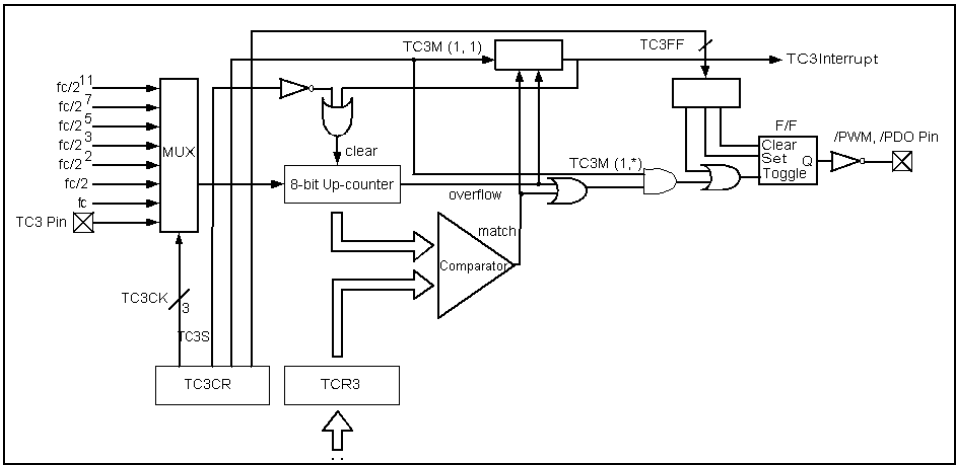


Figure 6-5a Timer / Counter 3 Configuration

In Timer mode, counting up is performed using the internal clock (rising edge trigger). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using an external clock input pin (TC3 pin). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by the program and it is initialized to "0" during reset.** A TC3 interrupt is generated each time the /PDO output is toggled.

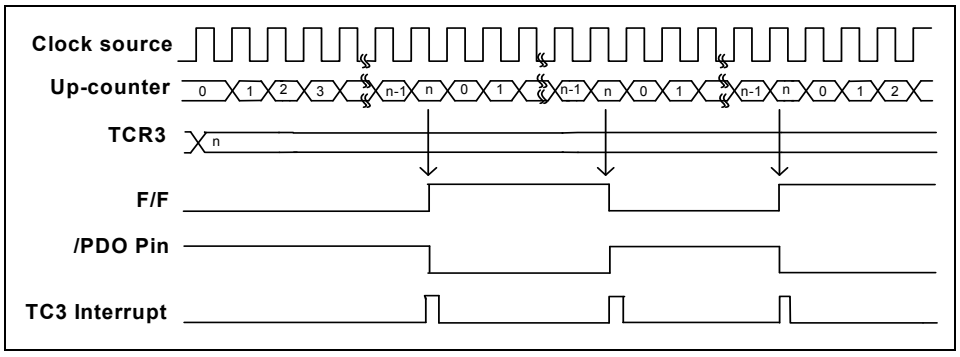


Figure 6-5b PDO Mode Timing Chart

In Pulse Width Modulation (PWM) Output Mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. While the counter continues counting, the F/F is toggled again when the counter overflows, after which the counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and, during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Therefore, the output can be changed continuously. However, only when TC3S is set to "**1**" will the TCR3 start to shift and allows data to be loaded into TCR3.

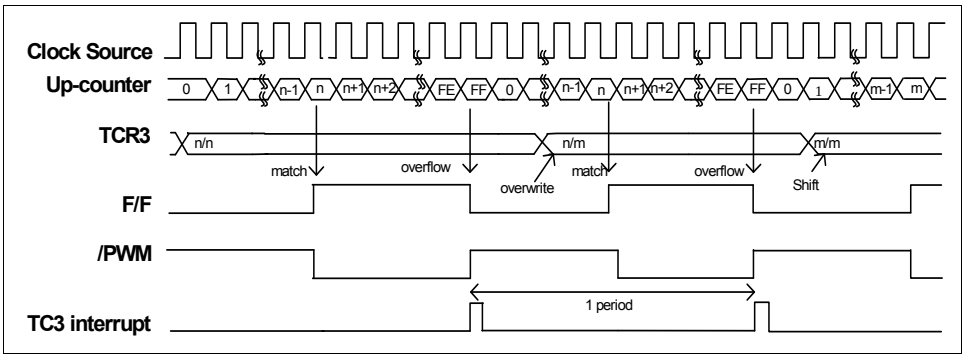


Figure 6-5c PWM Mode Timing Chart

6.1.44 Bank 3 RE TC3D (Timer 3 Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0

Bits 7 ~ 0 (TC3D7 ~ TC3D0): Data Buffer of 8-bit Timer/Counter 3.

6.1.45 Bank 3 RF (Pull-Down Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD77	/PD76	/PD75	/PD74	/PD73	/PD72	”1”	”1”

Bit 7 (/PD77): Control bit used to enable pull-down on P77 pin

0: Enable internal pull-down

1: Disable internal pull-down

Bit 6 (/PD76): Control bit used to enable pull-down of the P76 pin.

Bit 5 (/PD75): Control bit used to enable pull-down of the P75 pin.

Bit 4 (/PD74): Control bit used to enable pull-down of the P74 pin.

Bit 3 (/PD73): Control bit used to enable pull-down of the P73 pin.

Bit 2 (/PD72): Control bit used to enable pull-down of the P72 pin.

Bits 1 ~ 0: Not used, set to "**1**" all the time.

NOTE

- *The RF register is both readable and writable.*
- *For F642/542N, Bit 6 ~ Bit 5, Bit 3 ~ Bit 0 are unused. Set to "**1**" all the time.*
- *For F641/541N, Bit 7 ~ Bit 0 are unused. Set to "**1**" all the time.*

6.2 Special Function Registers (for EM78F644/642/641/544/542/541N Series Only)

6.2.1 A (Accumulator)

Internal data transfer operation or instruction operand holding usually involves the temporary storage function of the Accumulator. The Accumulator is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	/INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

0: Interrupt occurs at rising edge of the INT pin

1: Interrupt occurs at falling edge of the INT pin

Bit 6 (/INT): Interrupt enable flag

0: Masked by DISI or hardware interrupt

1: Enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

0: Internal instruction cycle clock

1: Transition on TCC pin

Bit 4 (TE): TCC signal edge

0: Increment if a transition from low to high takes place on the TCC pin

1: Increment if a transition from high to low takes place on the TCC pin

NOTE

*For F641/541N, Bit 5 ~ Bit 4 are unused. Set to "**0**" all the time.*

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit, TCC rate is 1:1

1: Prescaler enable bit, TCC rate is set as Bit 2~Bit 0

Bit 2 ~ Bit 0 (PST 2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

NOTE

The CONT register is both readable and writable.

6.2.3 IOC5 (I/O Port 5 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C57	C56	C55	C54	C53	C52	C51	C50

Bit 7 ~ 0 (C57 ~ C50): 8-bit Port5 I/O data register

0: Define I/O pin as output

1: Define I/O pin as high impedance

You can use IOC5 register to define each bit as input or output.

NOTE

- *For F642/542N, Bit 6, Bit 3 ~ Bit 1 are unused. Set to "**0**" all the time.*
- *For F641/541N, Bit 6, Bit 3 ~ Bit 1 are unused. Set to "**0**" all the time.*

6.2.4 IOC6 (I/O Port 6 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C67	C66	C65	C64	C63	C62	C61	C60

Bit 7 ~ 0 (C67 ~ C60): 8-bit Port6 I/O data register

0: Define I/O pin as output

1: Define I/O pin as high impedance

You can use IOC6 register to define each bit as input or output.

NOTE

*For F641/541N, Bit 7 ~ Bit 6 are unused. Set to "**0**" all the time.*

6.2.5 IOC7 (I/O Port 7 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C77	C76	C75	C74	C73	C72	-	-

Bits 7 ~ 2 (C77 ~ C72): 6-bit Port7 I/O data register

0: Define I/O pin as output

1: Define I/O pin as high impedance

Bits 1 ~ 0: Not used, set to "**0**" all the time.

You can use IOC7 register to define each bit as input or output.

NOTE

- *For F642/542N, Bit 6 ~ Bit 5, Bit 3 ~ Bit 0 are unused. Set to "**0**" all the time.*
- *For F641/541N, Bit 7 ~ Bit 0 are unused. Set to "**0**" all the time.*

6.2.6 IOC8 (I/O Port 8 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	C83	C82	C81	C80

Bits 7 ~ 4: Not used, set to "**0**" all the time.

Bit 3 ~ 0 (C83 ~ C80): 4-bit Port8 I/O data register

0: Define I/O pin as output

1: Define I/O pin as high impedance

You can use IOC8 register to define each bit as input or output.

NOTE

*For F644N, Bit 3 is unused. Set to "**0**" all the time.*

6.2.7 IOC9

Reserved registers

6.2.8 IOCA (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	-	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable the Watchdog timer

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the P60 (/INT) pin function

0: P60, bidirectional I/O pin

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "**1**".

When EIS is "**0**", the /INT path is masked. When EIS is "**1**", the status of the /INT pin can also be read by way of reading Port 6 (R6).

The EIS is both readable and writable.

Bits 5 ~ 4: Not used, set to "**0**" all the time

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit. WDT rate is 1:1

1: Prescaler enable bit. WDT rate is set at Bit 0~Bit 2

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.9 IOCB (Pull-Down Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD63	/PD62	/PD61	/PD60	/PD53	/PD52	/PD51	/PD50

Bit 7 (/PD63): Control bit used to enable pull-down of the P63 pin.

0: Enable internal pull-down

1: Disable internal pull-down

Bit 6 (/PD62): Control bit used to enable pull-down on P62 pin

Bit 5 (/PD61): Control bit used to enable pull-down on P61 pin

Bit 4 (/PD60): Control bit used to enable pull-down on P60 pin

Bit 3 (/PD53): Control bit used to enable pull-down on P53 pin

Bit 2 (/PD52): Control bit used to enable pull-down on P52 pin

Bit 1 (/PD51): Control bit used to enable pull-down on P51 pin

Bit 0 (/PD50): Control bit used to enable pull-down on P50 pin

The IOCB Register is both readable and writable.

NOTE

- *For F642/542N, Bit 3 ~ Bit 1 are unused. Set to "**1**" all the time.*
- *For F641/541N, Bit 3 ~ Bit 1 are unused. Set to "**1**" all the time.*

6.2.10 IOCC (Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60

Bit 7 (OD67): Control bit used to enable open-drain output of the P67 pin.

0: Disable open-drain output

1: Enable open-drain output

Bit 6 (OD66): Control bit used to enable open-drain output on P66 pin

Bit 5 (OD65): Control bit used to enable open-drain output on P65 pin

Bit 4 (OD64): Control bit used to enable open-drain output on P64 pin

Bit 3 (OD63): Control bit used to enable open-drain output on P63 pin

Bit 2 (OD62): Control bit used to enable open-drain output on P62 pin

Bit 1 (OD61): Control bit used to enable open-drain output on P61 pin

Bit 0 (OD60): Control bit used to enable open-drain output on P60 pin

The IOCC Register is both readable and writable.

NOTE

*For F641/541N, Bit 7 ~ Bit 6 are unused. Set to "**0**" all the time.*

6.2.11 IOCD (Pull-High Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

Bit 7 (/PH67): Control bit used to enable pull-high of the P67 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH66): Control bit used to enable pull-high on P66 pin

Bit 5 (/PH65): Control bit used to enable pull-high on P65 pin

Bit 4 (/PH64): Control bit used to enable pull-high on P64 pin

Bit 3 (/PH63): Control bit used to enable pull-high on P63 pin

Bit 2 (/PH62): Control bit used to enable pull-high on P62 pin

Bit 1 (/PH61): Control bit used to enable pull-high on P61 pin

Bit 0 (/PH60): Control bit used to enable pull-high on P60 pin

The IOCD Register is both readable and writable.

NOTE

*For F641/541N, Bit 7 ~ Bit 6 are unused. Set to "**1**" all the time.*

6.2.12 IOCE (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IE	-	TC3IE	TC2IE	TC1IE	UERRIE	URIE	UTIE

Bit 7 (CMP2IE): CMP2IF interrupt enable bit.

0: Disable CMP2IF interrupt

1: Enable CMP2IF interrupt

When the Comparator 2 output status change is used to enter an interrupt vector or enter the next instruction, the CMP2IE bit must be set to "Enable".

Bit 6: Not used, set to "**0**" all the time.

Bit 5 (TC3IE): Interrupt enable bit

0: Disable TC3IF interrupt

1: Enable TC3IF interrupt

Bit 4 (TC2IE): Interrupt enable bit

0: Disable TC2IF interrupt

1: Enable TC2IF interrupt

Bit 3 (TC1IE): Interrupt enable bit

0: Disable TC1IF interrupt

1: Enable TC1IF interrupt

Bit 2 (UERRIE): UART receive error interrupt enable bit

0: Disable UERRIF interrupt

1: Enable UERRIF interrupt

Bit 1 (URIE): UART receive mode Interrupt enable bit

0: Disable RBFF interrupt

1: Enable RBFF interrupt

Bit 0 (UTIE): UART transmit mode interrupt enable bit.

0: Disable TBEF interrupt

1: Enable TBEF interrupt

The IOCE Register is both readable and writable.

NOTE

- *For F642/542N, Bit 2 ~ Bit 0 are unused. Set to "**0**" all the time.*
- *For F641/541N, Bit 4 ~ Bit 0 are unused. Set to "**0**" all the time.*

6.2.13 IOCF (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ADIE	SPIIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE

Bits 7 ~ 6: Not used, set to "**0**" all the time.

Bit 5 (SPIIE): SPIIF interrupt enable bit.

0: Disable SPIIF interrupt

1: Enable SPIIF interrupt

Bit 4 (PWMBIE): PWMBIF interrupt enable bit

0: Disable PWMBIF interrupt

1: Enable PWMBIF interrupt

Bit 3 (PWMAIE): PWMAIF interrupt enable bit

0: Disable PWMAIF interrupt

1: Enable PWMAIF interrupt

Bit 2 (EXIE): EXIF interrupt enable bit

0: Disable EXIF interrupt

1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: Disable ICIF interrupt

1: Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0: Disable TCIF interrupt

1: Enable TCIF interrupt

The IOCF Register is both readable and writable.

NOTE

- *Individual interrupt is enabled by setting its associated control bit in the IOCF to "**1**".*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction.*
- *For F642/542N, Bit 5 ~ Bit 3 are unused. Set to "**0**" all the time.*
- *For F641/541N, Bit 5 ~ Bit 3 are unused. Set to "**0**" all the time.*

6.3 Operational Registers for EM78F648/548N

6.3.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.3.2 R1: BSR (Bank Selection Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	SBS0	0	0	0	GBS0

Bits 7 ~ 5: Not used, set to "**0**" all the time.

Bit 4 (SBS0): Special register bank select bit. It is used to select Bank 0/1 of special register R5~R4F.

0: Bank 0

1: Bank 1

Bits 3~1: Not used, set to "**0**" all the time.

Bit 0 (GBS0): General register bank select bit. It is used to select Bank 0/1of general register R80~RFF.

0: Bank 0

1: Bank 1

6.3.3 R2: PC (Program Counter)

- Depending on the device type, R2 and hardware stack are 12-bits wide. The program counter structure is depicted in Figure 6-6 below.
- Generates 8K×15 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 4096 words long.
- R2 is set as all "**0**"s when under RESET condition.
- "JMP" instruction allows direct loading of the lower 12 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 12 bits of the PC, and the present PC value will add 1 and is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 13 program counter bits. Therefore, "LJMP" allows PC to jump to any location within 8K (213).
- "LCALL" instruction loads the lower 13 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within 8K (213).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.

- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC are not changed.
- •Any instruction (except “ADD R2,A”) that is written to R2 (e.g., "MOV R2, A", "BC R2, 6",·etc.) will cause the ninth bit and the above bits (A8~A11) of the PC to remain unchanged.
- All instruction are single instruction cycle (fclk/2,fclk/4,fclk/8,fclk/16). The instruction that would change the contents of R2 will need one more instruction cycles.

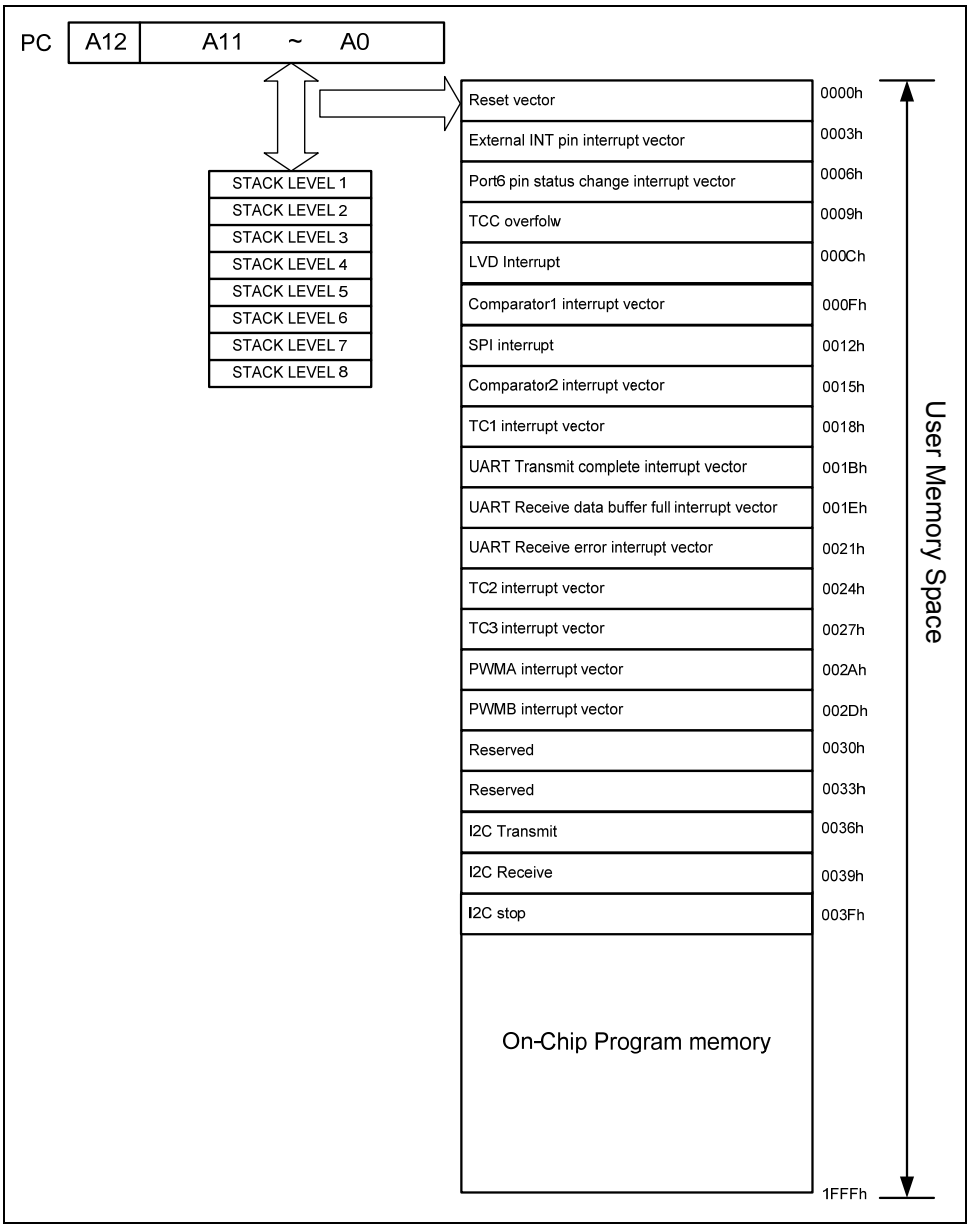


Figure 6-6 Program Counter Structure

■ **Data Memory Configuration**

Address	BANK 0	BANK 1
0X00	IAR (Indirect Addressing Reg.)	
0X01	BSR (Bank Selection Control Reg.)	
0X02	PC (program counter)	
0X03	SR (Status Reg.)	
0X04	RSR (RAM Selection Reg.)	
0X05	Port 5	P5PHCR
0X06	Port 6	P6PHCR
0X07	Port 7	P7PHCR
0X08	Port 8	P8PHCR
0X09	Port 9	P9PHCR
0X0A	-	-
0x0B	OMCR (Operating Mode Control Reg.)	P5PLCR
0X0C	ISR1 (Interrupt Status Reg. 1)	P6PLCR
0X0D	ISR2 (Interrupt Status Reg. 2)	P7PLCR
0X0E	ISR3 (Interrupt Status Reg. 3)	P8PLCR
0X0F	-	P9PLCR
0X10	EIESCR	-
0X11	WDTCR	P5HD/SCR
0X12	LVDCR	P6HD/SCR
0X13	TCCCR	P7HD/SCR
0X14	TCCDATA	P8HD/SCR
0X15	IOCR5	P9HD/SCR
0X16	IOCR6	-
0X17	IOCR7	P5ODCR
0X18	IOCR8	P6ODCR
0X19	IOCR9	P7ODCR
0X1A	-	P8ODCR
0X1B	-	P9ODCR
0X1C	IMR1 (Interrupt Mask Reg. 1)	-
0X1D	IMR2 (Interrupt Mask Reg. 2)	IRCS
0X1E	IMR3 (Interrupt Mask Reg. 3)	-
0X1F	-	EEROM CONTROL
0X20	P5WUCR	EEPROM ADDR
0X21	P5WUECR	EEPROM DATA

(Continuation)

Address	BANK 0	BANK 1
0X22	P7WUCR	-
0X23	P7WUECR	I2CCR1(I2C status and control reg. 1)
0X24	-	I2CCR2(I2C status and control reg. 2)
0X25	-	I2CSA(I2C slave address reg.)
0X26	-	I2CDA(I2C device address reg.)
0X27	-	I2CDB(I2C data buffer)
0X28	-	I2CA
0X29	-	-
0X2A	-	PWMER(PWM Enable Control Reg.r)
0x2B	SPICR (SPI Control Reg.)	TIMEN(Timer/PWM Enable Control Reg.)
0X2C	SPIS (SPI Status Reg.)	-
0X2D	SPIR (SPI Read Buffer)	-
0X2E	SPIW (SPI Write Buffer)	-
0X2F	WUCR1	PWMACR(PWM A control reg.)
0X30	-	PWMBCR(PWM B control reg.)
0X31	-	-
0X32	URCR1 (UART Control Reg. 1)	TACR(Timer A control reg.)
0X33	URCR2 (UART Control Reg. 2)	TBCR(Timer B control reg.)
0X34	URS (UART Status Register)	-
0X35	URRD (UART Receive Data Buffer Reg.)	TAPRD(Timer A Period buffer)
0X36	URTD (UART Transmit Data Buffer Reg.)	TBPRD(Timer B Period buffer)
0X37	TBPTL	-
0X38	TBPTH	TADT(Timer A Duty Buffer)
0X39	CMP1CR(Comparator 1 Control Reg.)	TBDT(Timer B Duty Buffer)
0X3A	-	-
0x3B	-	PRDxL
0X3C	CMP2CR	DTxL
0X3D	-	-
0X3E	-	-
0X3F	-	-
0X40	-	-
0X41	-	-
0X42	-	-
0X43	CPIRLCON	-
0X44	-	-

(Continuation)

Address	BANK 0	BANK 1
0X45	-	-
0X46	-	-
0X47	-	-
0X48	TC1CR	-
0X49	TCR1DA	-
0X4A	TCR1DB	-
0x4B	TC2CR	-
0X4C	TCR2DH	-
0X4D	TCR2DL	-
0X4E	TC3CR	-
0X4F	TCR3D	-
0X50	GENERAL PURPOSE REGISTER	
0X51		
. .		
0X7F		
0X80	BANK 0	BANK 1
0X81		
. . .		
0XFE		
0XFF		

6.3.4 R3: SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	T	P	Z	DC	C

Bits 7~5: Not used, set to "**0**" all the time.

Bit 4 (T): Time-out bit

Set to "**1**" by "SLEP" and "WDTC" command executions or during power up. Reset to "**0**" when WDT time-out occurs.

Bit 3 (P): Power down bit

Set to "**1**" at power on or by "WDTC" command execution. Reset to "**0**" by "SLEP" command execution.

Bit 2 (Z): Zero flag

Set to "**1**" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.3.5 R4: RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

Bit 7~0 (RSR7~RSR0): These bits are used to select registers (Address: 00~FF) in indirect address mode. Refer to the table on Data Memory Configuration (Section 6.3.3) for more details.

6.3.6 Bank0 R5 ~ R9 (Port 5 ~ Port 9)

R5, R6, R7, R8, & R9 are I/O data registers.

6.3.7 Bank0 RA (Not Used)

6.3.8 Bank0 RB OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	TC1SS	TC2SS	TC3SS	TASS	TBSS	0

Bit 7 (CPUS): CPU Oscillator Source Select.

0: Fs: sub-oscillator for WDT internal RC time base

1: Fm: main-oscillator

When CPUS=0, the CPU oscillator will select sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle mode enable bit.` This bit defines and instruct SLEP instruction which mode to go after the instruction is executed.

0: "IDLE=0"+SLEP instruction => Sleep mode

1: "IDLE=1"+SLEP instruction => Idle mode

■ CPU Operation Mode

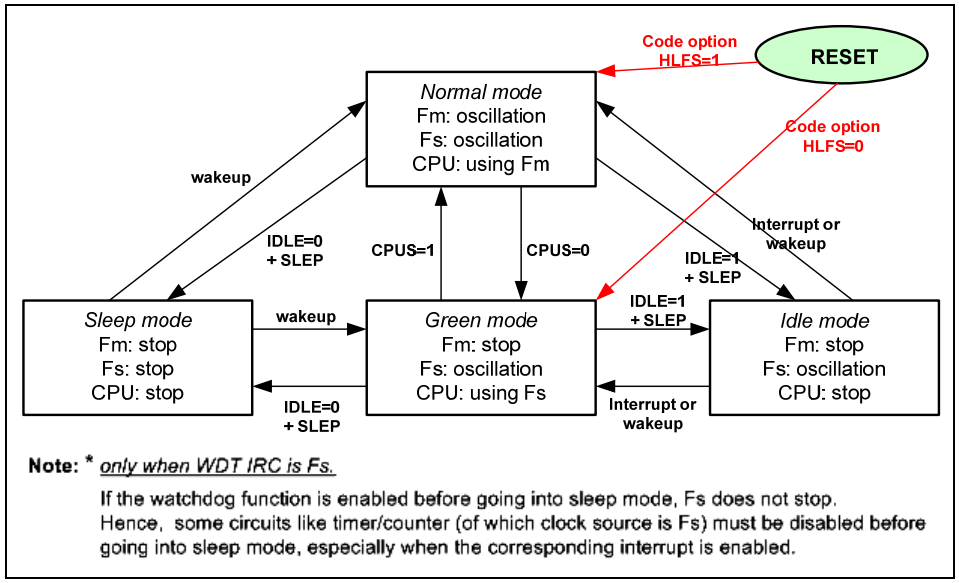


Figure 6-7 CPU Operation Mode Block Diagram

Oscillator (Normal Mode Source)	CPU Mode Status	Oscillator Stable Time (S)[1]	Count from Normal/Green (CLK)[2]
Crystal ; 1M ~ 16 MHz	Sleep/Idle → Normal	0.5 ms ~ 2 ms	254 CLK
	Green → Normal		254 CLK
	Sleep/Idle → Green	< 100 µs	32 CLK
ERC ; 3.5 MHz	Sleep/Idle → Normal	< 5 µs	32 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	
IRC ; 455K, 4M, 8M, 16 MHz	Sleep/Idle → Normal	< 2 µs	32 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	

[1] *The oscillator stable time depends on the oscillator characteristics*

[2] *After the oscillator has stabilized, the CPU will count 254/32 CLK in Normal/Green mode and continue to work in Normal/Green mode.*

Ex 1: *The 4 MHz IRC Wakes-up from Sleep mode to Normal mode. The total Wake-up time is 2 µs + 32 CLK @ 4 MHz*

Ex 2: *The 4 MHz IRC Wakes-up from Sleep mode to Green mode. The total wake-up time is 100 µs + 32 CLK @ 16kHz*

Bit 5 (TC1SS): TC1 clock source select bit

0: Fs is used as Fc

1: Fm is used as Fc

Bit 4 (TC2SS): TC2 clock source select bit

0: Fs is used as Fc

1: Fm is used as Fc

Bit 3 (TC3SS): TC3 clock source select bit

0: Fs is used as Fc

1: Fm is used as Fc

Bit 2 (TASS): Timer A clock source select bit

0: Fs is used as Fc

1: Fm is used as Fc

Bit 1 (TBSS): Timer B clock source select bit

0: Fs is used as Fc

1: Fm is used as Fc

Bit 0: Not used, fixed to "**0**" all the time.

6.3.9 Bank0 RC: ISR1 (Interrupt Status Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIF	0	SPIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF

NOTE: *Set to "**1**" to enable Interrupt Request, "**0**" to disable interrupt execution.*

Bit 7(LVDIF): Low voltage detector interrupt flag

When LVD1, LVD0 = "0,0", Vdd > 2.3V, LVDIF is "**0**",
Vdd<= 2.3V, set LVDIF to "**1**". LVDIF reset to "**0**" by software.

When LVD1, LVD0 = "0,1", Vdd > 3.3V, LVDIF is "**0**",
Vdd<= 3.3V, set LVDIF to "**1**". LVDIF reset to "**0**" by software.

When LVD1, LVD0 = "1,0", Vdd > 4.0V, LVDIF is "**0**",
Vdd<= 4.0V, set LVDIF to "**1**". LVDIF reset to "**0**" by software.

When LVD1, LVD0 = "1,1", Vdd > 4.5V, LVDIF is "**0**",
Vdd<= 4.5V, set LVDIF to "**1**". LVDIF reset to "**0**" by software.

Bit 6: Not used, fixed to "**0**" all the time.

Bit 5 (SPIF): SPI mode interrupt flag. Flag is cleared by software.

Bit 4 (PWMBIF): PWMB (Pulse Width Modulation) interrupt flag.
Set when a selected period is reached. Reset by software.

Bit 3 (PWMAIF): PWMA (Pulse Width Modulation) interrupt flag.
Set when a selected period is reached. Reset by software.

Bit 2 (EXIF): External interrupt flag.

Bit 1 (ICIF): Port 6 input status change interrupt flag.
Set when Port 6 input changes. Reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag.
Set when TCC overflows. Reset by software.

6.3.10 Bank0 RD: ISR2 (Interrupt Status Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IF	CMP1IF	TC3IF	TC2IF	TC1IF	UERRIF	RBFF	TBEF

Bit 7 (CMP2IF): Comparator2 interrupt flag. Set when a change occurs in the output of Comparator2. Reset by software.

Bit 6 (CMP1IF): Comparator1 interrupt flag. Set when a change occurs in the output of Comparator1. Reset by software.

Bit 5(TC3IF): 8-bit timer/counter 3 interrupt flag. Flag cleared by software.

Bit 4 (TC2IF): 16-bit timer/counter 2 interrupt flag. Flag cleared by software.

Bit 3 (TC1IF): 8-bit timer/counter 1 interrupt flag. Flag cleared by software.

Bit 2 (UERRIF): UART receiving error interrupt. Flag cleared by software or UART disabled.

Bit 1 (RBFF): UART receive mode data buffer full interrupt flag.
Flag cleared by software.

Bit 0 (TBEF): UART transmit mode data buffer empty interrupt flag.
Flag cleared by software.

6.3.11 Bank0 RE: ISR3 (Interrupt Status Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	I2CSTPIF	0	I2CRIF	I2CTIF

Bits 7~4: Not used, fixed to "**0**" all the time.

Bit 3 (I2CSTPIF): I2C slave receive data stop interrupt flag

Bit 2: Not used, fixed to "**0**" all the time.

Bit 1 (I2CRIF): I2C receive interrupt flag. Set when I2C receives 1byte data and responds ACK signal. Reset by firmware or I2C disable.

Bit 0 (I2CTIF): I2C transmit interrupt flag. Set when I2C transmits 1 byte data and receive handshake signal (ACK or NACK). Reset by firmware or I2C disable.

6.3.12 Bank0 RF (Not Used)

6.3.13 Bank0 R10: EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	EIES

Bits 7~1: Not used, fixed to "**0**" all the time.

Bit 0 (EIES): External interrupt edge select bit

0: Falling edge interrupt

1: Rising edge interrupt

6.3.14 Bank0 R11: WDTCR

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	INT	0	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Watchdog Timer enable bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bit 6 (EIS): P60/ /INT switch control bit. EIS is both readable and writable.

0: P60

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 must be set to "**1**". When EIS is "**0**", the path of /INT is masked. When EIS is "**1**", the status of /INT pin can also be read through reading Port 6 (R6).

Bits 5 (INT): Interrupt enable flag

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/DISI instructions

Bits 4: Not used, fixed to "**0**" all the time.

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disabled, WDT rate is 1:1

1: Prescaler enabled, WDT rate is set from bits 2~0

Bits 2~0 (PSW2~PSW0): WDT Prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	**0**	**0**	1:2
0	**0**	**1**	1:4
0	**1**	**0**	1:8
0	**1**	**1**	1:16
1	**0**	**0**	1:32
1	**0**	**1**	1:64
1	**1**	**0**	1:128
1	**1**	**1**	1:256

6.3.15 Bank0 R12: LVDCR (Low Voltage Detector Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	LVDEN	/LVD	LVD1	LVD0

Bits 7~4: Not used, fixed to "**0**" all the time.

Bit 3 (LVDEN): Low voltage detector enable bit

0: LVD disable

1: LVD enable

Bit 2 (/LVD): Low voltage detector. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (which is set by LVD1 and LVD0), this bit will be cleared.

0: The low voltage is detected

1: The low voltage is not detected or LVD function is disabled

Bits1~0 (LVD1~LVD0): Low voltage detector level select bits

LVD1	LVD0	LVD Voltage Interrupt Level
0	**0**	2.3
0	**1**	3.3
1	**0**	4.0
1	**1**	4.5

6.3.16 Bank0 R13: TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	TCCS	TS	TE	PSTE	PST2	PST1	PST0

Bit 7: Not used, fixed to "**0**" all the time.

Bit 6 (TCCS): TCC Clock Source Select Bit

0: Fs (sub clock)

1: Fm (main clock)

Bit 5 (TS): TCC Signal Source

0: Internal oscillator cycle clock. If P77 is used as I/O pin, TS must be "**0**".

1: Transition on the TCC pin

Bit 4 (TE): TCC Signal Edge

0: Increment if the transition from low to high takes place on the TCC pin;

1: Increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disabled, TCC rate is 1:1

1: Prescaler enabled, TCC rate is set as Bits 2~0.

Bits 2~0 (PST2~PST0): TCC Prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.3.17 Bank0 R14: TCCDATA (TCC Data Register)

Increase by an external signal edge through the TCC pin, or by the instruction cycle clock. External signal of TCC trigger pulse width must be greater than one instruction. The signals to increase the counter are determined by Bit 4 and Bit 5 of the TCCCR register. This register is writable and readable as any other registers.

6.3.18 Bank0 R15~R19 (IOCR5~IOCR9)

These registers are used to control I/O port direction. They are both readable and writable.

0: Set the relative I/O pin as output

1: Set the relative I/O pin into high impedance

6.3.19 Bank0 R1A~R1B (Not Used)

6.3.20 Bank0 R1C: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	0	SPIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE

Bits 7 (LVDIE): LVDIF interrupt enable bit

0: Disable LVDIF interrupt

1: Enable LVDIF interrupt

Bit 6: Not used, fixed to "**0**" all the time.

Bit 5 (SPIE): Interrupt enable bit

0: Disable SPIF interrupt

1: Enable SPIF interrupt

Bit 4 (PWMBIE): PWMBIF interrupt enable bit

0: Disable PWMB interrupt

1: Enable PWMB interrupt

Bit 3 (PWMAIE): PWMAIF interrupt enable bit

0: Disable PWMA interrupt

1: Enable PWMA interrupt

Bit 2 (EXIE): EXIF interrupt enable bit

0: Disable EXIF interrupt

1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: Disable ICIF interrupt

1: Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0: Disable TCIF interrupt

1: Enable TCIF interrupt

6.3.21 Bank0 R1D: IMR2 (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IE	CMP1IE	TC3IE	TC2IE	TC1IE	UERRIE	URIE	UTIE

Bit 7 (CMP2IE): CMP2IF interrupt enable bit

0: Disable CMP2IF interrupt

1: Enable CMP2IF interrupt

When the Comparator output status changeis used to enter interrupt vector or enter the instruction, the CMP2IE bit must be set to “Enable“.

Bit 6 (CMP2IE): CMP1IF interrupt enable bit

0: Disable CMP1IF interrupt

1: Enable CMP1IFinterrupt

When the Comparator output status change is used to enter interrupt vector or enter the next instruction, the CMP1IE bit must be set to “Enable“.

Bit 5 (TC3IE): Interrupt enable bit.

0: Disable TC3IF interrupt

1: Enable TC3IF interrupt

Bit 4 (TC2IE): Interrupt enable bit

0: Disable TC2IF interrupt

1: Enable TC2IF interrupt

Bit 3 (TC1IE): Interrupt enable bit

0: Disable TC1IF interrupt

1: Enable TC1IF interrupt

Bit 2 (UERRIE): UART receive error interrupt enable bit

0: Disable UERRIF interrupt

1: Enable UERRIF interrupt

Bit 1 (URIE): UART receive mode Interrupt enable bit

0: Disable RBFF interrupt

1: Enable RBFF interrupt

Bit 0 (UTIE): UART transmit mode interrupt enable bit

0: Disable TBEF interrupt

1: Enable TBEF interrupt

6.3.22 Bank0 R1E: IMR3 (Interrupt Mask Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	I2CSTPIE	0	I2CRIE	I2CTIE

Bits 7~3: Not used, fixed to "**0**" all the time.

Bit 3 (I2CSTPIE): I2CSTPIF interrupt enable bit.

0: Disable I2CSTP interrupt

1: Enable I2CSTP interrupt

Bit 2: Not used, fixed to "**0**" all the time.

Bit 1 (I2CRIE): I2C Interface Rx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

Bit 2 (I2CTIE): I2C Interface Tx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

6.3.23 Bank0 R1F (Not Used)

6.3.24 Bank0 R20: P5WUCR (Port 5 Wake Up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WU_P57	WU_P56	WU_P55	WU_P54	WU_P53	WU_P52	WU_P51	WU_P50

Bits 7~0(WU_P57~WU_P50): Wake up function control for Port 5

0: Disable wake up function

1: Enable wake up function

6.3.25 Bank0 R21: P5WUECR (Port 5 Wake Up Edge Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUE_P57	WUE_P56	WUE_P55	WUE_P54	WUE_P53	WUE_P52	WUE_P51	WUE_P50

Bits 7~0(WUE_P57~WUE_P50): Wake up signal edge selection for Port 5.

0: Falling edge trigger

1: Rising edge trigger

6.3.26 Bank0 R22: P7WUCR (Port 7 Wake Up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WU_P77	WU_P76	WU_P75	WU_P74	WU_P73	WU_P72	WU_P71	WU_P70

Bits 7~0(WU_P77~WU_P70): Wake up function control for Port 7.

0: Disable wake up function

1: Enable wake up function

6.3.27 Bank0 R23: P7WUECR (Port 7 Wake Up Edge Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUE_P77	WUE_P76	WUE_P75	WUE_P74	WUE_P73	WUE_P72	WUE_P71	WUE_P70

Bits 7~0(WUE_P77~WUE_P70): Wake up signal edge selection for Port 7.

0: Falling edge trigger

1: Rising edge trigger

6.3.28 Bank0 R24~R2A (Not Used)

6.3.29 Bank0 R2B: SPICR (SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0

Bit 7 (CES): Clock Edge Select bit

0: Data shifts out on rising edge and shifts in on falling edge. Data is on hold during low-level.

1: Data shifts out on falling edge and shifts in on rising edge. Data is on hold during high-level.

Bit 6 (SPIE): SPI Enable bit

0: Disable SPI mode

1: Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0: No overflow

1: A new data is received while the previous data is still being held in the SPIR register. Under this condition, the data in the SPI Shift register will be destroyed. To avoid setting this bit, users are required to read the SPIR register although only transmission is implemented. This can only occur in Slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0: Reset as soon as shifting is completed and the next byte is ready to shift.

1: Start to shift and keep at "**1**" while the current byte is being transmitted.

Bit 3 (SDOC): SDO output status control bit

0: After Serial data output, the SDO remains high

1: After Serial data output, the SDO remains low

Bits 2~0 (SBRS2~SBRS0): SPI Baud Rate Select bits

SBRS2	SBRS1	SBRS0	Mode	SPI Baud Rate
0	**0**	**0**	Master	Fosc/2
0	**0**	**1**	Master	Fosc/4
0	**1**	**0**	Master	Fosc/8
0	**1**	**1**	Master	Fosc/16
1	**0**	**0**	Master	Fosc/32
1	**0**	**1**	Master	Fosc/64
1	**1**	**0**	Slave	/SS enable
1	**1**	**1**	Slave	/SS disable

6.3.30 Bank0 R2C: SPIS (SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	0	OD3	OD4	0	RBF

Bit 7 (DORD): Data transmission order

0: Shift left (MSB first)

1: Shift right (LSB first)

Bits 6~5 (TD1~TD0): SDO status output delay time options. When CPU oscillator source uses Fs, it delays 1 CLK time.

TD1	TD0	Delay Time
0	**0**	8 CLK
0	**1**	16 CLK
1	**0**	24 CLK
1	**1**	32 CLK

Bit 4: Not used, fixed to "**0**" all the time.

Bit 3(OD3): Open Drain control bit

0: Open drain disable for SDO

1: Open drain enable for SDO

Bit 2(OD4): Open Drain control bit

0: Open drain disable for SCK

1: Open drain enable for SCK

Bit 1: Not used, fixed to "**0**" all the time.

Bit 0 (RBF): Read Buffer Full flag

0: Receiving not completed, and SPIR has not fully exchanged data.

1: Receiving completed, and SPIR has fully exchanged data.

6.3.31 Bank0 R2D: SPIR (SPI Read Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0

Bits 7~0 (SRB7~SRB0): SPI Read Data Buffer

6.3.32 Bank0 R2E: SPIR (SPI Write Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0

Bits 7~0 (SWB7~SWB0): SPI Write Data Buffer

6.3.33 Bank0 R2F: WUCR1 (Wake Up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SPIWE	LVDWE	ICWE	0	CMP2WE	CMP1WE	EXWE

Bits 7: Not used, fixed to "**0**" all the time.

Bit 6 (SPIWE): SPI Wake-up enable bit. Applicable only when SPI works in Slave mode.

0: Disable SPI Wake up

1: Enable SPI Wake up.

Bit 5 (LVDWE): Low Voltage Detect Wake-up Enable bit

Bit 4 (ICWE): Port 6 Input Status Change Wake-up enable bit

0: Disable Port 6 input status change Wake-up

1: Enable Port 6 input status change Wake-up

When the Port 6 input status change is used to enter interrupt vector or to wake-up IC from Sleep/Idle mode, the ICWE bit must be set to "Enable".

Bit 3: Not used, fixed to "**0**" all the time.

Bits 2~1 (CMP2WE~CMP1WE): Comparator 2~1 Wake-up enable bits

0: Disable Comparator Wake-up

1: Enable Comparator Wake-up

When the Comparators 2~1 output status change is used to enter an interrupt vector or to Wake-up the IC from Sleep, the CMPWE bit must be set to "Enable".

Bit 0 (EXWE): External Interrupts Wake-up Function Enable bit

0: Disable external interrupt Wake-up

1: Enable external interrupt Wake-up

When the External Interrupt status changed is used to enter an interrupt vector or to Wake-up the IC from Sleep, the EXWE bits must be set to "Enable".

6.3.34 Bank0 R30~R31 (Not Used)

6.3.35 Bank0 R32: URCR1 (UART Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE

Bit 7 (URTD8): UART transmit data buffer 8th bit

Bits 6~5 (UMODE1~UMODE0): UART mode select bits

UMODE1	UMODE0	UART Mode
0	**0**	Mode1: 7-bit
0	**1**	Mode1: 8-bit
1	**0**	Mode1: 9-bit
1	**1**	Reserved

Bits 4~2 (BRAT2~BRAT0): Transmit baud rate selection

BRATE2	BRATE1	BRATE0	Baud Rate	8MHz
0	**0**	**0**	Fc/13	38400
0	**0**	**1**	Fc/26	19200
0	**1**	**0**	Fc/52	9600
0	**1**	**1**	Fc/104	4800
1	**0**	**0**	Fc/208	2400
1	**0**	**1**	Fc/416	1200
1	**1**	**0**	TC3	
1	**1**	**1**	Reserved	

Bit 1 (UTBE): UART transfer buffer empty flag. Set to "**1**" when transfer buffer is empty. Reset to "**0**" automatically when write into URTD register.

> **NOTE**
> *UTBE bit is cleared by hardware when transmission is enabled, and UTBE bit is read-only. Therefore, Write URTD register is necessary when you want to start shift transmitting.*

Bit 0 (TXE): Enable transmission

0: Disable transmission

1: Enable transmission

6.3.36 Bank0 R33: URCR2 (UART Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	SBIM1	SBIM0	UINVEN	0	0	0

Bits 7~6: Not used, fixed to "**0**" all the time.

Bits 5~4 (SBIM1~SBIM0): Serial bus interface operation mode select

SBIM1	SBIM0	Operation Mode
0	**0**	I/O mode
0	**1**	SPI mode
1	**0**	UART mode
1	**1**	I2C mode

Bit 3 (UINVEN): Enable UART TX and RX port inverse output

0: Disable TX and RX port inverse output

1: Enable TX and RX port inverse output

Bits 2~0: Not used, fixed to "**0**" all the time.

6.3.37 Bank0 R34: URS (UART Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE

Bit 7 (URRD8): UART receive data buffer 8th bit

Bit 6 (EVEN): Select parity check

0: Odd parity

1: Even parity

Bit 5 (PRE): Enable parity addition

0: Disable

1: Enable

Bit 4 (PRERR): Parity error flag. Set to "**1**" when parity error occurs and clear to "**0**" by software.

Bit 3 (OVERR): Over running error flag. Set to "**1**" when overrun error occurs and clear to "**0**" by software.

Bit 2 (FMERR): Framing error flag. Set to "**1**" when framing error occurs and clear to "**0**" by software.

Bit 1 (URBF): UART read buffer full flag. Set to "**1**" when one character is received. Reset to "**0**" automatically when read from URS register. URBF is cleared by hardware when Receive is enabled. The URBF bit is read-only. Therefore, read URS register is necessary to avoid overrun error.

Bit 0 (RXE): Enable Receive

0: Disable Receive

1: Enable Receive

6.3.38 Bank0 R35: URRD (UART Receive Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0

Bits 7~0 (URRD7~URRD0): UART receive data buffer. Read only.

6.3.39 Bank0 R36: URTD (UART Transmit Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0

Bits 7~0 (URTD7~URTD0): UART transmit data buffer. Write only.

6.3.40 Bank0 R37: TBPTL (Table Point Low Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0

Bits 7~0 (TB7~TB0): Table point address Bits 7~0

6.3.41 Bank0 R38: TBPTH (Table Point High Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	GP1	GP0	TB12	TB11	TB10	TB9	TB8

Bit 7 (HLB): Take MLB or LSB at machine code

Bits 6~5 (GP1~GP0): General purpose read/write bits

Bits 4~0: Table point address Bits 12~8.

6.3.42 Bank0 R39: CMP1CR (Comparator 1 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C1RS	CP1OUT	CMP1COS1	CMP1COS0	CP1NS	CP1PS	CP1NRE	CP1NRDT

Bit 7 (C1RS): Comparator input reference source select bit

0: CIN1+ source external

1: CIN1+ source internal

Bit 6 (CP1OUT): The result of comparator output

Bits 5~4(CMP1COS1~CMP1COS0): Comparator 1/OP1 select bits

0	0	Comparator 1 not used. P70, P71, & P72 act as normal I/O pin
0	1	P71 & P72 function as Comparator 1 input pin and P70 functions as normal I/O pin
1	0	P71 & P72 function as Comparator 1 input pin and P70 functions as Comparator 1 output pin (CO1).
1	1	Reserved

Bit 3 (CP1NS): Negative end of Comparator 1 is connected to ground.

0: Disable, P72/CIN1- functions as CIN1-.

1: Enable, P72/CIN1- functions as P72

Bit 2 (CP1PS): Positive end of Comparator 1 is connected to ground.

0: Disable, P71/CIN1+ functions as CIN1+.

1: Enable, P71/CIN1+ functions as P71

Bit 1 (CP1NRE): Noise Rejection Enable bit for Comparator 1

0: Disable noise rejection

1: Enable noise rejection (default)

NOTE

In Low Crystal 2 Oscillator (LXT2) mode, Green mode, and Idle mode, the noise rejection circuits are always disabled.

Bit 0 (CP1NRDT): Comparator 1 Noise Rejection Delay Time.

In Low XTAL1 oscillator (LXT1) mode, the noise rejection high/low pulse is always 4/Fm.

0: Comparator 1 output H/L pulse equal to 4/Fm (0.5us at 8MHz) is considered as signal.

1: Comparator 1 output H/L pulse equal to 8/Fm (1us at 8MHz) is considered as signal.

6.3.43 Bank0 R3A~R3B: (Not Used)

6.3.44 Bank0 R3C: CMP2CR (Comparator 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C2RS	CP2OUT	CMP2COS1	CMP2COS0	CP2NS	CP2PS	CP2NRE	CP2NRDT

Bit 7 (C2RS): Comparator 2 input reference source select bit

0: CIN2+ source external

1: CIN2+ source internal

Bit 6 (CP2OUT): The result of Comparator 2 output

Bits 5~4 (CMP1COS1~CMP1COS0): Comparator 2/OP2 select bits

CMP2COS1	CMP2COS0	Function Description
0	0	Comparator2 not used. P80, P81, P82 act as normal I/O pin
0	1	P81, P82, act as an Comparator2 input pin and P80 acts as normal I/O pin
1	0	P81, P82 act as an Comparator2 input pin and P80 acts as Comparator2 output pin (CO2).
1	1	reserved

Bit 3 (CP2NS): Negative end of Comparator 2 is connected to ground.

0: disable, P82/CIN2- as CIN2-.

1: enable, P82/CIN2- as P82

Bit 2 (CP2PS): Positive end of Comparator 2 is connected to ground.

0: disable, P81/CIN2+ as CIN2+.

1: enable, P81/CIN2+ as P81

Bit 1 (CP2NRE): Noise Rejection Enable bit for Comparator 2

0: Disable noise rejection

1: Enable noise rejection (default). But in Low Crystal 2 Oscillator (LXT2) mode, Green mode, and Idle mode, the noise rejection circuits are always disabled.

Bit 0 (CP2NRDT): Comparator 2 Noise Rejection Delay Time.

In Low XTAL1 oscillator (LXT1) mode, the noise rejection high/low pulse is always 4/Fm.

0: Comparator1 output H/L pulse equal to 4/Fm (0.5us at 8MHz) is considered as signal.

1: Comparator1 output H/L pulse equal to 8/Fm (1us at 8MHz) is considered as signal.

6.3.45 Bank0 R3D~R42: (Not Used)

6.3.46 Bank0 R43: CPIRLCON (Comparator Internal Reference Level Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BG2OUT	C2IRL2	C2IRL1	C2IRL0	BG1OUT	C1IRL2	C1IRL1	C1IRL0

Bit 7 (BG2OUT): When this bit set to "**1**", Pin P83 will output the bandgap reference voltage.

Bits 6~4 (C2IRL2~C2IRL0): Comparator 2 internal reference level

Bit 3 (BG1OUT): When this bit set to "**1**", Pin P73 will output the bandgap reference voltage

Bits 2~0 (C1IRL2~C1IRL0): Comparator 1 internal reference level

CxIRL2	CxIRL1	CxIRL0	Voltage Level(V)
0	**0**	**0**	0.5
0	**0**	**1**	0.8
0	**1**	**0**	1.0
0	**1**	**1**	1.5
1	**0**	**0**	2.0
1	**0**	**1**	2.2
1	**1**	**0**	2.5
1	**1**	**1**	3.0

6.3.47 Bank0 R44~R47: (Not Used)

6.3.48 Bank0 R48: TC1CR (Timer 1 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1CAP	TC1S	TC1CK1	TC1CK0	TC1M	TC1ES	0	0

Bit 7 (TC1CAP): Software capture control

0: Software capture control disabled

1: Software capture control enabled

Bit 6 (TC1S): Timer/Counter 1 start control

0: Stop and clear counter

1: Start timer/counter

Bits 5~4(TC1CK1~TC1CK0): Timer/Counter 1 clock source select bits

TC1CK1	TC1CK0	Clock Source	Resolution 8MHZ	Max time 8MHz	Resolution 16KHZ	Max time 16KHz
		Normal	FC=8M	FC=8M	FC=16K	FC=16K
0	0	FC/2^{12}	512μS	131072μS	256ms	65536ms
0	1	FC/2^{10}	128μS	32768μS	64ms	16384ms
1	0	FC/2^{7}	16μS	4096μS	8ms	2048ms
1	1	External clock (TC1 pin)	-	-	-	-

Bit 3 (TC1M): Timer/Counter 1 mode select

0: Timer/Counter 1 mode

1: Capture mode

Bit 2 (TC1ES): Timer/Counter 1 signal edge

0: Increment if the transition from low to high (rising edge) take place on TC1 pin.

1: increment if the transition from high to low (falling edge) take place on TC1 pin.

Bits 1~0: Not used, fixed to "**0**" all the time.

■ **Timer/Counter 1 Configuration**

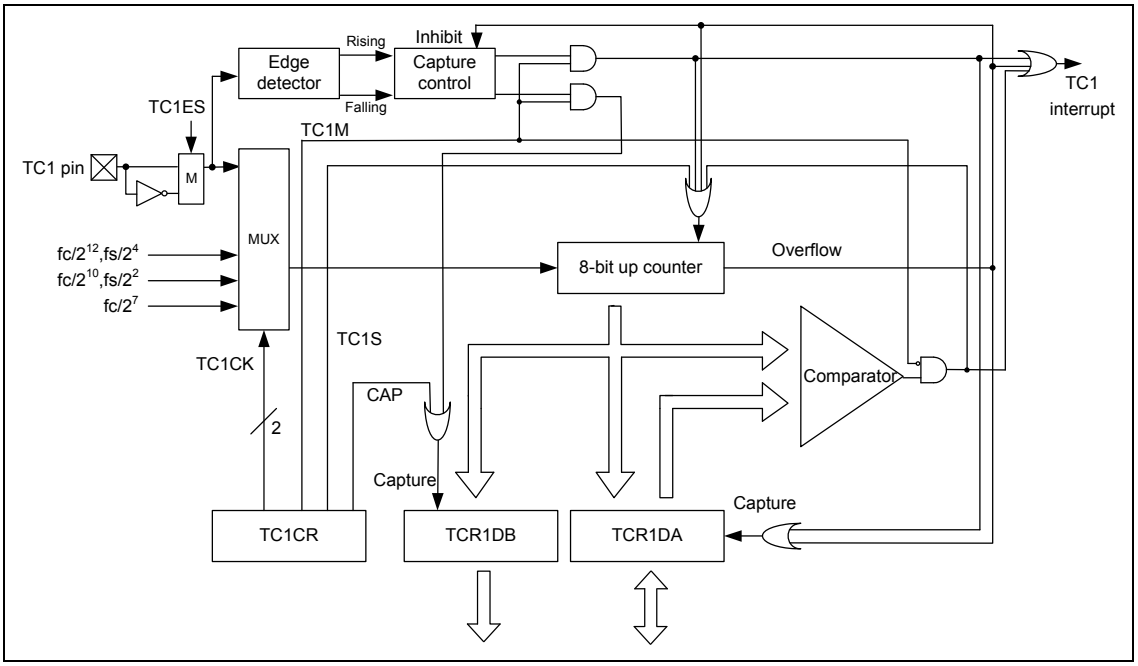


Figure 6-8a Timer/Counter1 Configuration Block Diagram

In Timer mode, counting up is performed using internal clock. When the contents of up-counter match the TCR1DA, the interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of up-counter are loaded into TCR1DB by setting TC1CAP to "**1**" and the TC1CAP is cleared to "**0**" after capture is completed automatically.

In Counter mode, counting up is performed using external clock input pin (TC1 pin) and either rising or falling edge can be selected by TC1ES, but **both edges can not be used**. When the contents of up-counter match the TCR1DA, the interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of up-counter are loaded into TCR1DB by setting TC1CAP to "**1**" and the TC1CAP is cleared to "**0**" after capture is completed automatically.

In Capture mode, the pulse width, period, and duty of the TC1 input pin are measured under this mode to decode the remote control signal. The counter is made free running by the internal clock. On the rising (falling) edge of TC1 pin input, the contents of counter are loaded into TCR1DA, then the counter is cleared and the interrupt is generated. On the falling (rising) edge of TC1 pin input, the contents of counter are loaded into TCR1DB. At the next rising edge of TC1 pin input while the counter is still counting, the contents of counter are loaded into TCR1DA. Then the counter is cleared and the interrupt is generated again. If an overflow is detected before the edge, the FFH is loaded into TCR1DA and the overflow interrupt is generated. During the interrupt process, you can check and determine an overflow has occurred by checking the TCR1DA value is FFH. After an interrupt (capture to TCR1DA or overflow detected) is generated, capture and overflow detection are halted until TCR1DA is read out.

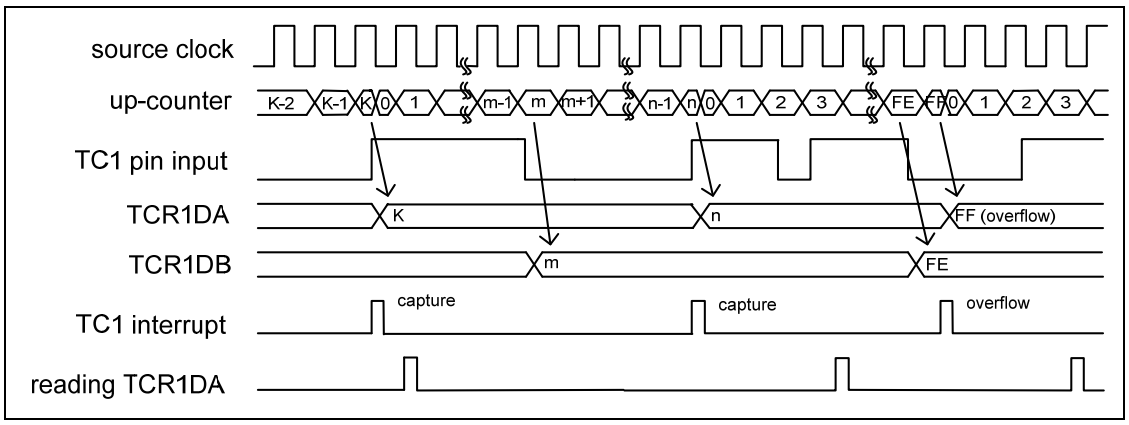


Figure 6-8b Capture Mode Timing Diagram

6.3.49 Bank0 R49: TCR1DA (Timer 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR1DA7	TCR1DA6	TCR1DA5	TCR1DA4	TCR1DA3	TCR1DA2	TCR1DA1	TCR1DA0

Bits 7~0 (TCR1DA7~TCR1DA0): 8-bit Timer/Counter 1 of Data Buffer A

6.3.50 Bank0 R4A: TCR1DB (Timer 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR1DB7	TCR1DB6	TCR1DB5	TCR1DB4	TCR1DB3	TCR1DB2	TCR1DB1	TCR1DB0

Bits 7~0 (TCR1DB7~TCR1DB0): 8-bit Timer/Counter 1 of Data Buffer B

6.3.51 Bank0 R4B: TC2CR (Timer 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0

Bits 7~6: Not used, fixed to "**0**" all the time.

Bit 5 (TC2ES): TC2 signal edge

0: Increment if the transition from low to high (rising edge) takes place on TC2 pin

1: Increment if the transition from high to low (falling edge) takes place on TC2 pin

Bit 4 (TC2M): Timer/Counter2 mode select

0: Timer/Counter 2 mode

1: Window mode

Bit 3 (TC2S): Timer/Counter 2 start control

0: Stop and clear counter

1: Start timer/counter

Bits 2~0 (TC2CK2~TC2CK0): Timer/Counter 2 clock source select

TC2CK2	TC2CK1	TC1CK0	CLOCK SOURCE	Resolution 8MHZ	Max time 8MHz	Resolution 16KHZ	Max time 16KHz
			Normal	F_C=8M	F_C=8M	F_C=16K	F_C=16K
0	0	0	$F_C/2^{23}$	1.05s	19.1hr	145hr	9544hr
0	0	1	$F_C/2^{13}$	1.024ms	66.21s	512ms	33554.432s
0	1	0	$F_C/2^8$	32µs	2.097s	16ms	1048.576s
0	1	1	$F_C/2^3$	1µs	65.536ms	0.5ms	32768ms
1	0	0	F_C	125ns	8.192ms	0.0625ms	4096ms
1	0	1	-	-	-	-	-
1	1	0	-	-	-	-	-
1	1	1	External clock (TC2 pin)	-	-	-	-

■ **Timer/Counter 2 Configuration**

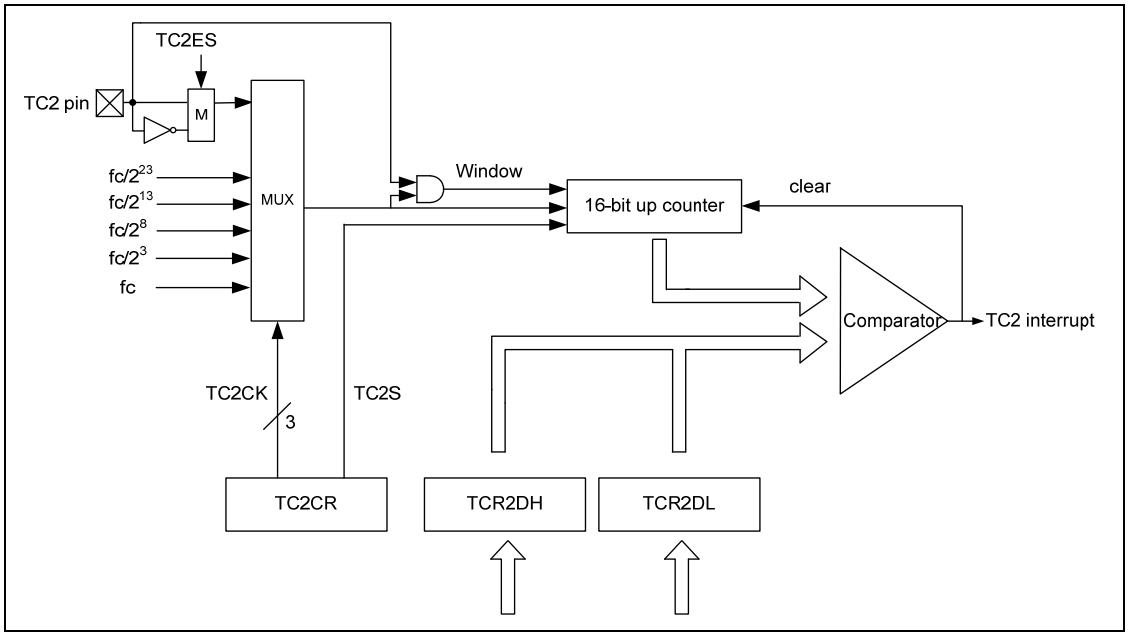


Figure 6-9a Timer/Counter2 Configuration Block Diagram

In Timer mode, counting up is performed using internal clock. When the contents of up-counter match the TCR2 (TCR2H+TCR2L), the interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared.

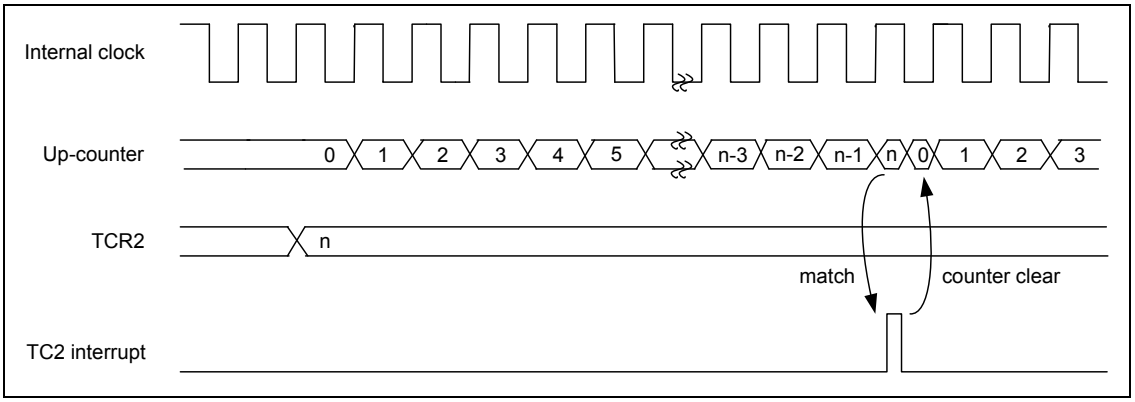


Figure 6-9b Timer Mode Timing Diagram

In Counter mode, counting up is performed using external clock input pin (TC2 pin) and either rising or falling edge can be select by setting TC2ES. When the contents of up-counter match the TCR2 (TCR2H+TCR2L), the interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared.

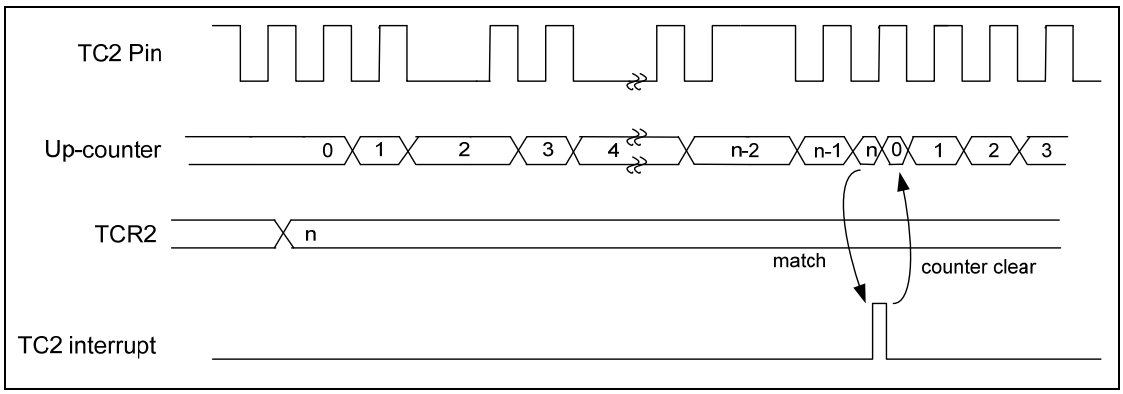


Figure 6-9c Counter Mode Timing (INT2ES = 1) Diagram

In Window mode, counting up is performed on rising edge of the pulse that is logical AND of an internal clock and of the TC2 pin (window pulse). When the contents of up-counter match the TCR2 (TCR2H+TCR2L), the interrupt is then generated and the counter is cleared. **The frequency (window pulse) must be slower than the selected internal clock.**

When writing to the TCR2L, the comparison is inhibited until TCR2H is written.

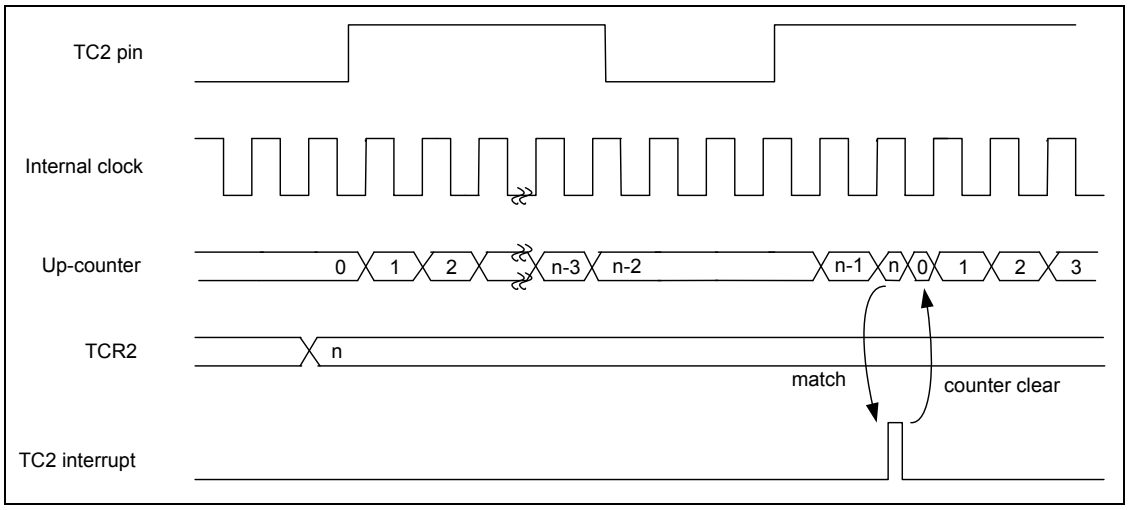


Figure 6-9d Window Mode Timing Diagram

6.3.52 Bank0 R4C: TCR2DH (Timer 2 High Byte Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR2D15	TCR2D14	TCR2D13	TCR2D12	TCR2D11	TCR2D10	TCR2D9	TCR2D8

Bits 7~0 (TCR2D15~ TCR2D8): 16-bit Timer/Counter 2 of high byte data buffer

6.3.53 Bank0 R4D: TCR2DL (Timer 2 Low Byte Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR2D7	TCR2D6	TCR2D5	TCR2D4	TCR2D3	TCR2D2	TCR2D1	TCR2D0

Bits 7~0 (TCR2D7~ TCR2D0): 16-bit Timer/Counter 2 of low byte data buffer

6.3.54 Bank0 R4E: TC3CR (Timer 3 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bits 7~6 (TC3FF1~TC3FF0): Timer/Counter 3 flip-flop control

TC3FF1	TC3FF0	Operating Mode
0	0	*Clear*
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5 (TC3S): Timer/Counter 3 start control

0: Stop and clear counter

1: Start timer/counter

Bits 4~2 (TC3CK2~TC3CK0): Timer/Counter 3 clock source select

TC3CK2	TC3CK1	TC3CK0	CLOCK Source	Resolution 8MHZ	Max Time 8MHz	Resolution 16KHZ	Max Time 16KHz
			Normal	FC=8M	FC=8M	FC=16K	FC=16K
0	0	0	FC/211	256µs	65536µs	128ms	32768ms
0	0	1	FC/27	16µs	4096µs	8ms	2048ms
0	1	0	FC/25	4µs	1024µs	2ms	512ms
0	1	1	FC/23	1µs	256µs	500µs	128ms
1	0	0	FC/22	500ns	128µs	250µs	64ms
1	0	1	FC/2	250ns	64µs	125µs	32ms
1	1	0	FC	125ns	32µs	62.5µs	16ms
1	1	1	External clock (TC3 pin)	-	-	-	-

Bits 1~0(TC3M1~TC3M0): Timer/Counter 3 operation mode select.

TC3M1	TC3M0	Operating Mode
0	0	Timer/Counter
0	1	Reserved
1	0	Programmable Divider output
1	1	Pulse Width Modulation output

■ **Timer/Counter 3 Configuration**

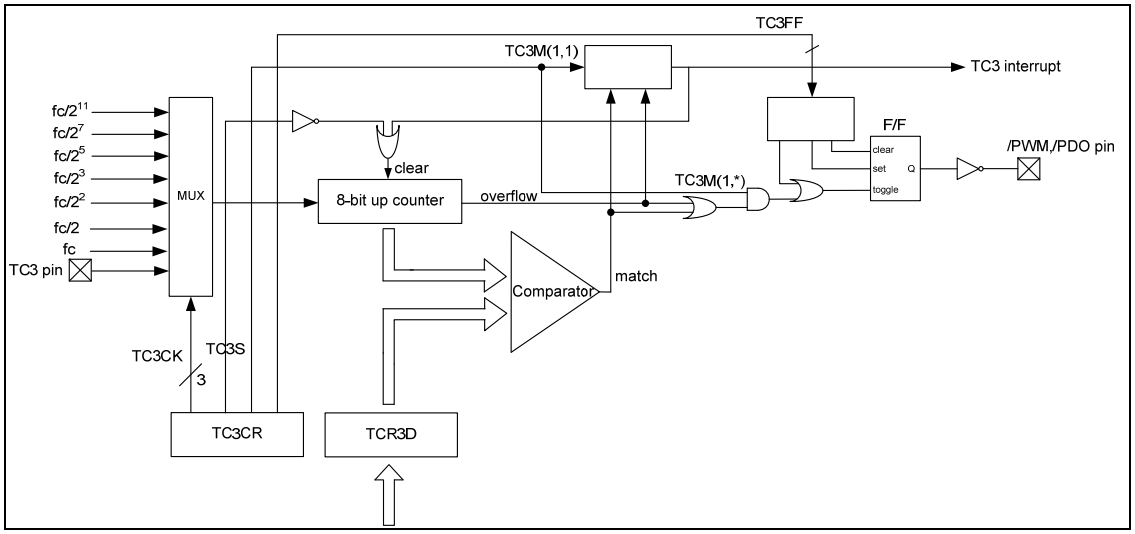


Figure 6-10a Timer/Counter3 Configuration Block Diagram

In Timer mode, counting up is performed using the internal clock (rising edge trigger). When the contents of up-counter match the TCR3D, the interrupt is generated and the counter is then cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using the external clock input pin (TC3 pin). When the contents of up-counter match the TCR3D, interrupt is generated and the counter is then cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3D are compared with the contents of up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by program and it is initialized to "0" during reset**. A TC3 interrupt is generated each time the /PDO output is toggled.

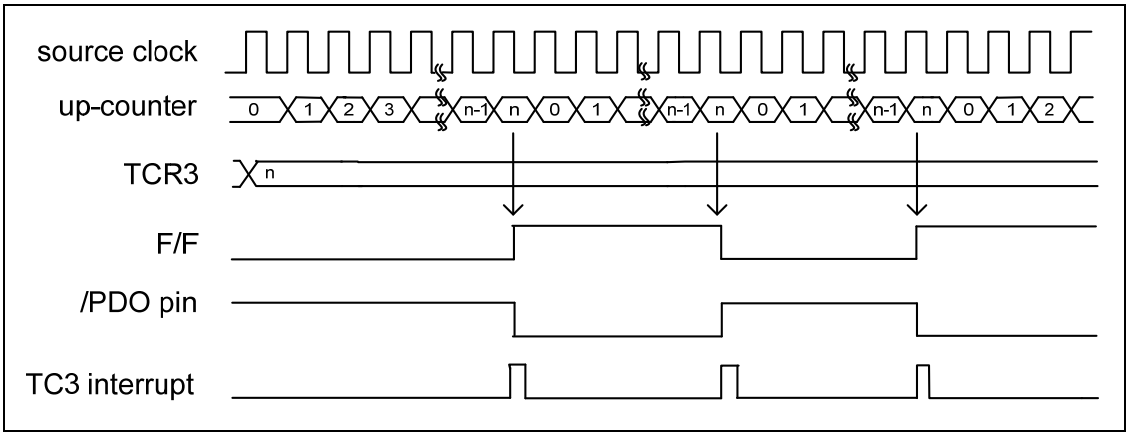


Figure 6-10b PDO Mode Timing Diagram

In Pulse Width Modulation (PWM) Output mode, counting up is performed using internal clock. The contents of TCR3 are compared with the contents of up-counter. The F/F is toggled when match is found. While the counter continues counting, the F/F is toggled again when counter overflow occurs, then counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as 2-stage shift register and, during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Therefore, the output can be changed continuously. TRC3 is also shifted for the first time by setting TC3S to "**1**" after data is loaded to TCR3.

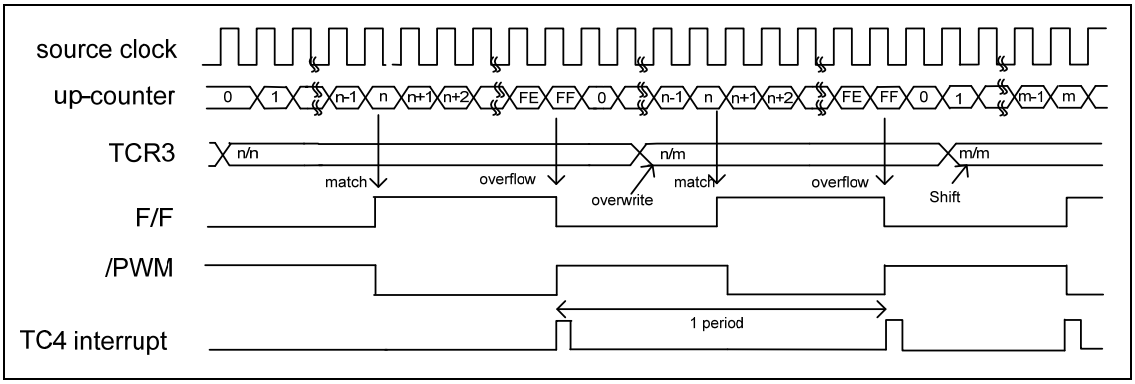


Figure 6-10c PWM Mode Timing Diagram

6.3.55 Bank0 R4F: TCR3D (Timer 3 Duty Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR3D7	TCR3D6	TCR3D5	TCR3D4	TCR3D3	TCR3D2	TCR3D1	TCR3D0

Bits 7~0(TCR3DB7~TCR13DB0): 8-bit Timer/Counter 3 of duty data buffer

6.3.56 Bank1 R5: P5PHCR (Port 5 Pull High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50

Bit 7 (/PH57): Control bit used to enable the pull high of P57 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH56): Control bit used to enable the pull high of P56 pin

Bit 5 (/PH55): Control bit used to enable the pull high of P55 pin

Bit 4 (/PH54): Control bit used to enable the pull high of P54 pin

Bit 3 (/PH53): Control bit used to enable the pull high of P53 pin

Bit 2 (/PH52): Control bit used to enable the pull high of P52 pin

Bit 1 (/PH51): Control bit used to enable the pull high of P51 pin

Bit 0 (/PH50): Control bit used to enable the pull high of P50 pin

6.3.57 Bank1 R6: P6PHCR (Port 6 Pull High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

Bit 7 (/PH67): Control bit used to enable the pull high of P67 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH66): Control bit used to enable the pull high of P66 pin

Bit 5 (/PH65): Control bit used to enable the pull high of P65 pin

Bit 4 (/PH64): Control bit used to enable the pull high of P64 pin

Bit 3 (/PH63): Control bit used to enable the pull high of P63 pin

Bit 2 (/PH62): Control bit used to enable the pull high of P62 pin

Bit 1 (/PH61): Control bit used to enable the pull high of P61 pin

Bit 0 (/PH60): Control bit used to enable the pull high of P60 pin

6.3.58 Bank1 R7: P7PHCR (Port 7 Pull High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	/PH71	/PH70

Bit 7 (/PH77): Control bit used to enable the pull high of P77 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH76): Control bit used to enable the pull high of P76 pin

Bit 5 (/PH75): Control bit used to enable the pull high of P75 pin

Bit 4 (/PH74): Control bit used to enable the pull high of P74 pin

Bit 3 (/PH73): Control bit used to enable the pull high of P73 pin

Bit 2 (/PH72): Control bit used to enable the pull high of P72 pin

Bit 1 (/PH71): Control bit used to enable the pull high of P71 pin

Bit 0 (/PH70): Control bit used to enable the pull high of P70 pin

6.3.59 Bank1 R8: P8PHCR (Port 8 Pull High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH87	/PH86	/PH85	/PH84	/PH83	/PH82	/PH81	/PH80

Bit 7 (/PH87): Control bit used to enable the pull high of P87 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH86): Control bit used to enable the pull high of P86 pin

Bit 5 (/PH85): Control bit used to enable the pull high of P85 pin

Bit 4 (/PH84): Control bit used to enable the pull high of P84 pin

Bit 3 (/PH83): Control bit used to enable the pull high of P83 pin

Bit 2 (/PH82): Control bit used to enable the pull high of P82 pin

Bit 1 (/PH81): Control bit used to enable the pull high of P81 pin

Bit 0 (/PH80): Control bit used to enable the pull high of P80 pin

6.3.60 Bank1 R9: P9PHCR (Port 9 Pull High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH97	/PH96	/PH95	/PH94	/PH93	/PH92	/PH91	/PH90

Bit 7 (/PH97): Control bit used to enable the pull high of P97 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH96): Control bit used to enable the pull high of P96 pin

Bit 5 (/PH95): Control bit used to enable the pull high of P95 pin

Bit 4 (/PH94): Control bit used to enable the pull high of P94 pin

Bit 3 (/PH93): Control bit used to enable the pull high of P93 pin

Bit 2 (/PH92): Control bit used to enable the pull high of P92 pin

Bit 1 (/PH91): Control bit used to enable the pull high of P91 pin

Bit 0 (/PH90): Control bit used to enable the pull high of P90 pin

6.3.61 Bank1 RA (Not Used)

6.3.62 Bank1 RB: P5PLCR (Port 5 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL57	/PL56	/PL55	/PL54	/PL53	/PL52	/PL51	/PL50

Bit 7 (/PL57): Control bit used to enable the pull low of P57 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PL56): Control bit used to enable the pull low of P56 pin

Bit 5 (/PL55): Control bit used to enable the pull low of P55 pin

Bit 4 (/PL54): Control bit used to enable the pull low of P54 pin

Bit 3 (/PL53): Control bit used to enable the pull low of P53 pin

Bit 2 (/PL52): Control bit used to enable the pull low of P52 pin

Bit 1 (/PL51): Control bit used to enable the pull low of P51 pin

Bit 0 (/PL50): Control bit used to enable the pull low of P50 pin

6.3.63 Bank1 RC: P6PLCR (Port 6 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL67	/PL66	/PL65	/PL64	/PL63	/PL62	/PL61	/PL60

Bit 7 (/PL67): Control bit used to enable the pull low of P67 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PL66): Control bit used to enable the pull low of P66 pin

Bit 5 (/PL65): Control bit used to enable the pull low of P65 pin

Bit 4 (/PL64): Control bit used to enable the pull low of P64 pin

Bit 3 (/PL63): Control bit used to enable the pull low of P63 pin

Bit 2 (/PL62): Control bit used to enable the pull low of P62 pin

Bit 1 (/PL61): Control bit used to enable the pull low of P61 pin

Bit 0 (/PL60): Control bit used to enable the pull low of P60 pin

6.3.64 Bank1 RD: P7PLCR (Port 7 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL77	/PL76	/PL75	/PL74	/PL73	/PL72	/PL71	/PL70

Bit 7 (/PL77): Control bit used to enable the pull low of P77 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PL76): Control bit used to enable the pull low of P76 pin

Bit 5 (/PL75): Control bit used to enable the pull low of P75 pin

Bit 4 (/PL74): Control bit used to enable the pull low of P74 pin

Bit 3 (/PL73): Control bit used to enable the pull low of P73 pin

Bit 2 (/PL72): Control bit used to enable the pull low of P72 pin

Bit 1 (/PL71): Control bit used to enable the pull low of P71 pin

Bit 0 (/PL70): Control bit used to enable the pull low of P70 pin

6.3.65 Bank1 RE: P8PLCR (Port 8 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL87	/PL86	/PL85	/PL84	/PL83	/PL82	/PL81	/PL80

Bit 7 (/PL87): Control bit used to enable the pull low of P87 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PL86): Control bit used to enable the pull low of P86 pin

Bit 5 (/PL85): Control bit used to enable the pull low of P85 pin

Bit 4 (/PL84): Control bit used to enable the pull low of P84 pin

Bit 3 (/PL83): Control bit used to enable the pull low of P83 pin

Bit 2 (/PL82): Control bit used to enable the pull low of P82 pin

Bit 1 (/PL81): Control bit used to enable the pull low of P81 pin

Bit 0 (/PL80): Control bit used to enable the pull low of P80 pin

6.3.66 Bank1 RF: P9PLCR (Port 9 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL97	/PL96	/PL95	/PL94	/PL93	/PL92	/PL91	/PL90

Bit 7 (/PL97): Control bit used to enable the pull low of P97 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PL96): Control bit used to enable the pull low of P96 pin

Bit 5 (/PL95): Control bit used to enable the pull low of P95 pin

Bit 4 (/PL94): Control bit used to enable the pull low of P94 pin

Bit 3 (/PL93): Control bit used to enable the pull low of P93 pin

Bit 2 (/PL92): Control bit used to enable the pull low of P92 pin

Bit 1 (/PL91): Control bit used to enable the pull low of P91 pin

Bit 0 (/PL90): Control bit used to enable the pull low of P90 pin

6.3.67 Bank1 R10 (Not Used)

6.3.68 Bank1 R11: P5HD/SCR (Port 5 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H57	/H56	/H55	/H54	/H53	/H52	/H51	/H50

Bits 7~0 (H57~H50): P57~P50 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.3.69 Bank1 R12: P6HD/SCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H67	/H66	/H65	/H64	/H63	/H62	/H61	/H60

Bits 7~0 (H67~H60): P67~P60 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.3.70 Bank1 R13: P7HD/SCR (Port 7 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H77	/H76	/H75	/H74	/H73	/H72	/H71	/H70

Bits 7~0 (H77~H70): P77~P70 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.3.71 Bank1 R14: P8HD/SCR (Port 8 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H87	/H86	/H85	/H84	/H83	/H82	/H81	/H80

Bits 7~0 (H87~H80): P87~P80 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.3.72 Bank1 R15: P9HD/SCR (Port 9 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H97	/H96	/H95	/H94	/H93	/H92	/H91	/H90

Bits 7~0 (H97~H90): P97~P90 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.3.73 Bank1 R16 (Not Used)

6.3.74 Bank1 R17: P5ODCR (Port 5 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50

Bits 7~0 (OD57~OD50): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.3.75 Bank1 R18: P6ODCR (Port 6 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60

Bits 7~0 (OD67~OD60): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.3.76 Bank1 R19: P7ODCR (Port 7 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD77	OD76	OD75	OD74	OD73	OD72	OD71	OD70

Bits 7~0 (OD77~OD70): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.3.77 Bank1 R1A: P8ODCR (Port 8 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD87	OD86	OD85	OD84	OD83	OD82	OD81	OD80

Bits 7~0 (OD87~OD80): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.3.78 Bank1 R1B: P9ODCR (Port 9 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD97	OD96	OD95	OD94	OD93	OD92	OD91	OD90

Bits 7~0 (OD97~OD90): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.3.79 Bank1 R1C (Not Used)

6.3.80 Bank1 R1D: IRCS (IRC Frequency Selection Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	RCM1	RCM0	0	0	0	0

Bits 7~6: Not used, fixed to "**0**" all the time.

Bits 5~4 (RCM1 ~ RCM0): IRC Mode Frequency select bits

RCM 1	RCM 0	Frequency(MHz)
0	**0**	4
0	**1**	16
1	**0**	8
1	**1**	455kHz

WORD1 COBS0 = 0: The R1D<5,4> of the initialized values will keep the same as WORD1<6,5>.

The R1D<5,4> can't be changed.

WORD1 COBS0 = 1: The R1D<5,4> of the initialized values will keep the same as WORD1<6,5>.

The R1D<5,4> can be changed if you want to work on other IRC frequency.

Ex**:** 4M →16M

Bits 3~0: Not used, fixed to "**0**" all the time.

6.3.81 Bank1 R1E (Not Used)

6.3.82 Bank1 R1F: EEPROM CONTROL

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	0	0	0

Bit 7 (RD): Read control bit

0: Don't execute EEPROM read

1: Read EEPROM contents (RD can be set by software. When Read instruction is completed, RD will be cleared by hardware.)

Bit 6 (WR): Write control bit

0: Write cycle to the EEPROM is completed.

1: Initiate a Write cycle (WR can be set by software. When Write cycle is completed, WR will be cleared by hardware.)

Bit 5 (EEWE): EEPROM Write enable bit

0: Prohibit Write to the EEPROM

1: Allow EEPROM Write cycles

Bit 4 (EEDF): EEPROM Detect flag

0: Write cycle is completed

1: Write cycle is uncompleted

Bit 3 (EEPC): EEPROM power down control bit

0: Switch OFF EEPROM

1: EEPROM is operating

Bits 2~0: Not used, fixed to "**0**" all the time.

NOTE

EM78F548N *currently does not support EEPROM function. Therefore, the corresponding control registers (Bank1 R1F~R21) are reserved.*

6.3.83 Bank1 R20: EEPROM ADDR

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EERA7	EERA6	EERA5	EERA4	EERA3	EERA2	EERA1	EERA0

Bits 7~0 (EERA7~EERA0): EEPROM address register

NOTE

EM78F548N *currently does not support EEPROM function. Therefore, the corresponding control registers (Bank1 R1F~R21) are reserved.*

6.3.84 Bank1 R21: EEPROM DATA

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EERD7	EERD6	EERD5	EERD4	EERD3	EERD2	EERD1	EERD0

Bits 7~0 (EERD7~EERD0): EEPROM data register. Read only.

NOTE

EM78F548N *currently does not support EEPROM function. Therefore, the corresponding control registers (Bank1 R1F~R21) are reserved.*

6.3.85 Bank1 R22 (Not Used)

6.3.86 Bank1 R23: I2CCR1 (I2C Status and Control Register1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY

Bit 7 (Strobe/Pend): In Master mode, it is used as strobe signal to control I2C circuit in sending SCL clock. Automatically resets after receiving or transmitting handshake signal (ACK or NACK). In Slave mode, it is used as pending signal. You should clear it after filling data into Tx buffer or taking data from Rx buffer to inform the Slave I2C circuit to release SCL signal.

Bit 6 (IMS): I2C Master/Slave mode select bit.

0: Slave

1: Master

Bit 5 (ISS): I2C Fast/Standard mode select bit (If Fm is 4MHz and I2CTS1~0<0,0>)

0: Standard mode (100K bit/s)

1: Fast mode (400K bit/s)

Bit 4 (SOTP): In Master mode, if STOP=1 and R/nW=1, then EM78F648N/F548N must return nACK signal to Slave device before sending STOP signal. If STOP=1 and R/nW=0, then EM78F648N/F548N sends STOP signal after receiving an ACK signal. Resets when EM78F648N/F548N sends STOP signal to Slave device.
In Slave mode, if STOP=1 and R/nW=0, then EM78F648N/F548N must return nACK signal to Master device.

Bit 3 (SAR_EMPTY): Set when EM78F648N/F548N transmits 1 byte data from I2C Slave Address Register and receive ACK (or nACK) signal. Resets when MCU writes 1 byte data to I2C Slave Address Register.

Bit 2 (ARK): The Ack condition bit is set to "**1**" by hardware when the device responds acknowledge (ACK). Resets when the device responds with a "not-acknowledge" (nACK) signal.

Bit 1 (FULL): Set by hardware when I2C Receive (Rx) Buffer register is full. Resets by hardware when MCU reads data from I2C Receive (Rx) Buffer register.

Bit 0 (EMPTY): Set by hardware when I2C Transmit (Tx) Buffer register is empty and receive ACK (or nACK) signal. Reset by hardware when MCU writes new data to I2C Transmit (Tx) Buffer register.

6.3.87 Bank1 R24: I2CCR2 (I2C Status and Control Register2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CBF	GCEN	0	0	I2CTS1	I2CTS0	0	I2CEN

Bit 7 (I2CBF): I2C Busy Flag bit

0: Clear to "**0**" under Slave mode if the received STOP signal or I2C Slave address does not match.

1: Set when I2C communicate with Master in Slave mode.

Bit 6 (GCEN): I2C General Call Function Enable bit

0: Disable General Call Function

1: Enable General Call Function

Bits 5~4: Not used, fixed to "**0**" all the time.

Bits 3~2 (I2CTS1~I2CTS0): I2C Transmit Clock Source Select bits (When I2CCS=0). When operating under different Fm, these bits must be set to correct value to let SCL clock match with Standard/Fast mode.

I2CCR1 Bit5=0, Standard mode**:**

I2CTS1	I2CTS0	SCL CLK	Operating Fm(MHz)
0	**0**	Fm/40	4
0	**1**	Fm/80	8
1	**0**	Fm/120	12
1	**1**	Fm/160	16

I2CCR1 Bit5=1, Fast mode**:**

I2CTS1	I2CTS0	SCL CLK	Operating Fm(MHz)
0	**0**	Fm/10	4
0	**1**	Fm/20	8
1	**0**	Fm/30	12
1	**1**	Fm/40	16

Bit 1: Not used, fixed to "**0**" all the time.

Bit 0 (I2CEN): I2C Enable Bit

0: Disable I2C mode

1: Enable I2C mode

6.3.88 Bank1 R25: I2CSA (I2C Slave Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW

Bits 7~1 (SA6~SA0): When EM78F648N/F548N is used as Master device for I2C application, this is the Slave device address register.

Bit 0 (IRW): When EM78F648N is used as Master device for I2C application, this bit is Read/Write transaction control bit.

0: Write

1: Read

6.3.89 Bank1 R26: I2CDA (I2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Bits 7~0 (DA7~DA0): When EM78F648N/F548N is used as Slave device for I2C application, this register stores the address of EM78F648N/F548N. It is used to identify the data on the I2C bus and to extract the message delivered to the EM78F648N/F548N.

6.3.90 Bank1 R27: I2CDB (I2C Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Bits 7~0 (DB7~DB0): I2C Receive/Transmit Data Buffer.

6.3.91 Bank1 R28: I2CA (I2C Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	DA9	DA8

Bits 7~2: Not used, fixed to "**0**" all the time.

Bits 1~0 (DA9~DA8): Device Address high bits

6.3.92 Bank1 R29 (Not Used)

6.3.93 Bank1 R2A: PWMER (PWM Enable Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	PWMBE	PWMAE

Bits 7~2: Not used, fixed to "**0**" all the time.

Bit 1 (PWMBE): PWM B Enable bit

0: PWM B is off (default value), and its related Pin P52 carries out I/O pin function.

1: PWM B is on, and its related pin is automatically set to output.

Bit 0 (PWMAE): PWM A Enable bit

0: PWM A is OFF (default value), and its related pin carries out I/O pin function.

1: PWM A is ON, and its related pin is automatically set to output.

6.3.94 Bank1 R2B: TIMEN (Timer/PWM Enable Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	TBEN	TAEN

Bits 7~2: Not used, fixed to "**0**" all the time.

Bit 1 (TBEN): Timer B enable bit

0: Timer B is off (Default)

1: Timer B is on

Bit 0 (TAEN): Timer A enable bit

0: Timer A is off (Default)

1: Timer A is on

6.3.95 Bank1 R2C~R2E: (Not Used)

6.3.96 Bank1 R2F: PWMACR (PWM A Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	TRCBA	0	0	0

Bits 7~4: Not used, fixed to "**0**" all the time.

Bit 3(TRCBA): Timer A Read Control bit

0: When this bit set to "**0**", the values of PRDA[9]~PRDA[0] in PRDAL and PRDxH are PWMA period data.

1: When this bit set to "**1**", READ values FROM PRDA[9]~PRDA[0] in PRDAL and PRDxH are PWMA timer data.

Bits 2~0: Not used, fixed to "**0**" all the time.

6.3.97 Bank1 R30: PWMBCR (PWM B Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	TRCBB	0	0	0

Bits 7~4: Not used, fixed to "**0**" all the time.

Bit 3(TRCBB): B Read Control bit

0: When this bit set to 0, the values of PRDB[9]~PRDB[0] in PRDBL and PRDxH are PWMB period data

1: When this bit set to 1, the values of PRDB[9]~PRDB[0] in PRDBL and PRDxH are PWMB timer data

Bits 2~0: Not used, fixed to "**0**" all the time.

6.3.98 Bank1 R31: (Not Used)

6.3.99 Bank1 R32: TACR (Timer A Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	TAP2	TAP1	TAP0

Bits 7~3: Not used, fixed to "**0**" all the time.

TAP2	TAP1	T1AP0	Prescaler
0	**0**	**0**	1 : 2 (Default)
0	**0**	**1**	1 : 4
0	**1**	**0**	1 : 8
0	**1**	**1**	1 : 16
1	**0**	**0**	1 : 32
1	**0**	**1**	1 : 64
1	**1**	**0**	1 : 128
1	**1**	**1**	1 : 256

6.3.100 Bank1 R33: TBCR (Timer B Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	TBP2	TBP1	TBP0

Bits 7~3: Not used, fixed to "**0**" all the time.

Bits 2~0 (TBP2~TBP0): Timer B Prescaler bits

TBP2	TBP1	TBP0	Prescaler
0	0	0	1 : 2 (Default)
0	0	1	1 : 4
0	1	0	1 : 8
0	1	1	1 : 16
1	0	0	1 : 32
1	0	1	1 : 64
1	1	0	1 : 128
1	1	1	1 : 256

6.3.101 Bank1 R34: (Not Used)

6.3.102 Bank1 R35: TAPRDH (Timer A Period Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA[9]	PRDA[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]

Bits 7~0 (PRDA[9]~PRDA[2]): The contents of this register is a period of Timer A.

6.3.103 Bank1 R36: TBPRDH (Timer B Period Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB[9]	PRDB[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]

Bits 7~0 (PRDB[9]~PRDB[2]): The contents of this register is a period of Timer B.

6.3.104 Bank1 R37: (Not Used)

6.3.105 Bank1 R38: TADTH (Timer A Duty Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA[9]	DTA[8]	DTA[7]	DTA[6]	DTA[5]	DTA[4]	DTA[3]	DTA[2]

Bits 7~0 (DTA[9]~ DTA[2]): The contents of this register is a duty of Timer A.

6.3.106 Bank1 R39: TBDTH (Timer B Duty Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB[9]	DTB[8]	DTB[7]	DTB[6]	DTB[5]	DTB[4]	DTB[3]	DTB[2]

Bits 7~0 (DTB[7]~DTB[0]): The contents of this register is a duty of Timer B.

6.3.107 Bank1 R3A: (Not Used)

6.3.108 Bank1 R3B: PRDxL (PWM A/B/C Period Buffer Low Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	PRDB[1]	PRDB[0]	PRDA[1]	PRDA[0]

Bits 7~4: Not used, fixed to "**0**" all the time.

Bits 3~2 (PRDB[1]~PRDB[0]): PWM B period buffer low bits

Bits 1~0 (PRDA[1]~PRDA[0]): PWM A period buffer low bits

6.3.109 Bank1 R3C: DTxL (PWM1/2 Duty Buffer Low Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	DTB[1]	DTB[0]	DTA[1]	DTA[0]

Bits 7~4: Not used, fixed to "**0**" all the time.

Bits 3~2 (DTB[1]~DTB[0]): PWM B duty buffer high bits

Bits 1~0 (DTA[1]~DTA[0]): PWM A duty buffer high bits

6.3.110 Bank1 R3D~R4F (Not Used)

6.3.111 Bank0 R50~R7F, Bank0~1 R80~RFF

These are all 8-bit general-purpose registers.

6.4 TCC/WDT and Prescaler

Two 8-bit counters are available as prescalers for the TCC and WDT respectively. The PST0~PST2 bits of the TCCCR register (Bank0 R13) are used to determine the ratio of the prescaler of TCC. Likewise, the PSW0~PSW2 bits of the WDTCR register Bank0 R11) are used to determine the prescaler of WDT. The prescaler counter is cleared by the instructions each time they are written into TCC. The WDT and prescaler are cleared by the "WDTC" and "SLEP" instructions. Figure 6-11 below depicts the circuit diagram of the TCC/WDT.

TCCDATA (Bank0 R14) is an 8-bit timer/counter. The clock source of TCC can be internal clock or external signal input (edge selectable from the TCC pin). If the TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). As illustrated in the following figure, if TCC signal source is from external clock input, TCC will increase by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (keep in High or low level) must be greater than 1CLK. **The TCC will stop running when sleep mode occurs.**

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e., in Sleep mode). During the normal operation or the Sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the Normal mode by software programming. Refer to WDDTE bit of Bank0 R11 register (Section 6.3.14). Without prescaler, the WDT time-out period is approximately 18 ms[1] (one oscillator start-up timer period).

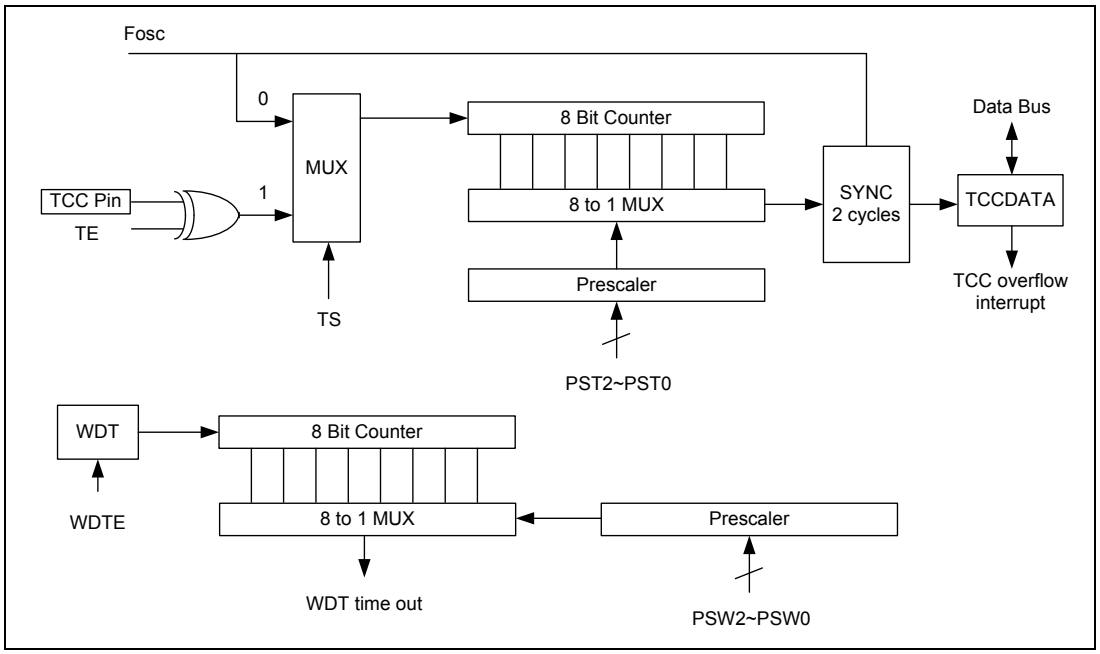


Figure 6-11 TCC and WDT Block Diagram

6.5 I/O Ports

6.5.1 I/O for EM78F644N/642/641/544/542/541N

The I/O registers, Ports 5, 6, 7, and 8, are bidirectional tri-state I/O ports. Port 6 or 7 can be pulled high internally by software. Moreover, Port 6 can also have an open-drain output by software. Input status change interrupt (or wake-up) function on Port 6 P50~P53, P60 ~ P63, and Port 7 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC8).

The I/O registers and I/O control registers are both readable and writable.

[1] *VDD=5V, WDT time-out period = 16.5ms ± 8%, VDD=3V, WDT time-out period = 18ms ± 8%.*

6.5.2 I/O for EM78F648/548N

The I/O registers, Port 5~Port 9 are bi-directional tri-state I/O ports. All have high sink/drive setting by software. Port 5, Port 6, and Port 7 also feature Wake up function. Furthermore, Port 6 is also equipped with input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC9).

The I/O registers and I/O control registers are both readable and writable.

Table below shows the usage of EM78F64xN/54xN Port 6 Input Change Wake-up/Interrupt functions:

Usage of Port 6 input status changed Wake-up/Interrupt	
I. Wake-up from Port 6 Input Status Change a) Before SLEEP 1. Disable WDT[2] (execute very carefully) 2. Read I/O Port 6 (MOV R6,R6) 3. Enable interrupt: After wake-up, if "ENI," switch to interrupt vector (006H). If "DISI," execute the next instruction. Disable interrupt: Always execute the next instruction. 4. Enable wake-up enable bit 5. Execute "SLEP" instruction b) After WAKE-UP 1. If "ENI" → Interrupt vector (006H) 2. If "DISI" → Next instruction	**II Port 6 Input Status Change Interrupt** 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt 4. IF Port 6 change (interrupt) → Interrupt vector (006H)

[2] *Software disables WDT (watchdog timer) but hardware must be enabled before applying Port 6 Change Wake-Up function (CODE Option Register and Bit 11 (ENWDTB-) set to "**1**").*

6.6 UART (Universal Asynchronous Receiver/Transmitter)

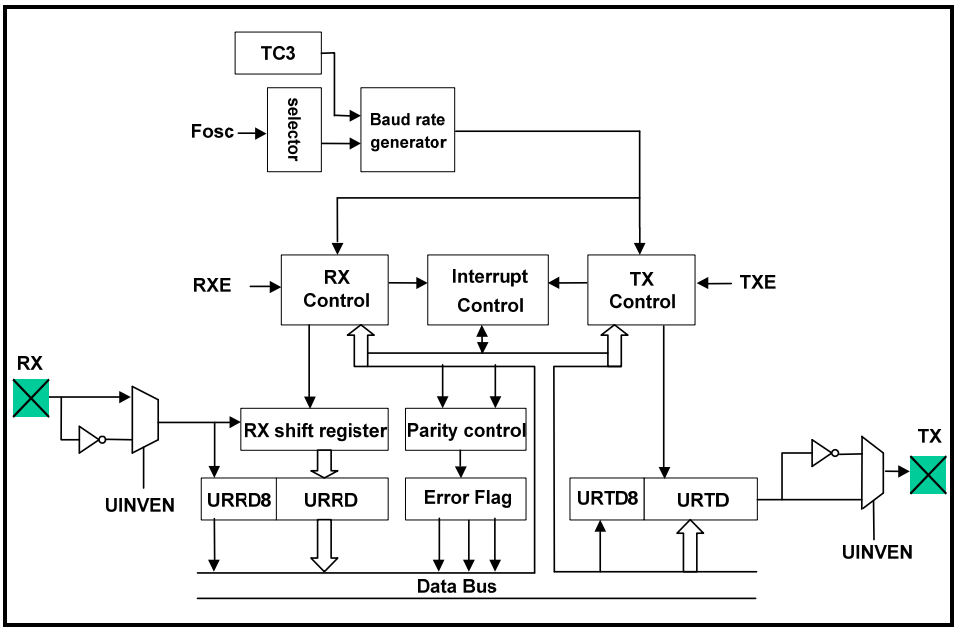


Figure 6-12a UART Function Block Diagram

In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

Full duplex data transfer is possible since the UART has independent transmit and receive sections. Double buffering for both sections allows the UART to be programmed for continuous data transfer.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the marked state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirm the end of the frame.

In receiving, the UART synchronizes on the falling edge of the start bit. When two or three "**0**" are detected during three samples, it is recognized as normal start bit and the receiving operation is started.

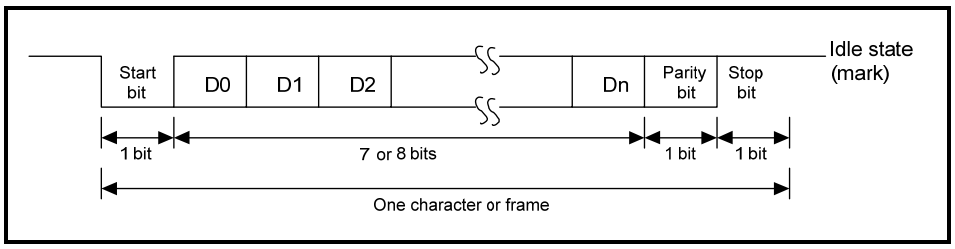


Figure 6-12b UART Data Format

6.6.1 UART Mode

Three UART modes are available. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bits. The parity bit addition is not available in Mode 3. Figure below shows the data format in each mode.

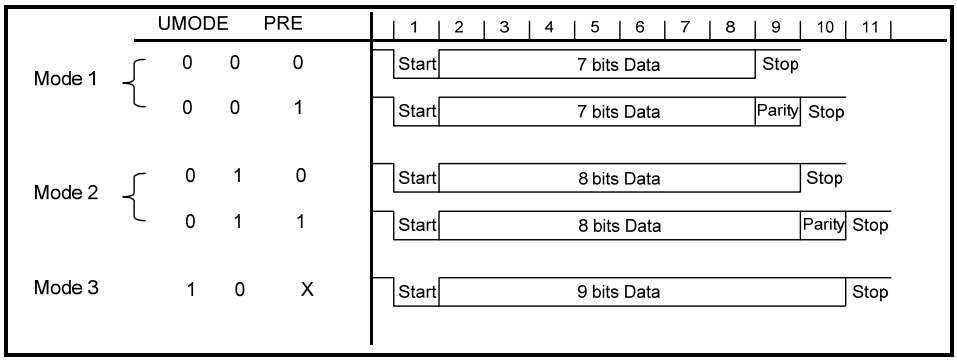


Figure 6-13 UART Modes 1, 2, &3 Data Formats

6.6.2 Transmitting

In transmitting serial data, the UART operates as follows:

1. Sets the TXE bit of the URCR1 register to enable the UART transmission function.
2. Writes data into the URTD register and the UTBE bit of the URCR1 register will be set by hardware.
3. Then start transmitting.
4. Serially transmitted data in the following order from the TX pin (see Figure 6-12b above):
   a) Start bit: One "**0**" bit is output.
   b) Transmit data: 7, 8, or 9 bits data are output from the LSB to the MSB.
   c) Parity bit: One parity bit (odd or even selectable) is output.
   d) Stop bit: One "**1**" bit (stop bit) is output.
   e) Mark state: Output "**1**" continues until the start bit of the next transmitted data.

NOTE

After transmitting the Stop bit, the UART generates a TBEF interrupt (if enabled).

6.6.3 Receiving

During Receiving, the UART operates as follows:

1. Sets RXE bit of the URS register to enable the UART receiving function. The UART monitors the RX pin and synchronizes internally when it detects a Start bit.
2. Received data is shifted into the URRD register in LSB to MSB order.
3. The parity bit and the stop bit are received. After one character is received, the URBF bit of the URS register will be set to "**1**" to allow UART interrupt to occur.
4. The UART then makes the following checks:
   a) Parity check: The number of ones ("**1**") of the received data must match the even or odd parity setting of the EVEN bit in the URS register.
   b) Frame check: The start bit must be "**0**" and the stop bit must be "**1**".
   c) Overrun check: The URBF bit of the URS register must be cleared (i.e., the URRD register should be read out) before the next received data is loaded into the URRD register.

   If any of the checks failed, the UERRIF interrupt will be generated (if enabled), and an error flag is indicated in PRERR, OVERR or FMERR bit. The error flag should be cleared by software. Otherwise, UERRIF interrupt will occur when the next byte is received.
5. Read the received data from URRD register and the URBF bit will be cleared by hardware.

6.6.4 Baud Rate Generator

The baud rate generator features a circuit that generates a clock pulse to determine the transfer speed for transmission/reception in the UART.

The BRATE2~BRATE0 bits of the URC register determine the desired baud rate.

6.6.5 UART Timing

■ Transmission Counter Timing:

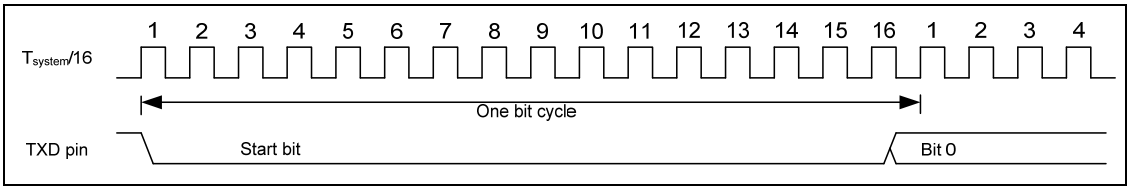


Figure 6-14a UART Transmission Counter Timing Diagram

■ Receiving Counter Timing:

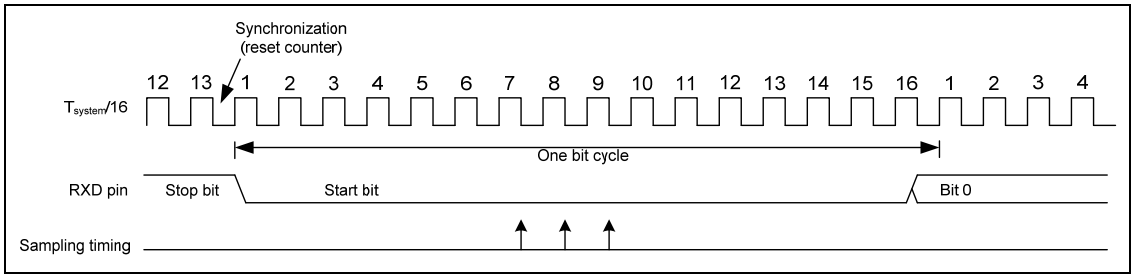


Figure 6-14b UART Receiving Counter Timing Diagram

6.7 SPI Function

6.7.1 Overview & Features

6.7.1.1 Overview

Figures 6-15a, 6-15b, and 6-16a below, illustrate how the EM78F648N/F548N MCUs communicate with other devices through SPI module. If the MCUs are a Master controller, they send clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if the MCUs are defined as a Slave, their SCK pins could be programmed as an input pin. Data will continue to be shifted based on both the clock rate and the selected edge. You can also set the SPIS bit 7(DORD) to decide the SPI transmission order, set the SPIS Bit 6 (TD1), Bit 5 (TD0) to decide the SDO status output delay time (see Section 6.3.30), and set SPICR Bit 3 (SDOC) to decide SDO pin status after serial data output (see Section 6.3.29).

6.7.1.2 Features

- Operation in either Master mode or Slave mode
- Three-wire or four-wire full duplex synchronous communication
- Programmable baud rates of communication,
- Programming clock polarity
- Interrupt flag available for the read buffer full
- SPI transmission order
- After serial data output SDO status select
- SDO status output delay time
- SPI handshake pin
- Up to 8 MHz (maximum) bit frequency

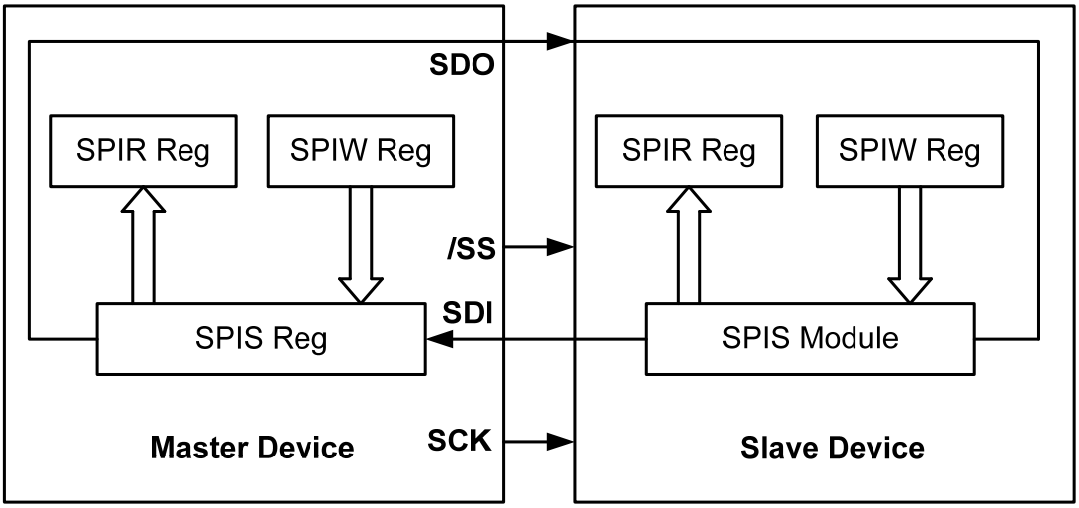


Figure 6-15a SPI Master/Slave Communication Block Diagram

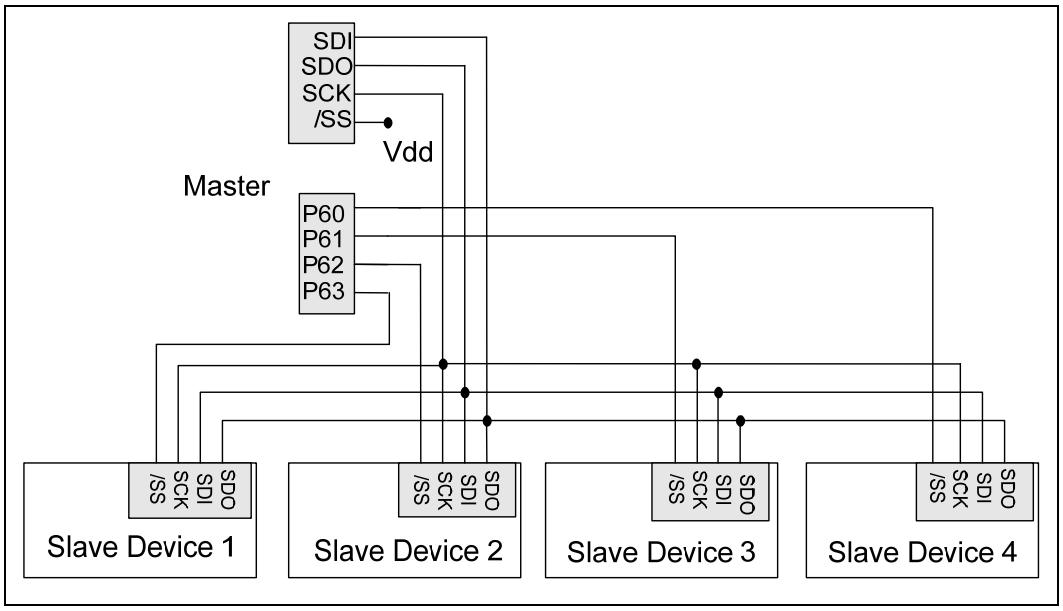


Figure 6-15b Single-Master and Multi-Slave SPI Configuration

6.7.2 SPI Function Description

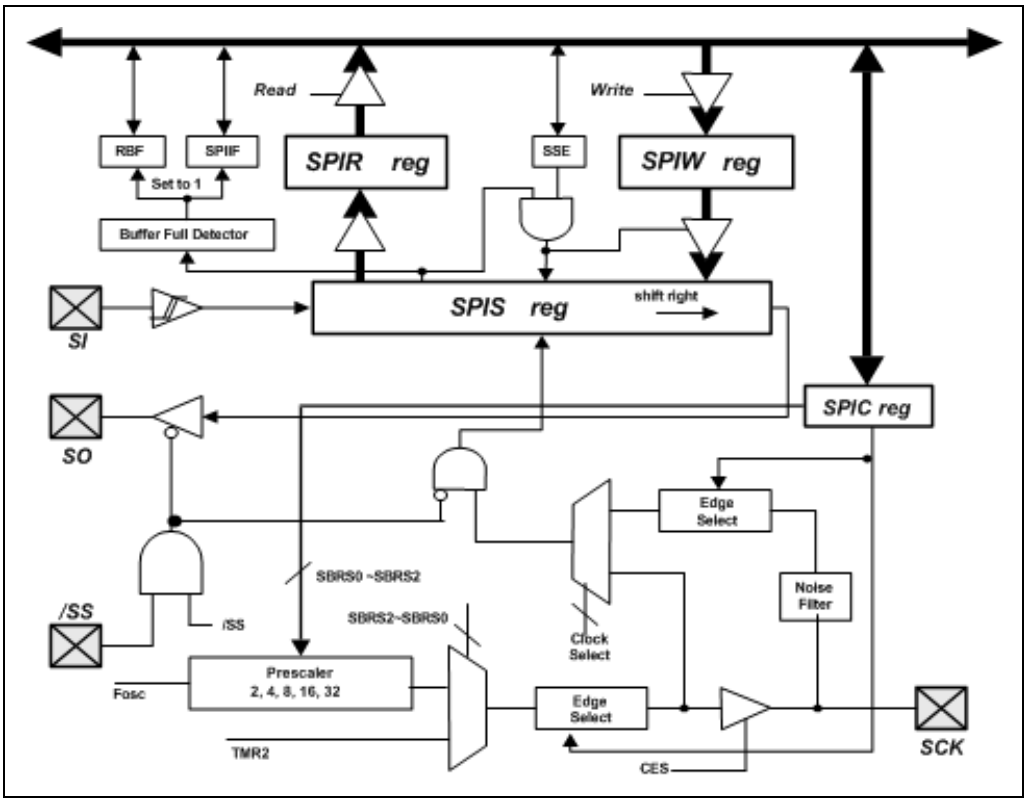


Figure 6-16a SPI Function Block Diagram

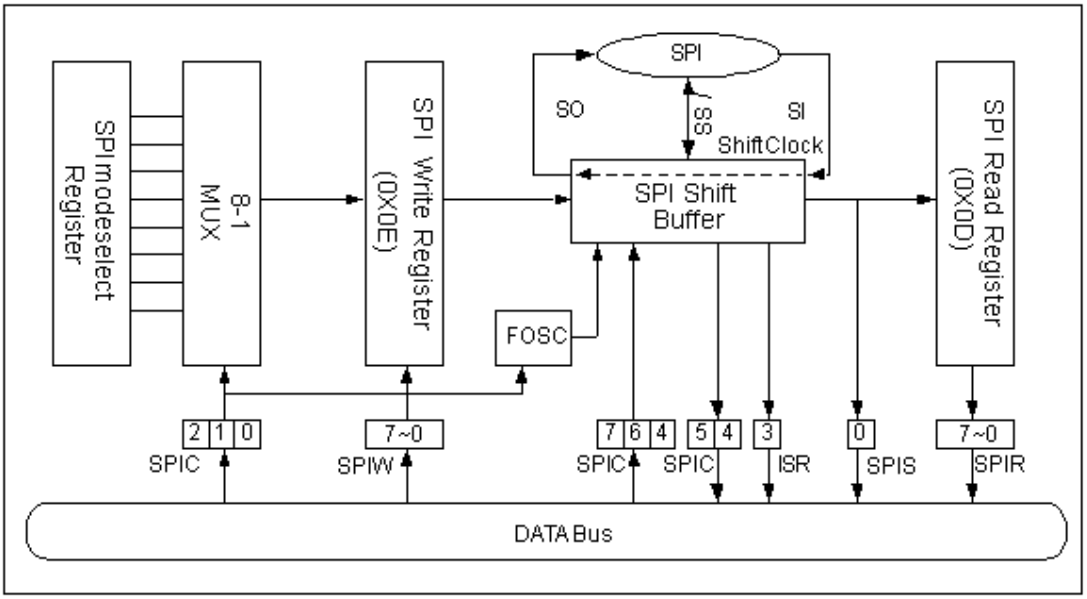


Figure 6-16b SPI Transmission Function Block Diagram

The following will describe the functions of each block and on how to carry out the SPI communication with the signals depicted in Figures 6-16a and 6-16b above.

- **SI:** Serial Data In
- **SO:** Serial Data Out
- **SCK:** Serial Clock
- **/SS:** /Slave Select (Option). This pin (/SS) may be required during a Slave mode
- **RBF:** Set by Buffer Full Detector
- **Buffer Full Detector:** Set to "**1**" when an 8-bit shifting is completed.
- **SSE:** Loads the data in SPIS register, and begin to shift. The SSE bit is kept at "**1**" while communication is continuing and to determine if the next write attempt is available. This flag must be cleared when shifting is completed.
- **SPIS reg.:** Shifting byte in and out. The MSB is shifted first. Both the SPIR and the SPIW registers are shifted at the same time. Once data are written, SPIS starts transmission / reception. The data received will be moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the SPIIF (SPI Interrupt) flag are then set.
- **SPIR reg.:** Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register is being read.
- **SPIW reg.:** Write buffer. The buffer will deny any attempts to write until the 8-bit shifting is completed.
- **SBRS2~SBRS0:** Programming the clock frequency/rates and sources.
- **Clock Select:** Selecting either the internal or the external clock as the shifting clock.
- **Edge Select:** Selecting the appropriate clock edges by programming the CES bit

6.7.3 SPI Signal & Pin Description

The detailed functions of the four pins, SI, SO, SCK, and /SS are as follows**:**

- **SI:**
  - Serial Data In
  - Receive in sequential order. The Most Significant Bit (MSB) first, the Least Significant Bit (LSB) last.
  - Defined as high-impedance, if not selected.

- Program the same clock rate and clock edge to latch on both the Master and Slave devices.
- The received byte will update the transmitted byte.
- The RBF will be set when the SPI operation is completed.
- Timing is shown in Figures 6-17a and 6-17b below (Section 6.7.4).

■ **SO:**

- Serial Data Out
- Transmit in sequential order. The Most Significant Bit (MSB) first, the Least Significant Bit (LSB) last
- Program the same clock rate and clock edge to latch on both the Master and Slave devices
- The received byte will update the transmitted byte
- The CES bit will reset as the SPI operation is completed
- Timing is shown in Figures 6-17a and 6-17b below (Section 6.7.4).

■ **SCK:**

- Serial Clock
- Generated by a Master device
- Synchronize the data communication on both the SI and SO pins
- The CES is used to select the edge to communicate.
- The SBR0~SBR2 is used to determine the communication baud rate.
- The CES, SBR0, SBR1, and SBR2 bits have no effect under Slave mode
- Timing is shown in Figures 6-17a and 6-17b below (Section 6.7.4).

■ **/SS:**

- Slave Select; negative logic
- Generated by a Master device to indicate the Slave(s) to receive data
- Goes low before the first cycle of SCK appears, and remains low until the last (eighth) cycle is completed.
- Ignores the data on the SI and SO pins while /SS is high. This is due to the SO is no longer driven.
- Timing is shown in Figures 6-17a and 6-17b below (Section 6.7.4).

6.7.4 SPI Mode Timing

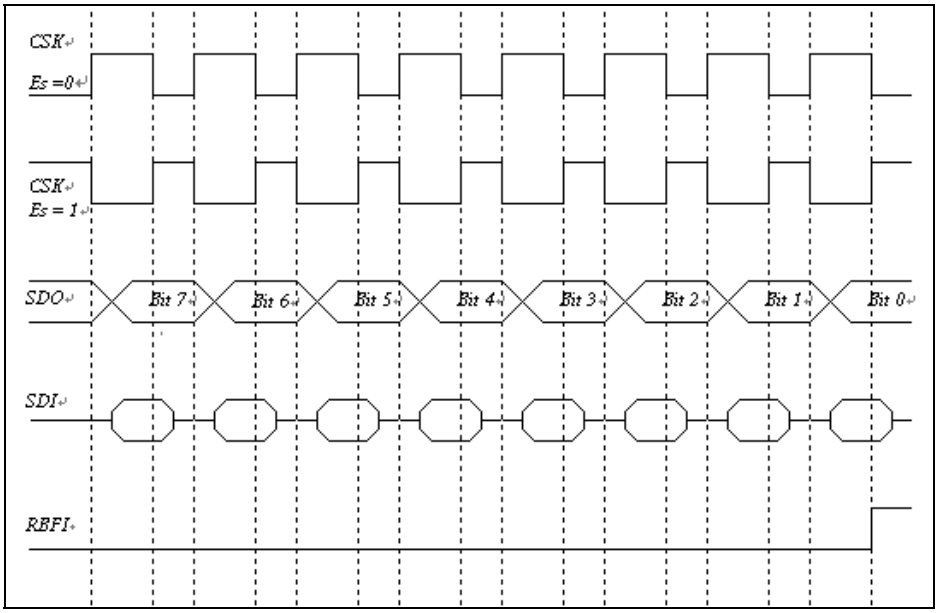


Figure 6-17a SPI Mode with /SS Disabled Timing Diagram

The SCK edge is selected by programming the CES bit. The waveform shown in the above figure (Figure 17a) is applicable regardless of whether the EM78F648N/644N /548N/544N is in Master or Slave mode with /SS disabled. However, the waveform in the figure below (Figure 17b) can only be implemented in Slave mode with /SS enabled.

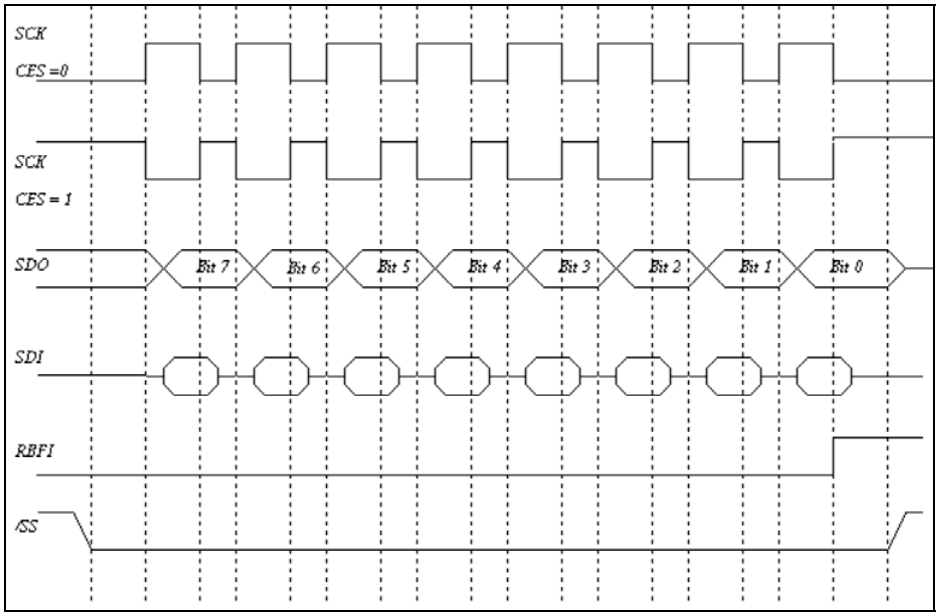


Figure 6-17b SPI Mode with /SS Enabled Timing Diagram

6.8 I2C Function

■ **EM78F648N/F548N** Registers for I2C Circuit

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0X23	**I2CCR1**	**Strobe/ Pend**	**IMS**	**ISS**	**STOP**	**SAR_ EMPTY**	**ACK**	**FULL**	**EMPTY**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X24	**I2CCR2**	0	0	0	0	**I2CTS1**	**I2CTS0**	**I2CCS**	**I2CEN**
			R	R	R	R	R/W	R/W	R/W	R/W
Bank 1	0X25	**I2CSA**	**SA6**	**SA5**	**SA4**	**SA3**	**SA2**	**SA1**	**SA0**	**IRW**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X26	**I2CDA**	**DA7**	**DA6**	**DA5**	**DA4**	**DA3**	**DA2**	**DA1**	**DA0**
				R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X27	**I2CDB**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X28	**I2CA**	**0**	**0**	**0**	**0**	**0**	**0**	**DA9**	**DA8**
				R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0E	**ISR3**	0	0	0	0	0	PWMCIF	**I2CRIF**	**I2CTIF**
			R	R	R	R	R	R/W	R/W	R/W
Bank 0	0x1E	**IMR3**	0	0	0	0	0	PWMCIE	**I2CRIE**	**I2CTIE**
			R	R	R	R	R	R/W	R/W	R/W

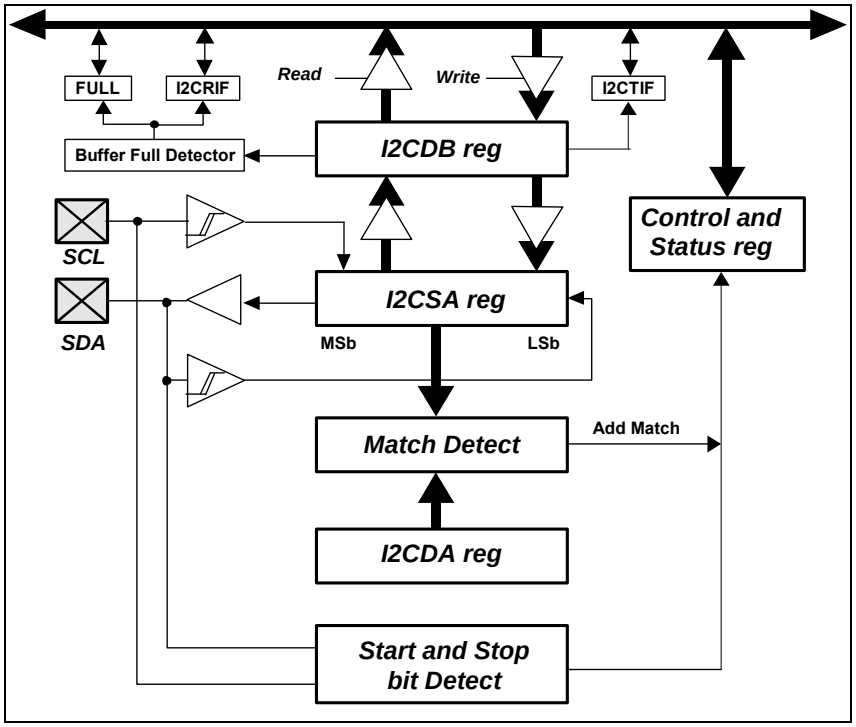


*Figure 6-18a **EM78F648N/F548N** I2C Block Diagram*

The **EM78F648N/F548N** supports a bidirectional, 2-wire bus, 7-bits & 10-bits addressing and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device that receives data is defined as a receiver. The bus has to be controlled by a Master device which generates the Serial Clock (SCL), controls the bus access, and generates the Start and Stop conditions. Both Master and Slave can operate as transmitter or receiver, but only the Master device can determine which mode is activated.

Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. The output stages of the devices that are connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I2C-bus can be transferred at the rates of up to 100k bit/s in Standard-mode or up to 400k bit/s in the Fast-mode.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Within the procedure of the I2C bus, unique situations could arise, which are defined as START (S) and STOP (P) conditions.

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

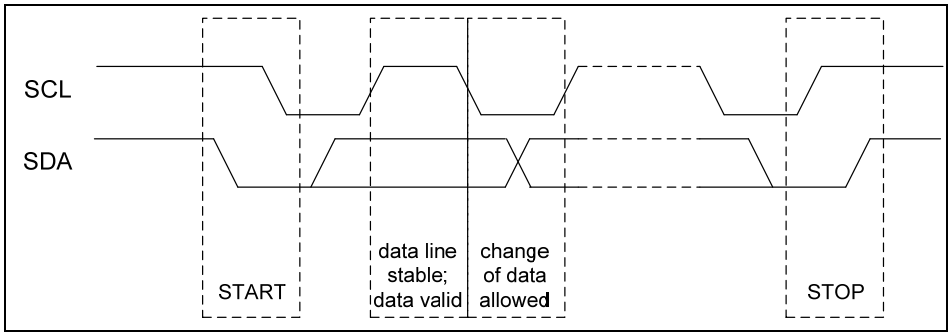


Figure 6-18b I2C Transfer Condition

6.8.1 7-Bit Slave Address

Master-transmitter transmits to Slave-receiver. The transfer direction is not changed. Master reads Slave immediately after the first byte. At the moment of the first acknowledge, the Master-transmitter becomes a Master-receiver and the Slave-receiver becomes a Slave-transmitter. This first acknowledge is still generated by the Slave. The STOP condition is generated by the Master, which has previously sent a not-acknowledge (A). The difference between Master-transmitter and Master-receiver is only with their in R//W bit. If the R//W bit is "**0**", the Master device becomes a transmitter. Otherwise, the Master device turns to be a receiver (R//W bit is "**1**"). The Master-transmitter operation is illustrated in Figure 6-19a, and that of Master-receiver is shown in "Figure 6-19b below.

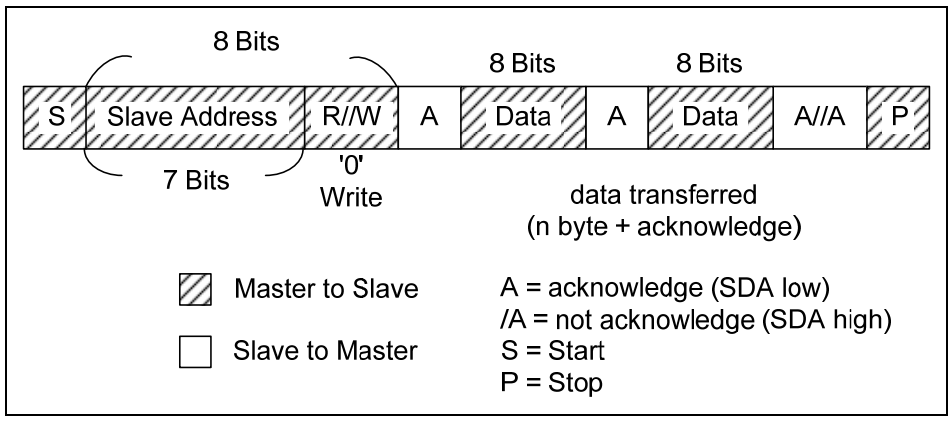


Figure 6-19a Master-Transmitter Transmits to Slave-Receiver with 7-Bit Slave Address

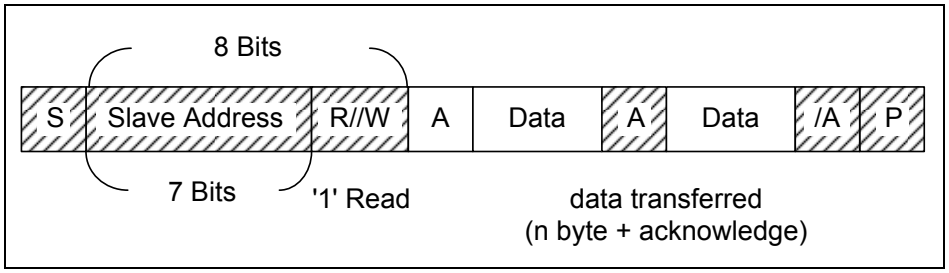


Figure 6-19b Master-Receiver Reads from Slave-Transmitter with 7-Bit Slave Address

6.8.2 10-Bit Slave Address:

In 10-bit Slave Address mode, using 10-bit for addressing exploits the reserved combination 11110XX for the first 7 bits of the first byte following a START (S) or repeated START (Sr) condition. The first 7 bits of the first byte are the combination 11110XX of which the last 2 bits (XX) are the two most-significant bits of the 10-bit address. If the R//W bit were "0", the second byte after acknowledge would be the 8 address bits of the10-bit Slave address. Otherwise, the second byte would just be the next transmitted data from a Slave to Master device. The first bytes 11110XX are transmitted using the Slave address register (I2CSA), and the second bytes XXXXXXXX are transmitted using the data buffer (I2CDB).

The possible data transfer formats for 10-bit Slave Address Mode are explained in the following paragraphs:

6.8.2.1 Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address

When the Slave received the first byte after the START bit from the Master, each Slave device will compare with the 7 bits of the first byte (11110XX) with their own address and the 8th bit (R//W). If the R//W bit is "**0**", the Slave will return an Acknowledge A1. It is possible that more than one Slave devices will return the Acknowledge A1. Then all Slave devices will continue to compare with the second address (XXXXXXXX). If a Slave device has found a match, that particular Slave device will be the only one to return an Acknowledge A2. The matched Slave device will remain addressed by the Master until it receives a STOP condition or a repeated START condition followed by a different Slave address.

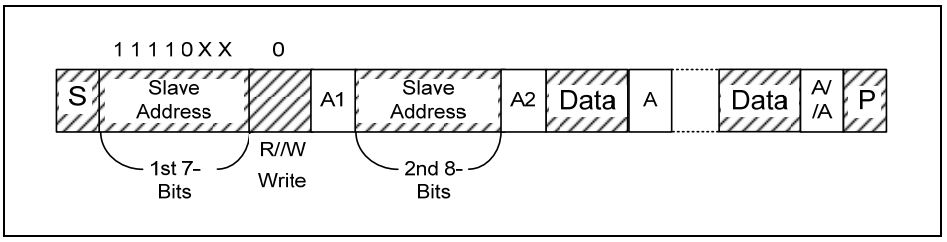


Figure 6-20a Master-Transmitter Transmits to Slave-Receiver with a 10-Bit Slave Address

6.8.2.2 Master-Receiver Reads from Slave-Transmitter with a 10-bit Slave Address

Up to, and including Acknowledge Bit A2, the procedure is the same as that described above for Master-transmitter addressing a Slave receiver. After the Acknowledge A2, a repeated START (Sr) condition takes place, followed by 7 bits Slave address (11110XX) but the 8th bit R//W is "**1**". The addressed Slave device will then return an Acknowledge A3. If the repeated START (Sr) condition occurs and the 7 bits of the first byte (11110XX) are received by the Slave device, all the Slave devices will compare with their own address and test the 8th bit (R//W). However, none of the Slave devices can return an Acknowledge because R//W=1.

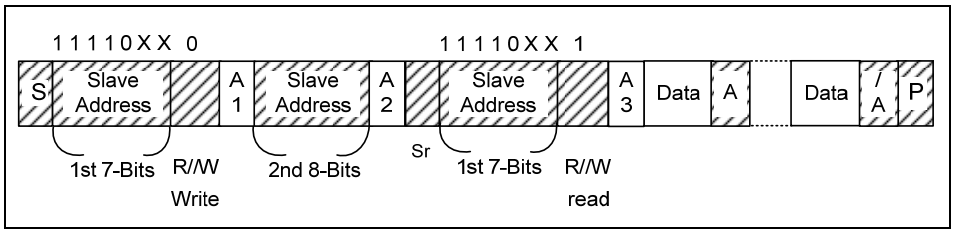


Figure 6-20b Master-Receiver Read Slave-Transmitter with a 10-Bit Slave Address

6.8.2.3 Master Transmits and Receives Data to & from the Same Slave Device with 10-Bit Addresses

The Initial operation of this data transfer format is the same as explained in Section 6.8.2.1 above. Then the Master device starts to transmit the data to the Slave device. When the Slave device receives an Acknowledge or Not Acknowledge that is followed by repeat START (Sr), the operation "*Master-Receiver Reads from Slave-Transmitter with 10-bit Slave Address*" described in the preceding Section 6.8.2.2, is then performed.

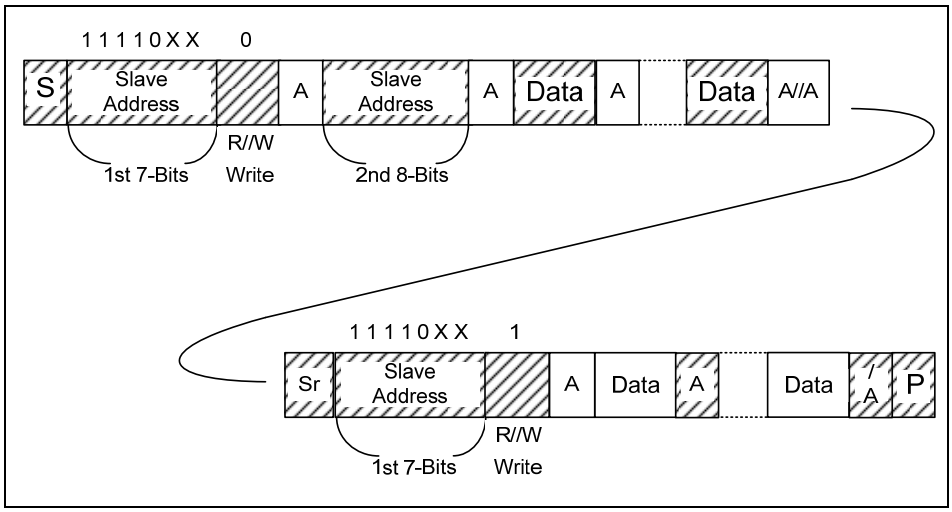


Figure 6-20c Master Addresses a Slave with 10-Bit addresses Transmits and Receives Data in the Same Slave Device.

6.8.2.4 Master Device Transmits Data to Two or More Slave Devices with 10 & 7 Bits Slave Address

For 10-bit Slave address transmittal, the initial operation of this data transmit format is the same as explained in the Section 6.8.2.1 above which describes how to transmit the data to Slave device. After the Master device completed the initial transmittal, and want to continue transmitting data to another device, the Master needs to address each of the new Slave devices by repeating the initial operation mentioned above.

When the Master device wants to transmit data in 7-bit and 10-bit Slave address modes successively, this could be done after the START or repeat START conditions as illustrated in the following figures.

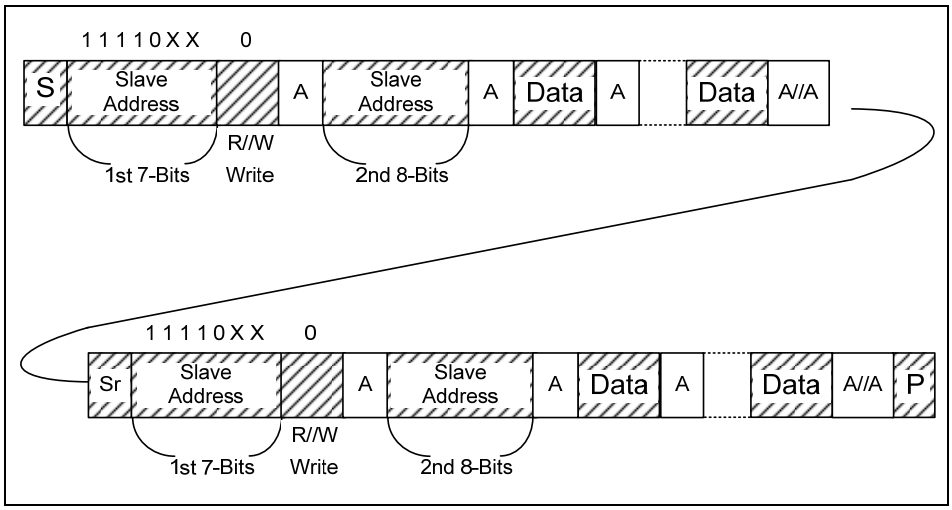


Figure 6-20d Master Transmitting to More than One Slave Devices with 10-Bit Slave Address

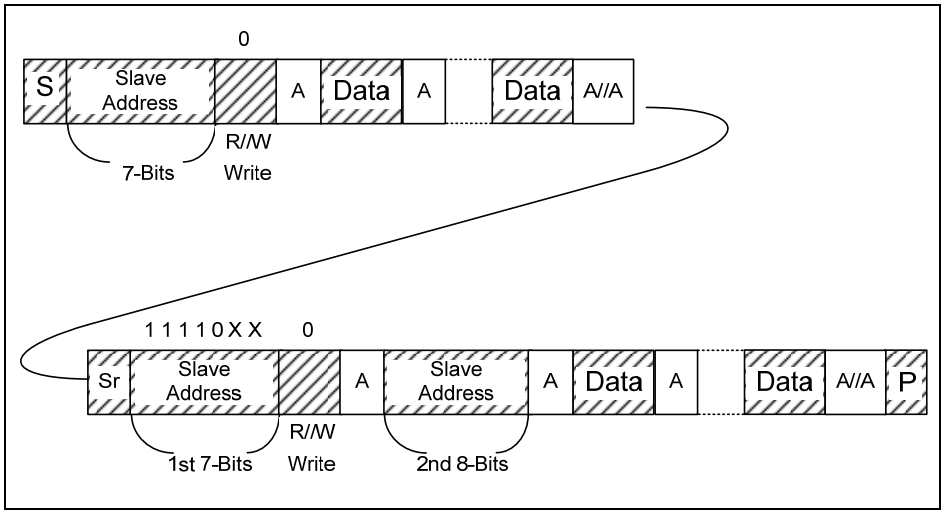


Figure 6-20e Master Successively Transmitting 7-Bit & 10-Bit Slave Addresses to Slave

6.8.3 Master Mode I2C Tranmit

In transmitting serial data, the I2C operates as follows:

1. Set I2CTS1~0, I2CCS, and ISS bits to select I2C transmit clock source.
2. Set I2CEN and IMS bits to enable I2C master function.
3. Write Slave address into the I2CSA register and IRW bit to select Read or Write.
4. Set strobe bit will start transmitting and then Check SAR_EMPTY bit.
5. Write 1st data into the I2CDB register, set Strobe bit and Check EMPTY bit.
6. Write 2nd data into the I2CDB register, set Strobe bit, STOP bit and Check EMPTY bit.

6.8.2 Slave Mode I2C Tranmit

In receiving, the I2C operates as follows:

1. Set I2CTS1~0, I2CCS, and ISS bits to select I2C transmit clock source.
2. Set I2CEN and IMS bits to enable I2C Slave function.
3. Write device address into the I2CDA register.
4. Check FULL bit, read I2CDB register (address), and then clear Pend bit.
5. Check FULL bit, read I2CDB register (1st data), and then clear Pend bit.
6. Check FULL bit, read I2CDB register (2nd data), and then clear Pend bit.

6.9 Dual Set of PWM (Pulse Width Modulation)

6.9.1 Overview

In PWM mode, PWMA and PWMB pins produce up to a 10-bit resolution PWM output (see Figure 6-21a below for the functional block diagram). A PWM output has a period and a duty cycle, and it keeps the output in high. The baud rate of the PWM is the inverse of the period. Figure 6-21b depicts the relationships between a period and a duty cycle.

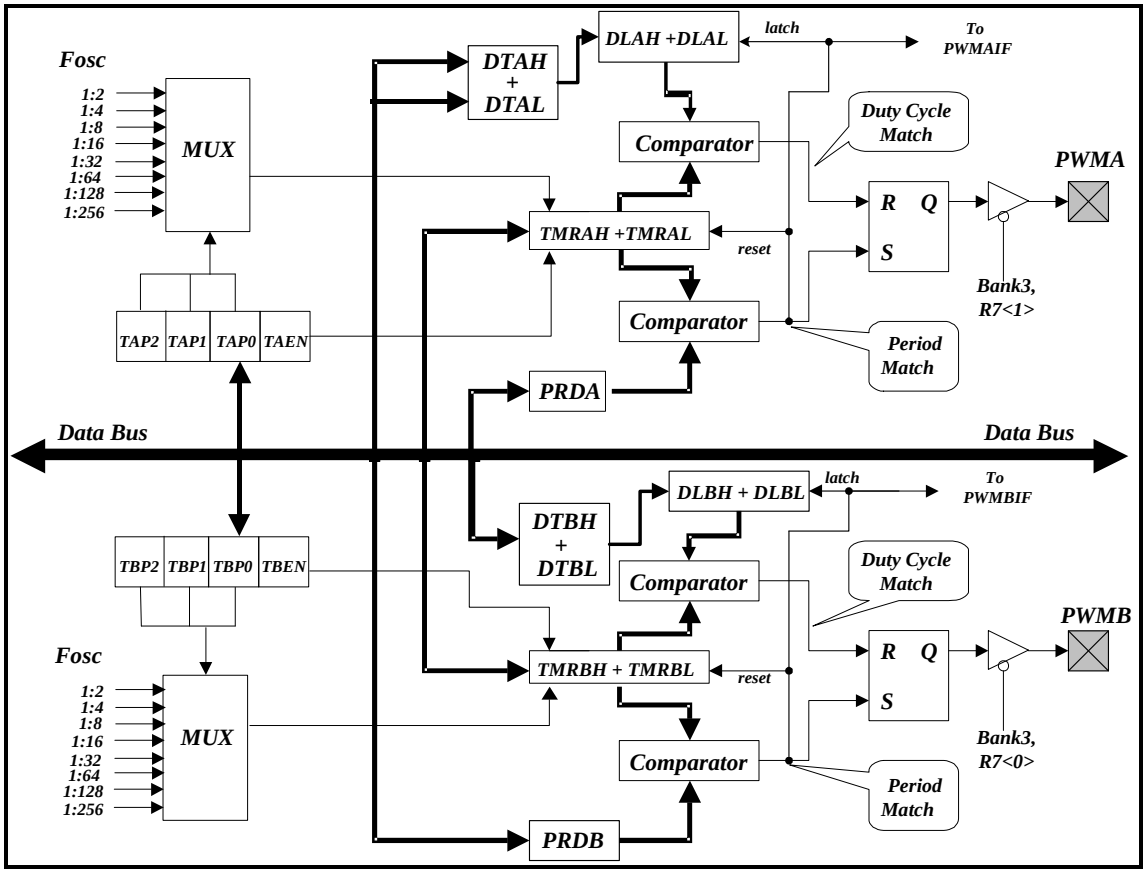


Figure 6-21a Two PWMs Functional Block Diagram

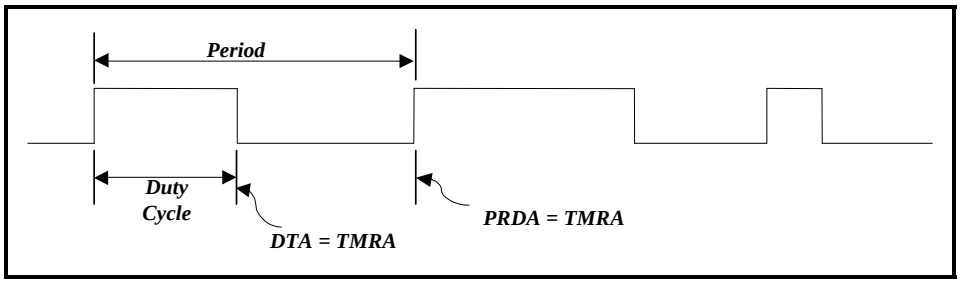


Figure 6-21b PWM Output Timing

6.9.2 Increment Timer Counter (TMRX: TMRAH/L or TMRBH/L)

TMRX are 10-bit clock counters with programmable prescalers. They are designed as baud rate clock generators for the PWM module. TMRX is Read only. When is use, they can be turned off for power saving by setting the TAEN or TBEN bits to "**0**".

6.9.3 PWM Period (PRDX : PRDA or PRDB)

The PWM period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

1) TMRX is cleared.
2) The PWMX pin is set to 1.
3) The PWM duty cycle is latched from DTA/DTB to DLA/DLB.

NOTE

*The PWM output will not be set, if the duty cycle is "**0**".*

(4) The PWMXIF pin is set to "**1**".

To calculate the PWM time period, use the following formula:

$$Period = (PRDX + 1) \times \left(\frac{1}{Fosc}\right) \times (TMRX \ \ prescaler\ value)$$

Example:

PRDX = 49; Fosc = 4 MHz, TMRX (0, 0, 0) = 1 : 2,

Then-

$$Period = (49+1) \times \left(\frac{1}{4M}\right) \times 2 = 25\mu s$$

6.9.4 PWM Duty Cycle (DTX: DTA or DTB)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at any time. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle:

$$Duty\ cycle = (DTX) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX \ \ prescale\ value)$$

Example:

DTX = 10; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 2,

Then-

$$Duty\ cycle = (10) \times \left(\frac{1}{4M}\right) \times 2 = 5\mu s$$

6.10 Comparator

EM78F664N/F662N/F661N/F564N/F562N/F561N has one comparator; while F648N/F548N has two comparators. Each one has two analog inputs and one output. The comparators can be utilized to Wake up the MCU from Sleep mode. The following figure illustrates the comparator circuit and operation mode.

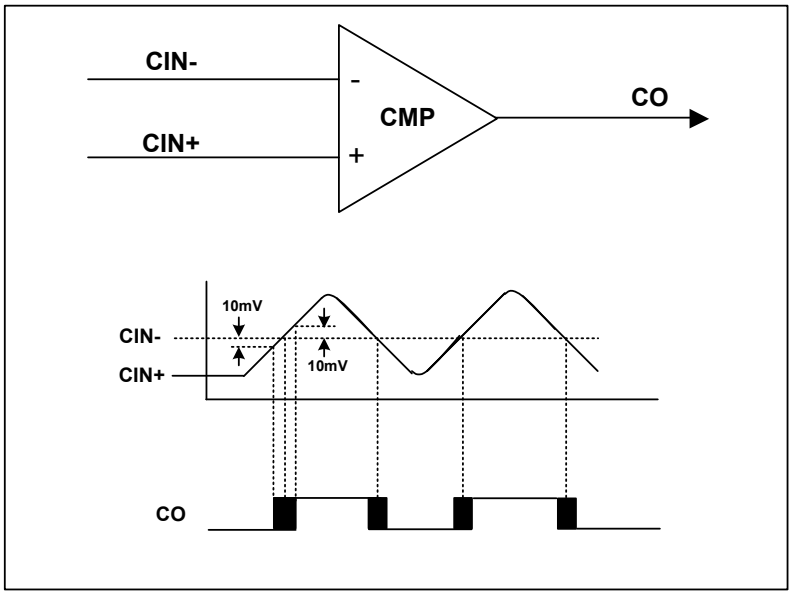


Figure 6-22 Comparator Circuit and Operation Mode

6.10.1 External Reference Signal

The analog signal that is presented at CIN- compares to the signal at CIN+, and the digital output (CO) of the comparator is adjusted accordingly.

- The reference signal must be between VSS and VDD.
- The reference voltage can be applied to either pin of the comparator.
- Threshold detector applications may use the same reference.
- The comparator can operate from the same or different reference source.

6.10.2 Internal Reference Signal

EM78F648N/F548N offers two internal voltage references which are applicable to CIN1+/CIN2+. You can use the voltage references in setting C1RS of R39 Bank 0/C2RS of R3C Bank 0 and corresponding voltage level in R43 Bank 0.

6.10.3 Comparator Outputs

For EM78F664N/F662N/F661N/F564N/F562N/F561N:

- The compared result is stored in the CPOUT2 of R7 Bit 4 of Bank 3.
- The comparator is output to CO2 (P80) by programming Bit 3, Bit 2 <COS21, COS20> of Register R7 Bank 3.

For EM78F648N/F548N:

- The compared result is stored in CP1OUT of R39 Bit 6 of Bank 0 for comparator1; in CP2OUT of R3C Bit 6 of Bank 0 for comparator 2.
- By programming Bit 5, Bit 4 <CMP1COS1, CMP1COS0> of Register R39 Bank 0 and Bit 5, Bit 4 <CMP2COS1, CMP2COS0> of Register R3C Bank 0, the compared results can be output to CO1 and CO2 pins.

The following figure depicts the comparator output block diagram.

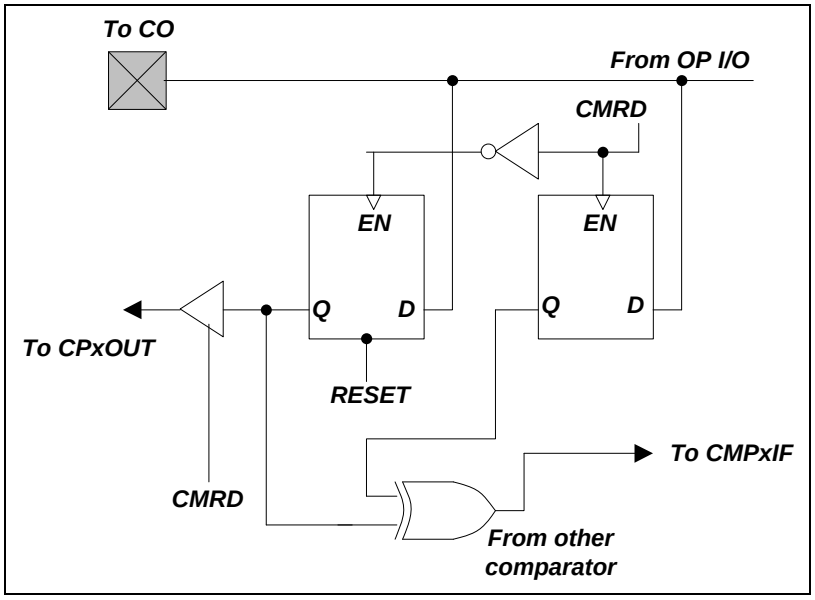


Figure 6-23 Comparator Output Block Diagram

6.10.4 Interrupt

For EM78F664N/F662N/F661N/F564N/F562N/F561N:

- CMP2IE (IOCE.7) and the "ENI" instruction execution must be enabled.
- Interrupt is executed whenever a change occurs on the output pin of the comparator.
- The actual change on the pin can be determined by reading the Bit CPOUT2, R7 Bit 4 of Bank 3.
- CMP2IF (RF.7 Bank 1) and the comparator interrupt flag, can only be cleared by software.

For EM78F648N/F548N**:**

- CMP1IE, CMP2IE, and the “ENI” instruction execution must be enabled.
- Interrupt occurs whenever a change occurs on the comparators output pins.
- The actual change on the pins can be determined by reading the bit CP1OUT of R39 Bit 6 of Bank 0 for Comparator 1 and the bit CP2OUT of R3C Bit 6 of Bank 0 for Comparator 2.
- CMP1IF, CMP2IF, and the comparator interrupt flags, can only be cleared by software.

6.10.5 Wake-up from Sleep Mode

- When enabled, the comparator remains active and the interrupt remains functional, even under Sleep mode.
- If a mismatch occurs, the interrupt will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is not utilized during Sleep mode, turn off the comparator before going into Sleep mode.

6.11 RESET and Wake-up

6.11.1 RESET & Wake-up for EM78F644/642/641/544/542/541N

A RESET is initiated by one of the following events**:**

1) Power-on reset
2) /RESET pin input "low"
3) WDT time-out (if enabled)

The device is kept in a RESET condition for a period of approximately 18ms (one oscillator start-up timer period) after a RESET is detected. Once a RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "**0**".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper three bits of R3 are cleared.
- The bits of RB, RC, RD registers are set to their previous status.
- The bits of CONT register are set to all "**0**".
- The bits of IOCA register are set to all "**0**".

- The bits of IOCB register are set to all "**1**".
- The bits of IOCC register are set to all "**0**".
- The bits of IOCD register are set to all "**1**".
- The bits of IOCE register are set to all "**0**".
- The bits of IOCF register are set to all "**0**".

The Sleep (power down) mode is asserted by executing the "SLEP" instruction. While entering Sleep mode, the WDT (if enabled) is cleared but keeps on running until wake-up is triggered by one of the following events (wake-up time in RC mode, the wake-up time is 10μs and in High Crystal (XTAL) mode is 800μs)**:**

Event 1) External reset input on /RESET pin

Event 2) WDT time-out (if enabled)

Event 3) Port 6 input status changes (if enabled)

Event 4) Comparator output status changes (if CMPWE is enabled)

Event 5) External (P60, /INT) pin changes (if EXWE is enabled)

Event 6) SPI receives data while SPI is acting as Slave device (if SPIWE is enabled)

The first two events will cause the IC to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Events 3, 4, 5, & 6 are considered as continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the Address 0×6, 0×15, 0×3, 0×12 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. In RC mode, the wake-up time is 10μs and that of High Crystal (XTAL) mode, is 800μs.

Only one event of Events 2 to 6 can be enabled before entering into Sleep mode. That is-

a) If WDT is enabled before SLEP, all the RA register bits are disabled. Hence, the IC can wake-up only under Events 1 or 2 conditions. Refer to the Interrupt section (Section 6.12) for further details.

b) If Port 6 Input Status Change is used to wake-up the IC and the ICWE bit of RA register is enabled before SLEP, WDT must be disabled. Hence, the IC can wake-up only under Event 3 conditon.

Under this situation, the following instructions must be executed before SLEP:

```
MOV           A, @0xxx1000b ; Select WDT prescaler and
                            ; Disable the WDT
IOW           IOCA
WDTC                        ; Clear WDT and prescaler
MOV           R6, R6        ; Read Port 6
ENI (or DISI)               ; Enable (or disable) global
                            ; interrupt
BC            R4, 7         ; Select Bank 0
BC            R4, 6
MOV           A, @0100xxxxb ; Enable Port 6 input change
                            ; wake-up bit
MOV           RA,A
MOV           A, @xxxxxx1xb ; Enable Port 6 input change
                            ; interrupt
IOW           IOCF
SLEP                        ; Sleep
```

c) If Comparator 2 Output Status Change is used to wake-up the IC and the CMPWE bit of RA register is enabled before SLEP, WDT must be disabled by software. Hence, the IC can wake-up only under Event 4 condition.

Under this situation, the following instructions must be executed before SLEP:

```
BS            R4, 7         ; Select Bank 3
BS            R4, 6
MOV           A, @xxxx10xxb ; Select a comparator and P80 act
                            ; as CO pin
MOV           R7,A
MOV           A, @0xxx1000b ; Select WDT prescaler and
                            ; Disable the WDT
IOW           IOCA
WDTC                        ; Clear WDT and prescaler
ENI (or DISI)               ; Enable (or disable) global
                            ; interrupt
BC            R4, 7         ; Select Bank 0
BC            R4, 6
MOV           A, @1000xxxxb ; Enable comparator output status
                            ; change wake-up bit
MOV           RA,A
MOV           A, @10000000b ; Enable comparator output status
                            ; change interrupt
IOW           IOCE
SLEP                        ; Sleep
```

d) If External (P60,/INT) pin change is used to wake-up IC and the EXWE bit of RA register is enabled before SLEP, WDT must be disabled. Hence, the IC can wake up only under Events 5 condition.

e) When SPI is used as Slave device, IC will wake-up after receiving data, and the SPIWE bit of RA register is enabled before SLEP. The WDT must be disabled by software. Hence, the IC can wake up only under Events 6 condition.

■ Summary of all types of Wake-up and Interrupt modes:

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	EXWE = 0, EXIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	EXWE = 0, EXIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	EXWE = 1, EXIE = 0	Wake-up + Next Instruction		Wake-up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	EXWE = 1, EXIE = 1	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Port 6 Pin Change	ICWE = 0, ICIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	ICWE = 0, ICIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWE = 1, ICIE = 0	Wake-up + Next Instruction		Wake-up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	ICWE = 1, ICIE = 1	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC Overflow	TCIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	TCIE = 1	Wake-up is invalid.		Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
SPI Interrupt	SPIWE = 0, SPIIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	SPIWE = 0, SPIIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	SPIWE = 1, SPIIE = 0	Wake-up + Next Instruction*		Wake-up + Next Instruction*		Interrupt is invalid.		Interrupt is invalid.	
	SPIWE = 1, SPIIE = 1	Wake-up + Next Instruction*	Wake-up + Interrupt Vector*	Wake-up + Next Instruction*	Wake-up + Interrupt Vector*	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

* *SPI must be in Slave mode*

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
Comparator 2 (Comparator Output Status Change)	CMP2WE=0 CMP2IE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	CMP2WE=0 CMP2IE = 1	wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	CMP2WE=1 CMP2IE = 0	Wake-up + Next Instruction		Wake-up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	CMP2WE=1 CMP2IE = 1	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC1 interrupt	TC1IE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	TC1IE = 1	Wake-up is invalid.		Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Transmit Complete Interrupt	UTIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	UTIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive Data Buffer Full Interrupt	URIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	URIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive Error Interrupt	UERRIE = 0	wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	UERRIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC2 Interrupt	TC2IE = 0	Wake-Up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	TC2IE = 1	Wake-up is invalid.		Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC3 Interrupt	TC3IE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	TC3IE = 1	Wake-up is invalid.		Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWM A/B (When TimerA/B Match PRDA/B)	PWMxIE = 0 (x = A or B)	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	PWMxIE = 1 (x = A or B)	Wake-up is invalid.		Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

NOTE

After wake up:
1. If interrupt enabled → interrupt + next instruction
2. If interrupt disabled → next instruction

■ Summary of the Initialized Values for Registers:

Legend: ***U:*** *Unknown or don't care,* ***P:*** *Previous value before reset,* ***T:*** *Check table in (next) Section 6.11.3.*

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC7	Bit Name	C77	C76	C75	C74	C73	C72	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC8	Bit Name	-	-	-	-	-	C82	C81	C80
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to interrupt vector address or continue to execute next instruction.							

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×03	R3 (SR)	Bit Name	-	-	-	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0×04	R4 (RSR)	Bit Name	Bank 1	Bank 0	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	P5 (Bank 0)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	P6 (Bank 0)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	P7 (Bank 0)	Bit Name	P77	P76	P75	P74	P73	P72	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	P8 (Bank 0)	Bit Name	-	-	-	-	P83	P82	P81	P80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	R9 (Bank 0)	Bit Name	RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (Bank 0)	Bit Name	CMP2WE	ICWE	-	EXWE	SPIWE	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	RB (ECR) (Bank 0)	Bit Name	RD	WR	EEWE	EEDF	EEPC	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0C	RC (Bank 0)	Bit Name	EE_A7	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 0)	Bit Name	EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 0)	Bit Name	-	TIMERSC	CPUS	IDLE	-	-	-	-
		Power-on	0	1	1	1	0	0	0	0
		/RESET and WDT	0	1	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (ISR) (Bank 0)	Bit Name	-	-	SPIIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	R5 (Bank 1)	Bit Name	TC1CAP	TC1S	TC1CK1	TC1CK0	TC1M	TC1ES	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	R6 (Bank 1)	Bit Name	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	R7 (Bank 1)	Bit Name	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	R8 (Bank 1)	Bit Name	RCM1	RCM0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0
		Power-on	WORD1<3,2>		0	0	0	0	0	0
		/RESET and WDT	WORD1<3,2>		0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	R9 (Bank 1)	Bit Name	TC2D15	TC2D14	TC2D13	TC2D12	TC2D11	TC2D10	TC2D9	TC2D8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0A	RA (Bank 1)	Bit Name	TC2D7	TC2D6	TC2D5	TC2D4	TC2D3	TC2D2	TC2D1	TC2D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	RB (Bank 1)	Bit Name	DORD	TD1	TD0	-	OD3	OD4	-	RBF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	RC (Bank 1)	Bit Name	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 1)	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 1)	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (Bank 1)	Bit Name	CMP2IF	-	TC3IF	TC2IF	TC1IF	UERRIF	RBFF	TBEF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (Bank 2)	Bit Name	URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
		Power-on	U	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	RB (Bank 2)	Bit Name	-	-	SBIM1	SBIM0	UINVEN	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	P	P	P	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	RC (Bank 2)	Bit Name	URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0D	RD (Bank 2)	Bit Name	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 2)	Bit Name	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (Bank 2)	Bit Name	/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	R5 (Bank 3)	Bit Name	TAEN	TAP2	TAP1	TAP0	TBEN	TBP2	TBP1	TBP0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	R6 (Bank 3)	Bit Name	MLB	-	-	-	RBit11	RBit10	RBit9	RBit8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	R7 (Bank 3)	Bit Name	-	-	-	CPOUT2	COS21	COS20	PWMAE	PWMBE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	R8 (Bank 3)	Bit Name	PRDA[1]	PRDA[0]	DTA[1]	DTA[0]	PRDB[1]	PRDB[0]	DTB[1]	DTB[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	R9 (Bank 3)	Bit Name	PRDA[9]	PRDA[8]	PRDA[7]	PRDA[6]	PRDA[5]	PRDA[4]	PRDA[3]	PRDA[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (Bank 3)	Bit Name	DTA[9]	DTA[8]	DTA[7]	DTA[6]	DTA[5]	DTA[4]	DTA[3]	DTA[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0B	RB (Bank 3)	Bit Name	PRDB[9]	PRDB[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	RC (Bank 3)	Bit Name	DTB[9]	DTB[8]	DTB[7]	DTB[6]	DTB[5]	DTB[4]	DTB[3]	DTB[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 3)	Bit Name	TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 3)	Bit Name	TCR3D7	TCR3D6	TCR3D5	TCR3D4	TCR3D3	TCR3D2	TCR3D1	TCR3D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (Bank 3)	Bit Name	/PD77	/PD76	/PD75	/PD74	/PD73	/PD72	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0×0A	IOCA	Bit Name	WDTE	EIS	-	-	PSWE	PSW2	PSW1	PSW0
		Power-un	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	IOCB	Bit Name	/PD63	/PD62	/PD61	/PD60	/PD53	/PD52	/PD51	/PD50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	IOCC	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	IOCD	Bit Name	/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0E	IOCE	Bit Name	CMP2IE	-	TC3IE	TC2IE	TC1IE	UERRIE	URIE	UTIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	IOCF	Bit Name	-	-	SPIIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×10 ~ 0×3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

6.11.2 RESET & Wake-up for EM78F648/548N

A RESET is initiated by one of the following events**:**

1) Power on reset.

2) /RESET pin input "low"

3) WDT time-out (if enabled).

The device is kept in a RESET condition for a period of approximately 18ms[3] (one oscillator start-up timer period) after a reset is detected. If the /Reset pin goes “low” or WDT time-out is active, a RESET is generated. In RC mode the reset time is 34clocks, while in High XTAL mode, reset time is 2ms + 32clocks. In Low XTAL mode, the reset time is 500ms. Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "**0**".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- The bits of the control register are set as indicated in the table on “*Summary of the Initialized Values for Registers*.” shown below.

[3] Vdd = 5V, set up time period = 16.8ms ± 8%
Vdd = 3V, set up time period = 18ms ± 8%

The Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering Sleep mode, the WDT (if enabled) is cleared but keeps on running until wake-up is triggered by one of the following events (wake-up time in RC mode is 34clocks, in High XTAL mode is 2ms + 32clocks, and in Low XTAL mode, is 500ms)**:**

Event 1) External reset input on /RESET pin

Event 2) WDT time-out (if enabled)

Event 3) External (P60,/INT) pin changes (if EXWE is enabled)

Event 4) Port 6 input status changes (if ICWE is enabled)

Event 5) Comparator 1/2 output status changes (if CMP1WE/CMP2WE is enabled)

Event 6) SPI receives data while SPI is acting as Slave device (if SPIWE is enabled)

Event 7) Port 5/Port 7 input status changes (if corresponding control bits are enabled)

The first two cases will cause the EM78F648N/F548N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Events 3,4,5,6, & 7 are considered as the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x3, 0x6, 0X15, 0X30 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. All of the Sleep mode wake-up time is 150μs, regardless of what the status is of the oscillation mode (except for Low XTAL mode which has a wake-up time of 500ms).

Only one of Events 2 to 7 can be enabled before entering into Sleep mode. That is-

a) If WDT is enabled before SLEP, the EM78F648N/F548N can wake-up only by Events 1 or 2. Refer to the Interrupt section (Section 12) for further details.

b) If External (P60, /INT) pin change is used to wake-up EM78F648N/F548N and the EXWE bit is enabled before SLEP, the WDT must be disabled. Hence, the controller can wake-up only under Event 3 condition.

c) If Port 6 Input Status Change is used to wake-up EM78F648N/F548N and the corresponding wake-up setting is enabled before SLEP, the WDT must be disabled. Hence, the controller can wake-up only under Event 4 condition.

d) If Comparator 1/2 Output Status Change is used to wake-up EM78F648N/F548N and the CMP1WE/CMP2WE bit of Bank0 R2F register is enabled before SLEP, the WDT must be disabled by software. Hence, the controller can wake-up only under Event 5 condition.

e) When SPI is acting as Slave device, EM78F648N/F548N will wake-up after receiving data, and the SPIWE bit of Bank0 R2F register is enabled before SLEP, the WDT must be disabled by software. Hence, the controller can wake-up only under Event 6 condition.

f) If Ports 6 & 7 Input Status Change is used to wake-up EM78F648N/F548N and the corresponding wake-up setting is enabled before SLEP, the WDT must be disabled. Hence, the controller can wake-up only under Event 7 condition.

■ Summary of all types of Wake-up and Interrupt modes (for EM78F648/548N only):

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	EXWE = 0, EXIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	EXWE = 0, EXIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	EXWE = 1, EXIE = 0	Wake-up + Next Instruction		Wake-up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	EXWE = 1, EXIE = 1	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Port 6 Pin Change	ICWE = 0, ICIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	ICWE = 0, ICIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWE = 1, ICIE = 0	Wake-up + Next Instruction		Wake-up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	ICWE = 1, ICIE = 1	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC Overflow	TCIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	TCIE = 1	Wake-up is invalid.		Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
SPI Interrupt	SPIWE = 0, SPIIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	SPIWE = 0, SPIIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	SPIWE = 1, SPIIE = 0	Wake-up + Next Instruction*		Wake-up + Next Instruction*		Interrupt is invalid.		Interrupt is invalid.	
	SPIWE = 1, SPIIE = 1	Wake-up + Next Instruction*	Wake-up + Interrupt Vector*	Wake-up + Next Instruction*	Wake-up + Interrupt Vector*	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

* *SPI must be in Slave mode*

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
Comparator x (Comparator Output Status Change) x = 1, 2	CMPxWE=0 CMPxIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	CMPxWE=0 CMPxIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	CMPxWE=1 CMPxIE = 0	Wake-up + Next Instruction		Wake-up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	CMPxWE=1 CMPxIE = 1	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC1 interrupt	TC1IE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	TC1IE = 1	Wake-up is invalid.		Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Transmit Complete Interrupt	UTIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	UTIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive Data Buffer Full Interrupt	URIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	URIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive Error Interrupt	UERRIE = 0	wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	UERRIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC2 Interrupt	TC2IE = 0	Wake-Up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	TC2IE = 1	Wake-up is invalid.		Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
LVD	LVDWE = 0, CMPxIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	LVDWE = 0, LVDIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	LVDWE = 1, LVDIE = 0	Wake-up + Next Instruction		Wake-up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	LVDWE = 1, LVDIE = 1	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC3 Interrupt	TC3IE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	TC3IE = 1	Wake-up is invalid.		Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWM A/B (When TimerA/B Match PRDA/B)	PWMxIE = 0 (x = A or B)	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	PWMxIE = 1 (x = A or B)	Wake-up is invalid.		Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I2C TX Interrupt	I2CTIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	I2CTIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I2C RX Interrupt	I2CRIE = 0	Wake-up if received correct address		Wake-up if received correct address		Interrupt is invalid.		Interrupt is invalid.	
	I2CRIE = 1	Wake-up if received correct address		Wake-up if received correct address		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I2C STOP Interrupt	I2CSTPIE=0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	I2CSTPIE=1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

NOTE

After wake up:
1. If interrupt enabled → interrupt + next instruction
2. If interrupt disabled → next instruction

■ Summary of the Initialized Values for Registers (for EM78F648/548N only):

Legend: ***U:*** *Unknown or don't care,* ***P:*** *Previous value before reset,* ***T:*** *Check table in (next) Section 6.11.3.*

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (BSR)	Bit Name	0	0	0	SBS0	0	0	0	GBS0
		Power-On	0	0	0	U	0	0	0	U
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	P	0	0	0	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	0	0	0	T	P	Z	DC	C
		Power-On	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-Up from Pin Change	0	0	0	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X05	BANK 0, R5 (PORT 5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x06	BANK 0, R6 (PORT 6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x07	BANK 0, R7 (PORT 7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x08	BANK 0, R8 (PORT 8)	Bit Name	P87	P86	P85	P84	P83	P82	P81	P80
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09	BANK 0, R9 (PORT 9)	Bit Name	P97	P96	P95	P94	P93	P92	P91	P90
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0B	BANK 0, RB (OMCR)	Bit Name	CPUS	IDLE	TC1SS	TC2SS	TC3SS	TASS	TBSS	TCSS
		Power-On	1	1	0	0	0	0	0	0
		/RESET and WDT	1	1	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0C	BANK 0, RC (ISR1)	Bit Name	LVDIF	ADIF	SPIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0D	BANK 0, RD (ISR2)	Bit Name	CMP2IF	CMP1IF	TC3IF	TC2IF	TC1IF	UERRIF	RBFF	TBEF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	BANK 0, RE (ISR3)	Bit Name	0	0	0	0	I2CDTPIF	0	I2CRIF	I2CTIF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x10	BANK 0, R10 EIESCR	Bit Name	0	0	0	0	0	0	0	EIES
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	0	0	P
0x11	BANK 0, R11 WDTCR	Bit Name	WDTE	EIS	INT	0	PSWE	PSW2	PSW1	PSW0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	0	P	P	P	P
0x12	BANK 0, R12 LVDCR	Bit Name	0	0	0	0	LVDEN	/LVD	LVD1	LVD0
		Power-On	0	0	0	0	0	R	0	0
		/RESET and WDT	0	0	0	0	0	R	0	0
		Wake-Up from Pin Change	0	0	0	0	P	R	P	P
0X13	BANK 0, R13 TCCCR	Bit Name	0	TCCS	TS	TE	PSTE	PST2	PST1	PST0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	P	P	P	P	P	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X14	BANK 0, R14 TCCDATA	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X15	BANK 0, R15 IOCR5	Bit Name	IOC57	IOC56	IOC55	IOC54	IOC53	IOC52	IOC51	IOC50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X16	BANK 0, R16 IOCR6	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X17	BANK 0, R17 IOCR7	Bit Name	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X18	BANK 0, R18 IOCR8	Bit Name	IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X19	BANK 0, R19 IOCR9	Bit Name	IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X1C	BANK 0, R1C IMR1	Bit Name	LVDIE	ADIE	SPIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X1D	BANK 0, R1D IMR2	Bit Name	CMP2IE	CMP1IE	TC3IE	TC2IE	TC1IE	UERRIE	URIE	UTIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X1E	BANK 0, R1E IMR3	Bit Name	0	0	0	0	I2CSTPIE	0	I2CRIE	I2CTIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X20	BANK 0, R20 P5WUCR	Bit Name	WU_P57	WU_P56	WU_P55	WU_P54	WU_P53	WU_P52	WU_P51	WU_P50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X21	BANK 0, R21 P5WUECR	Bit Name	WUE_P57	WUE_P56	WUE_P55	WUE_P54	WUE_P53	WUE_P52	WUE_P51	WUE_P50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X22	BANK 0, R22 P7WUCR	Bit Name	WU_P77	WU_P76	WU_P75	WU_P74	WU_P73	WU_P72	WU_P71	WU_P70
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X23	BANK 0, R23 P7WUECR	Bit Name	WUE_P77	WUE_P76	WUE_P75	WUE_P74	WUE_P73	WUE_P72	WUE_P71	WUE_P70
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X2B	BANK 0, R2B SPICR	Bit Name	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X2C	BANK 0, R2C SPIS	Bit Name	DORD	TD1	TD0	0	OD3	OD4	0	RBF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	0	P	P	0	P
0X2D	BANK 0, R2D SPIR	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X2E	BANK 0, R2E SPIW	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X2F	BANK 0, R2F WUCR1	Bit Name	0	SPIWE	LVDWE	ICWE	0	CMP2WE	CMP1WE	EXWE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	P	P	P	P	P	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X32	BANK 0, R32 URCR1	Bit Name	URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
		Power-On	U	0	0	0	0	0	1	0
		/RESET and WDT	P	0	0	0	0	0	1	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X33	BANK 0, R33 URCR2	Bit Name	0	0	SBIM1	SBIM0	UINVEN	0	0	0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	P	P	P	0	0	0
0X34	BANK 0, R34 URS	Bit Name	URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
		Power-On	U	0	0	0	0	0	0	0
		/RESET and WDT	P	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X35	BANK 0, R35 URRD	Bit Name	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X36	BANK 0, R36 URTD	Bit Name	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X37	BANK 0, R37 TBPTL	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X38	BANK 0, R38 TBPTH	Bit Name	HLB	GP1	GP0	TB12	TB11	TB10	TB9	TB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X39	BANK 0, R39 CMP1CR	Bit Name	C1RS	CP1OUT	CMP1COS	CMP1COS	CP1NS	CP1PS	CP1NRE	CP1NRDT
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X3C	BANK 0, R3C CMP2CR	Bit Name	C2RS	CP2OUT	CMP2COS	CMP2COS	CP2NS	CP2PS	CP2NRE	CP2NRDT
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	0	0	P	P	0	0
0X43	BANK 0, R43 CPIRLCON	Bit Name	BG2OUT	C2IRL2	C2IRL1	C2IRL0	BG1OUT	C1IRL2	C1IRL1	C1IRL0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X48	BANK 0, R48 TC1CR	Bit Name	TC1CAP	TC1S	TC1CK1	TC1CK0	TC1M	TC1ES	0	0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	0	0
0X49	BANK 0, R49 TCR1DA	Bit Name	TCR1DA7	TCR1DA6	TCR1DA5	TCR1DA4	TCR1DA3	TCR1DA2	TCR1DA1	TCR1DA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X4A	BANK 0, R4A TCR1DB	Bit Name	TCR1DB7	TCR1DB6	TCR1DB5	TCR1DB4	TCR1DB3	TCR1DB2	TCR1DB1	TCR1DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X4B	BANK 0, R4B T2CR	Bit Name	0	0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	P	P	P	P	P	P
0X4C	BANK 0, R4C TCR2DH	Bit Name	TCR2D15	TCR2D14	TCR2D13	TCR2D12	TCR2D11	TCR2D10	TCR2D9	TCR2D8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X4D	BANK 0, R4D TCR2DL	Bit Name	TCR2D7	TCR2D6	TCR2D5	TCR2D4	TCR2D3	TCR2D2	TCR2D1	TCR2D0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X4E	BANK 0, R4E TC3CR	Bit Name	TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X4F	BANK 0, R4F TC3RD	Bit Name	TCR3D7	TCR3D6	TCR3D5	TCR3D4	TCR3D3	TCR3D2	TCR3D1	TCR3D0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X05	BANK 1, R5 P5PHCR	Bit Name	/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X06	BANK 1, R6 P6PHCR	Bit Name	/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X07	BANK 1, R7 P7PHCR	Bit Name	/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	/PH71	/PH70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X08	BANK 1, R8 P8PHCR	Bit Name	/PH87	/PH86	/PH85	/PH84	/PH83	/PH82	/PH81	/PH80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X09	BANK 1, R9 P9PHCR	Bit Name	/PH97	/PH96	/PH95	/PH94	/PH93	/PH92	/PH91	/PH90
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0B	BANK 1, RB P5PLCR	Bit Name	/PL57	/PL56	/PL55	/PL54	/PL53	/PL52	/PL51	/PL50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0C	BANK 1, RC P6PLCR	Bit Name	/PL67	/PL66	/PL65	/PL64	/PL63	/PL62	/PL61	/PL60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0D	BANK 1, RD P7PLCR	Bit Name	/PL77	/PL76	/PL75	/PL74	/PL73	/PL72	/PL71	/PL70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0E	BANK 1, RE P8PLCR	Bit Name	/PL87	/PL86	/PL85	/PL84	/PL83	/PL82	/PL81	/PL80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0F	BANK 1, RF P9PLCR	Bit Name	/PL97	/PL96	/PL95	/PL94	/PL93	/PL92	/PL91	/PL90
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X11	BANK 1, R11 P5HD/SCR	Bit Name	/H57	/H56	/H55	/H54	/H53	/H52	/H51	/H50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X12	BANK 1, R12 P6HD/SCR	Bit Name	/H67	/H66	/H65	/H64	/H63	/H62	/H61	/H60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X13	BANK 1, R13 P5HD/SCR	Bit Name	/H77	/H76	/H75	/H74	/H73	/H72	/H71	/H70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X14	BANK 1, R14 P5HD/SCR	Bit Name	/H87	/H86	/H85	/H84	/H83	/H82	/H81	/H80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X15	BANK 1, R15 P5HD/SCR	Bit Name	/H97	/H96	/H95	/H94	/H93	/H92	/H91	/H90
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X17	BANK 1, R17 P5ODCR	Bit Name	OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X18	BANK 1, R18 P6ODCR	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X19	BANK 1, R19 P7ODCR	Bit Name	OD77	OD76	OD75	OD74	OD73	OD72	OD71	OD70
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X1A	BANK 1, R1A P8ODCR	Bit Name	OD87	OD86	OD85	OD84	OD83	OD82	OD81	OD80
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1B	BANK 1, R1B P9ODCR	Bit Name	OD97	OD96	OD95	OD94	OD93	OD92	OD91	OD90
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X1D	BANK 1, R1D IRCS	Bit Name	0	0	RCM1	RCM0	0	0	0	0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X1F	BANK 1, R21 EEPROM CONTROL	Bit Name	RD	WR	EEWE	EEDF	EEPC	0	0	0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X20	BANK 1, R1F EEPROM ADDR	Bit Name	EERA7	EERA6	EERA5	EERA4	EERA3	EERA2	EERA1	EERA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X21	BANK 1, R20 EEPROM DATA	Bit Name	EERD7	EERD6	EERD5	EERD4	EERD3	EERD2	EERD1	EERD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X23	BANK 1, R23 I2CCR1	Bit Name	Strobe/ Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
		Power-On	0	0	0	0	U	U	U	U
		/RESET and WDT	0	0	0	0	U	U	U	U
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X24	BANK 1, R24 I2CCR2	Bit Name	I2CBF	GCEN	0	0	I2CTS1	I2CTS0	I2CCS	I2CEN
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	P	P	P	P
0X25	BANK 1, R25 I2CSA	Bit Name	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X26	BANK 1, R26 I2CDA	Bit Name	0	DA6	DA5	DA4	DA3	DA2	DA1	DA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X27	BANK 1, R27 I2CDB	Bit Name	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X28	BANK 1, R28 I2CA	Bit Name	0	0	0	0	0	0	DA9	DA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X2A	BANK 1, R2A PWMER	Bit Name	0	0	0	0	0	0	PWMBE	PWMAE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	P	P	P
0X2B	BANK 1, R2B TIMEN	Bit Name	0	0	0	0	0	0	TBEN	TAEN
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	P	P	P
0X2F	BANK 1, R2F PWMACR	Bit Name	0	0	0	0	TRCBA	0	0	0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	P	0	0	0
0X32	BANK 1, R32 TACR	Bit Name	0	0	0	0	0	TAP2	TAP1	TAP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	P	P	P
0X33	BANK 1, R33 TBCR	Bit Name	0	0	0	0	0	TBP2	TBP1	TBP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	P	P	P
0X35	BANK 1, R35 TAPRDL	Bit Name	PRDA[9]	PRDA[8]	PRDA[7]	PRDA[6]	PRDA[5]	PRDA[4]	PRDA[3]	PRDA[2]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X36	BANK 1, R36 TBPRDL	Bit Name	PRDB[9]	PRDB[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X38	BANK 1, R38 TADT	Bit Name	DTA[9]	DTA[8]	DTA[7]	DTA[6]	DTA[5]	DTA[4]	DTA[3]	DTA[2]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X39	BANK 1, R38 TBDT	Bit Name	DTB[9]	DTB[8]	DTB[7]	DTB[6]	DTB[5]	DTB[4]	DTB[3]	DTB[2]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X3B	BANK 1, R3B PRDxL	Bit Name	0	0	0	0	PRDB[1]	PRDB[0]	PRDA[1]	PRDA[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	P	P	P	P	P	P
0X3C	BANK 1, R3C DTxL	Bit Name	0	0	0	0	DTB[1]	DTB[0]	DTA[1]	DTA[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	P	P	P	P	P	P

6.11.3 The Status of RST, T, and P of STATUS Register

A RESET condition is initiated by the following events:

1) A power-on condition,
2) A high-low-high pulse on /RESET pin, and
3) Watchdog timer time-out.

The values of T and P as listed in the following table are used to check how the processor wakes up.

■ Values of RST, T, and P after RESET:

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	P*	P*
/RESET wake-up during SLEEP mode	1	0
WDT during Operating mode	0	P*
WDT wake-up during SLEEP mode	0	0
Wake-Up on pin change during SLEEP mode	1	0

* *Previous status before reset*

The table below shows the events that may affect the status of T and P.

■ Status of T and P Being Affected by Events:

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	P*
SLEP instruction	1	0
Wake-Up on pin change during SLEEP mode	1	0

* *Previous status before reset*

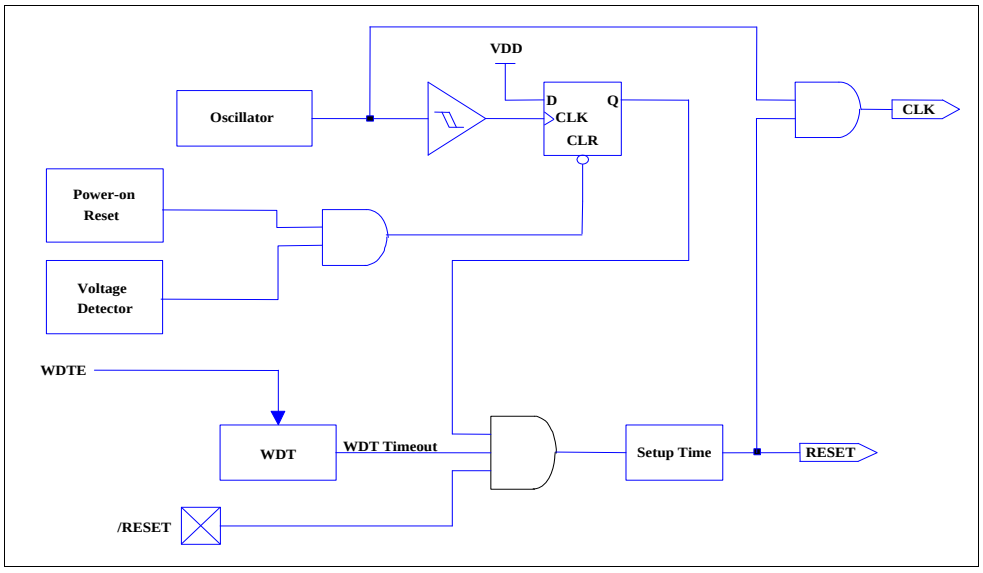


Figure 6-24 Controller Reset Block Diagram

6.12 Interrupt

6.12.1 Interrupt for EM78F644/642/641/544/542/541N

■ The **EM78F644/544N** has 13 interrupts (3 external, 10 internal) as listed below**:**

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI +ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
Internal	SPI	ENI + SPIIE=1	SPIIF	0012	4
External	Comparator2	ENI+CMP2IE=1	CMP2IF	0015	5
Internal	TC1	ENI + TC1IE=1	TC1IF	0018	6
Internal	UART Transmit	ENI + UTIE=1	TBEF	001B	7
Internal	UART Receive	ENI + URIE=1	RBFF	001E	8
Internal	UART Receive error	ENI+UERRIE=1	UERRIF	0021	9
Internal	TC2	ENI + TC2IE=1	TC2IF	0024	10
Internal	TC3	ENI + TC3IE=1	TC3IF	0027	11
Internal	PWMA	ENI+PWMAIE=1	PWMAIF	002A	12
Internal	PWMB	ENI+PWMBIE=1	PWMBIF	002D	13

■ The **EM78F642/542N** has 6 interrupts (3 external, 3 internal) listed below**:**

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI +ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
External	Comparator2	ENI+CMP2IE=1	CMP2IF	0015	4
Internal	TC2	ENI + TCIE2=1	TCIF2	0024	5
Internal	TC3	ENI + TCIE3=1	TCIF3	0027	6

■ The **EM78F641/541N** has 5 interrupts (3 external, 2 internal) as listed below**:**

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI +ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
External	Comparator 2	ENI+CMP2IE=1	CMP2IF	0015	4
Internal	TC3	ENI + TC3IE=1	TC3IF	0027	5

RE and RF are the Interrupt Status registers that record the interrupt requests in the relative flags/bits. IOCE and IOCF are the Interrupt Mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from their individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF and RE) is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

The external interrupt is equipped with an on-chip digital noise rejection circuit (input pulse of less than **8 system clock time** is eliminated as noise), **but in Low Crystal oscillator (LXT) mode, the noise rejection circuit is disabled**. When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 & R4 registers are saved by hardware. If another interrupt occurs, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, ACC, R3, and R4 will be pushed back.

6.12.2 Interrupt for EM78F648/548N

■ The **EM78F648/548N** has 18 interrupts (4 external, 14 internal) listed below**:**

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI +ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
Internal	LVD	ENI+LVDEN & LVDIE=1	LVDIF	000C	4
External	Comparator1	ENI+CMP1IE=1	CMP1IF	000F	5
Internal	SPI	ENI + SPIIE=1	SPIIF	0012	6
External	Comparator2	ENI+CMP2IE=1	CMP2IF	0015	7
Internal	TC1	ENI + TC1IE=1	TC1IF	0018	8
Internal	UART Transmit	ENI + UTIE=1	TBEF	001B	9
Internal	UART Receive	ENI + URIE=1	RBFF	001E	10
Internal	UART Receive error	ENI+UERRIE=1	UERRIF	0021	11
Internal	TC2	ENI + TC2IE=1	TC2IF	0024	12
Internal	TC3	ENI + TC3IE=1	TC3IF	0027	13
Internal	PWMA	ENI+PWMAIE=1	PWMAIF	002A	14
Internal	PWMB	ENI+PWMBIE=1	PWMBIF	002D	15
Internal	I2C Transmit	ENI+ I2CTIE	I2CTIF	0036	16
Internal	I2C Receive	ENI+ I2CRIE	I2CRIF	0039	17
Internal	I2C Stop	ENI+ I2CSTPIE	I2CSTPIF	003F	18

Bank0 RC~RF are the Interrupt Status registers that record the interrupt requests in the relative flags/bits. Bank0 R1C~R1F is the Interrupt Mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from their individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit delete) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

The External interrupt is equipped with digital noise rejection circuit (input pulse of less than **8 system clocks time** is eliminated as noise), **but in Low XTAL oscillator (LXT) mode the noise rejection circuit is disabled.** When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 & R4 registers are saved by hardware. If another interrupt occurs, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, ACC, R3, and R4 will be pushed back.

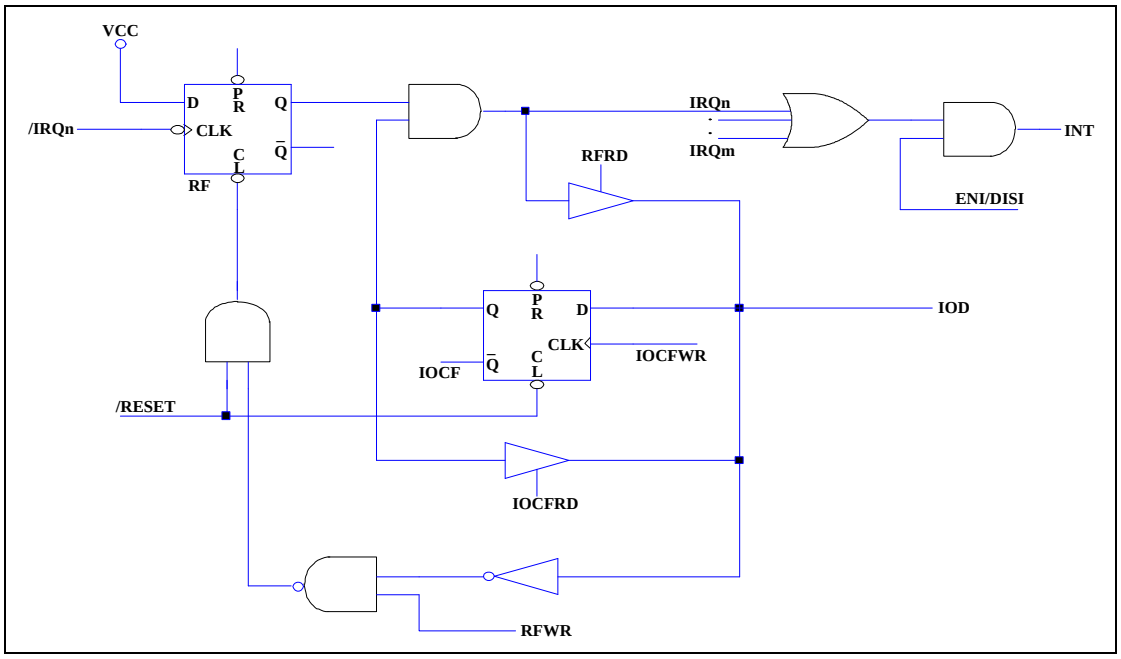


Figure 6-25a Interrupt Input Circuit Diagram

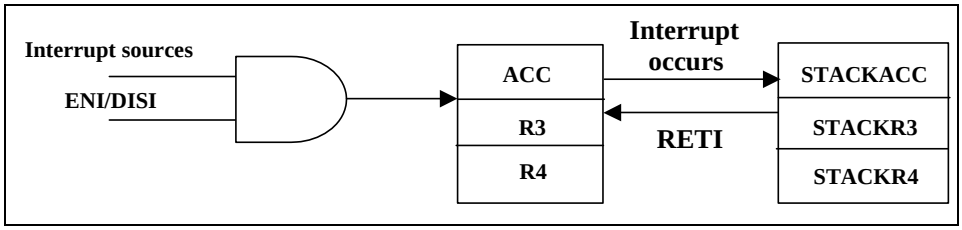


Figure 6-25b Interrupt Backup Diagram

6.13 LVD (Low Voltage Detector) for EM78F648/548N

When an unstable power source condition occurs, such as external power noise interference or EMS test condition, a violent power vibration is generated. At the same time, the Vdd becomes unstable as it maybe operating below working voltage. When the system is operating under low voltage condition, the IC kernel will automatically keep all register status.

6.13.1 LVD Level Control

LVD property is set at Bank0 R12 (Section 6.3.15). Bits 1 & 0 operation mode is as follows.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	LVDEN	/LVD	LVD1	LVD0

Bits 1~Bit 0 (LVD1~LVD0): Low Voltage Detect level control bits

6.13.2 LVD Interrupt

The LVD status and interrupt flag refers to Bank0 RC (Section 6.3.9) and Bank0 R1C (Section 6.3.20). Their respective Bit 7 operation mode is as follows.

■ LVD Interrupt Flag (Bank0 RC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIF	0	SPIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF

Bit 7 (LVDIF): Low voltage Detector interrupt flag.

When LVD1, LVD0 = “0,0”, Vdd > 2.2V, LVDIF is “0”, Vdd<= 2.2V, set LVDIF to “**1**”. LVDIF reset to “**0**” by software.

When LVD1, LVD0 = “0,1”, Vdd > 3.3V, LVDIF is “0”, Vdd<= 3.3V, set LVDIF to “**1**”. LVDIF reset to “**0**” by software.

When LVD1, LVD0 = “1,0”, Vdd > 4.0V, LVDIF is “0”, Vdd<= 4.0V, set LVDIF to “**1**”. LVDIF reset to “**0**” by software.

When LVD1, LVD0 = “1,1”, Vdd > 4.5V, LVDIF is “0”, Vdd<= 4.5V, set LVDIF to “**1**”. LVDIF reset to “**0**” by software.

■ LVD Interrupt Enable (Bank0 R1C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	0	SPIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE

Bits 7 (LVDIE): LVDIF interrupt enable bit

0: Disable LVDIF interrupt

1: Enable LVDIF interrupt

6.13.3 LVD Function Setup

To setup the LVD function, perform the following steps:

1) Set the LVDEN to “**1**”, then use Bits 1,0 (LVD1, LVD0) of Register RB to set LVD interrupt level
2) Enable LVDIE
3) Wait for the LVD interrupt to occur
4) Clear LVD interrupt flag

NOTE

- *The internal LVD module uses the internal circuit to match low voltage detection. When the LVDEN is set to enable the LVD module, the current consumption will increase about 10uA.*
- *During the Sleep mode, the LVD module continues to operate. If the device voltage drops slowly and crosses the detection point, the LVDIF bit will be set and the device will not wake-up from Sleep mode. Until the other wake-up sources wake-up EM78F648/548N, the LVD interrupt flag setting will remain at priority status.*
- *When system resets, the LVD flag is cleared.*

Figure 6-26 below shows the LVD module detection point in an external voltage condition.

- When Vdd drops but above VLVD, LVDIF is kept at "**0**".
- When Vdd drops below VLVD, LVDIF is set to "**1**". If the global ENI is enabled, LVDIF is also set to "**1**" and the next instruction will branch to interrupt vector. The LVD interrupt flag is cleared to "**0**" by software.
- When Vdd drops below VRESET at less than 80us, the system will keep all the register status and halts its operation, but oscillation remains active.
- When Vdd drops below VRESET at more than 80us, system RESET will occur.

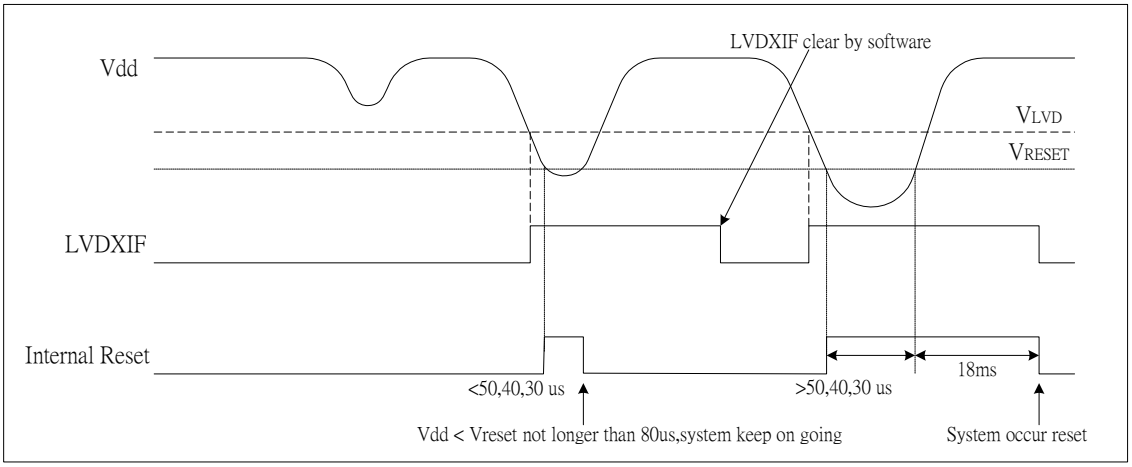


Figure 6-26 LVD Waveform Characteristics Showing Detection Point in an External Voltage Condition

6.14 DATA EEPROM

The Data EEPROM is readable and writable during normal operation over the whole Vdd range. The operation for Data EEPROM is base on a single byte. A write operation makes an erase-then-write cycle to take place on the allocated byte.

The DATA EEPROM memory provides the high erase and writes cycles. A byte write automatically erases the location and write the new value.

The following are the steps to write to or read data from the EEPROM**:**

1) Set the **EEPC** bit to "**1**" for enable EEPROM power

2) Write the address to EERA8~EERA0 (512 bytes EEPROM address)

3) A. ● Set the **EEWE** bit to "**1**", if the write function is employed
   ● Write the 8-bit value of the data to be programmed (256 bytes EEPROM data)
   ● Set the **WR** bit to "**1**", then; execute write function
   B. Set the **RD** bit to "**1**", then; execute read function

4) A. Wait for the **EEDF** or **WR** to be cleared
   B. Wait for the **EEDF** to be cleared

5) For the next conversion, go to Step 2 as required

6) To save power and make sure the EEPROM are data not used, clear the **EEPC**.

6.15 Oscillator

6.15.1 Oscillator Modes

The EM78F64x/F54xN can be operated in the four different oscillator modes, such as Internal RC oscillator mode (IRC), External RC oscillator mode (ERC), High XTAL oscillator mode (HXT), and Low XTAL oscillator mode (LXT). You can select one of them by programming OSC2, OCS1, and OSC0 in the CODE Option register. The following table depicts how these four modes are defined.

The maximum operation frequency of crystal/resonator under different VDD voltages listed in the table on next page.

■ Oscillator Modes defined by OSC2 ~ OSC0

Mode	OSC2	OSC1	OSC0
XT (XTAL Oscillator mode)	0	0	0
HXT (High XTAL Oscillator mode)	0	0	1
LXT1 (Low XTAL1 Oscillator mode)	0	1	0
LXT2 (Low XTAL2 Oscillator mode)	0	1	1
IRC mode, OSCO (P54) acts as I/O pin	1	0	0
IRC mode, OSCO (P54) acts as RCOUT pin	1	0	1
ERC mode, OSCO (P54) acts as I/O pin	1	1	0
ERC mode, OSCO (P54) acts as RCOUT pin	1	1	1

In LXT1, LXT2, XT, HXT, and ERC modes, OSCI and OSCO are used. These pins can't be used as normal I/O pin. In IRC mode, P55 is used as normal I/O pin

NOTE

1. Frequency range of HXT mode is 20MHz ~ 6MHz.
2. Frequency range of XT mode is 6MHz ~ 1MHz.
3. Frequency range of LXT1 mode is 1MHz ~ 100kHz.
4. Frequency range of XT mode is 32kHz.

■ Summary of Maximum Operating Speed:

Conditions	VDD	Fxt Max.(MHz)
Two cycles with two clocks	2.5	4.0
	3.0	8.0
	5.0	20.0

6.15.2 Crystal Oscillator/Ceramic Resonators (XTAL)

EM78F64x/54xN can be driven by an external clock signal through the OSCI pin as illustrated below.

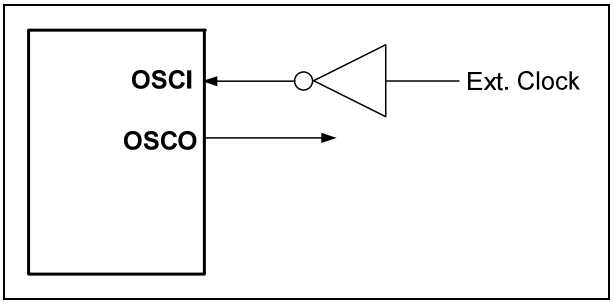


Figure 6-27a External Clock Input Circuit

In most applications, Pins OSCI and OSCO are connected with a crystal or ceramic resonator to generate oscillation as depicted in the circuit diagram below. The same thing applies under HXT or LXT mode. The following table (next page) provides the recommended values for C1 and C2. Since each resonator has its own attribute, you should refer to the pertinent resonator specification for appropriate C1/C2 values. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

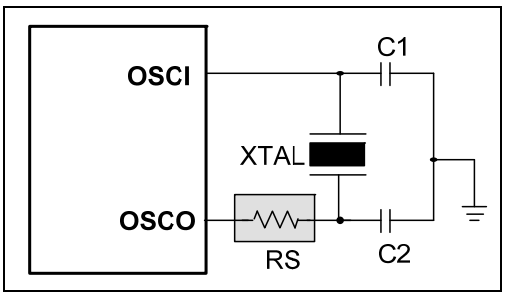


Figure 6-27b Crystal/Resonator Circuit

■ Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator:

Oscillator Type	Frequency Mode	Frequency	C1(pF)	C2(pF)
Ceramic Resonators	HXT	455 kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100KHz	25	25
		200KHz	25	25
	HXT	455KHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15

6.15.3 External RC Oscillator Mode

For some applications that do not require a very precise timing calculation, the use of RC oscillator (see figure below) offers a lot of cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by such factors as supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variations.

In order to maintain a stable system frequency, the values of the Cext should be more than 20pF, and that the value of Rext should be less than 1 MΩ. If the values cannot be kept within the prescribed range, the frequency can be easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the way the PCB is layout, could affect the system frequency.

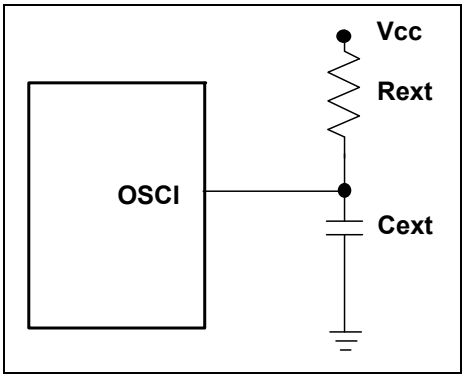


Figure 6-28 Circuit for External RC Oscillator Mode

■ RC Oscillator Frequencies:

Cext	Rext	Average Fosc 5V,25°C	Average Fosc 3V,25°C
20 pF	3.3k	3.5 MHz	3.2 MHz
	5.1k	2.5 MHz	2.3 MHz
	10k	1.30 MHz	1.25 MHz
	100k	140 KHz	140 KHz
100 pF	3.3k	1.27 MHz	1.21 MHz
	5.1k	850 KHz	820 KHz
	10k	450 KHz	450 KHz
	100k	48 KHz	50 KHz
300 pF	3.3k	560 KHz	540 KHz
	5.1k	370 KHz	360 KHz
	10k	196 KHz	192 KHz
	100k	20 KHz	20 KHz

NOTE

1. Data obtained from DIP packages measurement.

2. Data provided for design reference only.

6.15.4 Internal RC Oscillator Mode

The EM78F64x/54xN series MUCs offer a versatile internal RC mode with default frequency value of 4MHz. The internal RC oscillator mode has other frequencies (4MHz, 16MHz, 8MHz, & 455kHz), that can be set by CODE OPTION: RCM1 and RCM0. All these four main frequencies can be calibrated by programming the CODE OPTION Bits C4~C0. The following table shows a typical drift rate of the calibration.

■ **F644/544N** Internal RC Drift Rate (Ta=25°C, VDD=5 V± 5%, VSS=0V):

Internal RC	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.4V~5.5V)	Process	Total
4 MHz	± 3%	± 5%	± 2.5%	± 10.5%
16 MHz*	± 3%	± 5%	± 2.5%	± 10.5%
8 MHz	± 3%	± 5%	± 2.5%	± 10.5%
455kHz	± 3%	± 5%	± 2.5%	± 10.5%

**16 MHz Operating Temperature: -40℃ ~ 50℃*

■ **F642/542N** Internal RC Drift Rate (Ta=25°C, VDD=5 V± 5%, VSS=0V):

Internal RC	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.4V~5.5V)	Process	Total
1MHz	± 5%	± 4%	± 2.5%	± 11.5%
4MHz	± 5%	± 4%	± 2.5%	± 11.5%
8MHz	± 5%	± 5%	± 2.5%	± 12.5%
16MHz	± 5%	± 5%	± 2.5%	± 12.5%

■ **F641/541N** Internal RC Drift Rate (Ta=25°C, VDD=5 V± 5%, VSS=0V)**:**

Internal RC	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.4V~5.5V)	Process	Total
4 MHz	± 3%	± 5%	± 2.5%	± 10.5%
16 MHz	± 3%	± 5%	± 2.5%	± 10.5%
8 MHz	± 3%	± 5%	± 2.5%	± 10.5%

■ **F648/548N** Internal RC Drift Rate (Ta=25°C , VDD=5 V± 5%, VSS=0V)**:**

Internal RC Frequency	Drift Rate			
	Temperature (-40°C+85°C)	Voltage (2.2V~5.5V)	Process	Total
455kHz	±5%	±5%	±4%	±14%
4MHz	±5%	±5%	±4%	±14%
8MHz	±5%	±5%	±4%	±14%
16MHz	±5%	±5%	±4%	±14%

6.16 Power-On Considerations

Any microcontroller is not guaranteed to start operating properly before the power supply reaches its steady state. EM78F64x/54xN is equipped with aPower-On Voltage Detector (POVD) with a detecting level of 2.0V. Power will work normally if the Vdd rises fast enough (50ms or less). However, in critical applications, extra devices are still required to assist in solving power-up problems.

6.17 External Power-On Reset Circuit

The circuit diagram shown below implements an external RC to generate the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reached minimum operational voltage. Apply this circuit when the power supply has a slow rise time. Since the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40KΩ in order for the /RESET pin voltage is remain at below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing into /RESET pin.

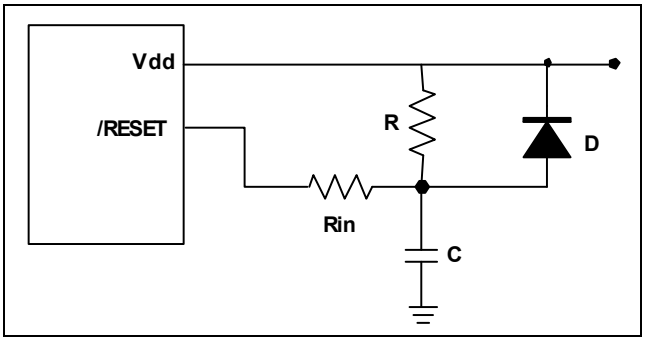


Figure 6-29 External Power-Up Reset Circuit

6.18 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trips below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figures 6-30a and 6-30b below show how to accomplish a proper residue-voltage protection circuit.

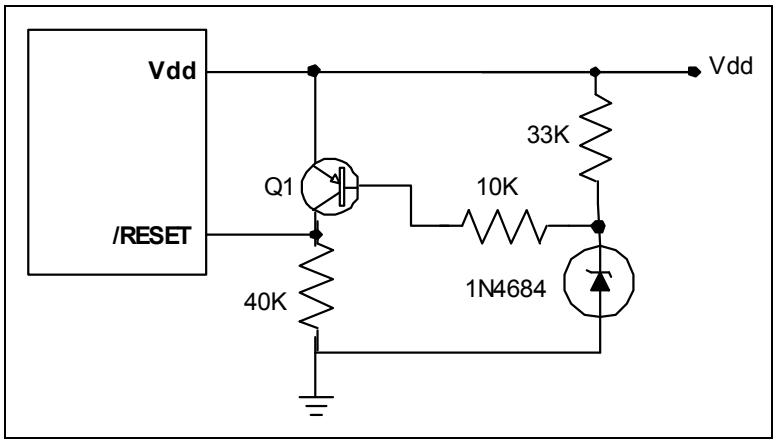


Figure 6-30a Circuit 1 for the Residue Voltage Protection

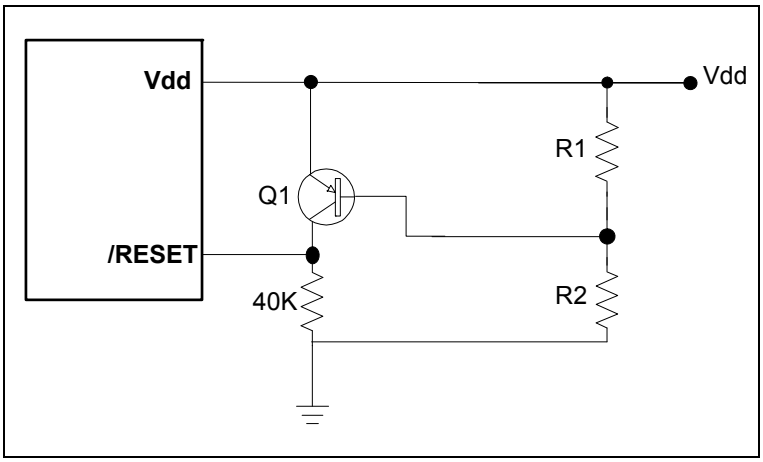


Figure 6-30b Circuit 2 for the Residue Voltage Protection

6.19 Code Option Register

The EM78F648/644/642/641/548/544/542/541N has a Code Option Word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Their respecrtive Code Option Register and Customer ID Register arrangement distribution are as follows:

■ **EM78F644/642/641/544/542/541N**

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

■ **EM78F648/548N**

Word 0	Word 1	Word 2
Bit 14~Bit 0	Bit 14~Bit 0	Bit 14~Bit 0

6.19.1 Code Option Register (Word 0)

6.19.1.1 EM78F644/642/641/544/542/541N Code Option Word 0

Word 0												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	NRHL	NRE	RESET ENB	CLKS1	CLKS0	EN WDTB	OSC2	OSC1	OSC0	Protect		

Bit 12: Not used, set to "**0**" all the time

Bit 11 (NRHL): Noise Rejection High/Low Pulse Define bit. INT pin is a falling edge trigger.

0: Pulses equal to 32/fc [s] is regarded as signal (default)

1: Pulses equal to 8/fc [s] is regarded as signal

NOTE

The noise rejection function is turned off in the LXT2 and in Sleep mode.

Bit 10 (NRE): Noise Rejection Enable bit. INT pin is a falling edge trigger.

0: Enable noise rejection (default)

1: Disable noise rejection

Note that in Low Crystal oscillator (LXT2) mode, the noise rejection circuit is always disabled

Bit 9 (RESETENB): Reset Pin Enable Bit

0: P83 set to I/O pin (default)

1: P83 set to /RESET pin

NOTE

The "RESETENB" bit is NOT available from EM78F644/544N

Bit 8 ~ Bit 7 (CLKS1 ~ CLKS0): Instruction period option bit

Instruction Period	CLKS1	CLKS0
4 clocks (default)	**0**	**0**
2 clocks	**0**	**1**
8 clocks	**1**	**0**
16 clocks	**1**	**1**

Refer to the Instruction Set in Section 6.20 below.

NOTE

ELAN UICE only supports the 2 or 4 clocks instruction period.

Bit 6 (ENWDTB): Watchdog Timer Enable bit

0: Disable (default)

1: Enable

Bit 5 ~ Bit 3 (OSC2 ~ OSC0): Oscillator Mode selection bits

Oscillator Modes as defined by OSC2 ~ OSC0**:**

Mode	OSC2	OSC1	OSC0
XT[1] (Crystal oscillator mode) (default)	0	0	0
HXT[2] (High Crystal oscillator mode)	0	0	1
LXT1[3] (Low Crystal 1 oscillator mode)	0	1	0
LXT2[4] (Low Crystal 2 oscillator mode)	0	1	1
IRC (Internal RC oscillator mode); P55, P54 act as I/O pin	1	0	0
IRC (Internal RC oscillator mode); P55 act as I/O pin P54 act as RCOUT pin	1	0	1
ERC (External RC oscillator mode); P55 act as ERCin pin P54 act as I/O pin	1	1	0
ERC (External RC oscillator mode); P55 act as ERCin pin P54 act as RCOUT pin with Open-Drain	1	1	1

[1] *Frequency range of XT mode is 6 MHz ~ 1 MHz.*
[2] *Frequency range of HXT mode is 16 MHz ~ 6 MHz.*
[3] *Frequency range of LXT1 mode is 1 MHz ~ 100kHz.*
[4] *Frequency range of LXT2 mode is 32kHz.*

Bit 2 ~ Bit 0 (Protect): Protect select bit as shown below**:**

Protect	Protect
1	Enable
0	Disable

6.19.1.1 EM78F648/548 Code Option Word 0

Word 0														
Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
COBS0	-	-	CLKS0	-	-	LVR1	LVR0	RESETEN	ENWDT	NRHL	NREB	Protect		

Bit 14 (COBS0): IRC mode selection bit

0: Select IRC frequency from code option

1: Select IRC frequency from register

Bits 13~12: Not used, set to "**0**" all the time.

Bits 11(CLKS0): Instruction period option bits

Instruction Period	CLKS0
4 clocks	**0**
2 clocks	**1**

Bits 10~9: Not used, set to "**0**" all the time.

Bits 8~7(LVR1~LVR0): Low voltage reset enable bit

LVR1, LVR0	VDD reset level
00	NA
01	2.7V
10	3.7V
11	4.2V

Bit 6 (RESETEN): P83//RST pin selection bit

0: P83 pin

1: /RST pin

Bit 5(ENWDT): WDT enable bit

0: Disable

1: Enable

Bit 4(NRHL): Noise rejection high/low pulse definition bit

0: Pulses equal to 32/fc [s] is regarded as signal

1: Pulses equal to 8/fc [s] is regarded as signal

Bit 3(NREB): Noise rejection enable bit

0: Enable

1: Disable

Bits 2~0 (Protect): Protect bits

Protect	Protect
1	Enable
0	Disable

6.19.2 Code Option Register (Word 1)

6.19.2.1 EM78F644/642/641/544/542/541N Code Option Word 1

Word 1												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
COBS0	TCEN	"0"	"1"	C4	C3	C2	C1	C0	RCM1	RCM0	LVR1	LVR0

Bit 12 (COBS0): IRC mode selection bit

0: Select IRC frequency from code option (default)

1: Select IRC frequency from register

Bit 11 (TCEN): TCC enable bit

0: P77/TCC is set as P77 (default)

1: P77/TCC is set as TCC.

NOTE

TCEN must be set to"0" in EM78F641/541N

Bit 10: Not used, set to "**0**" all the time.

Bit 9: Not used, set to "**1**" all the time.

Bit 8 ~ Bit 4 (C4 ~ C0): Internal RC mode calibration bits.
C4 ~ C0 must be set to "**0**" only (auto-calibration).

Bit 3 ~ Bit 2 (RCM1 ~ RCM0): RC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
0	**0**	4 (default)
0	**1**	16
1	**0**	8
1	**1**	455kHz

NOTE

The frequency 455kHz is NOT available from EM78F641/541N

Bit 1 ~ Bit 0 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1	LVR0	Reset Level	Release Level
0	**0**	NA	NA
0	**1**	2.7V	2.9V
1	**0**	3.5V	3.7V
1	**1**	4.0V	4.2V

LVR1, LVR0="0, 0": LVR is disabled. The IC power-on reset is 2.0~2.1V (default).

LVR1, LVR0="0, 1": If Vdd < 2.7V, the IC will reset.

LVR1, LVR0="1, 0": If Vdd < 3.5V, the IC will reset.

LVR1, LVR0="1, 1": If Vdd < 4.0V, the IC will reset.

6.19.2.2 EM78F648/548N Code Option Word 1

Word 1														
Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HLFS	-	SHE	C4	C3	C2	C1	C0	RCM1	RCM0	-	OSC2	OSC1	OSC0	RCOD

Bit 14(HLFS): Initialize CPU operation mode

0: Normal mode

1: Green mode

Bit 13: Not used, set to "**1**" all the time.

Bit 12 (SHE): System halt enable bit.

0: Disable

1: Enable

Bits 11~7(C4~C0): IRC trim bits. This part will be auto setup by the writer

Bits 6~5 (RCM1~RCM0): IRC frequency selection bits

RCM 1	RCM 0	Frequency (MHz)
0	**0**	4 (default)
0	**1**	16
1	**0**	8
1	**1**	455kHz

Bit 4: Not used, set to "**1**" all the time.

Bits 3~1 (OSC2~OSC0): Oscillator mode selection bits

Mode	OSC2	OSC1	OSC0
XT (XTAL oscillator mode)	**0**	**0**	**0**
HXT (High XTAL oscillator mode)	**0**	**0**	**1**
LXT1 (Low XTAL1 oscillator mode)	**0**	**1**	**0**
LXT2 (Low XTAL2 oscillator mode)	**0**	**1**	**1**
IRC mode, OSCO (P54) act as I/O pin	**1**	**0**	**0**
IRC mode, OSCO (P54) act as RCOUT pin	**1**	**0**	**1**
ERC mode, OSCO (P54) act as I/O pin	**1**	**1**	**0**
ERC mode, OSCO (P54) act as RCOUT pin	**1**	**1**	**1**

Bit 0 (RCOD): Oscillator output or I/O port selection bit

RCOD	Pin Function
1	OSCO pin is open drain
0	OSCO output system clock (default)

6.19.3 Customer ID Register (Word 2)

6.19.3.1 EM78F644/642/641/544/542/541N Code Option Word 2

Word 2											
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SC3	SC2	SC1	SC0	“0”	“1”	“0”	“0”	ID4	ID3	ID2	ID1	ID0

Bits 12 ~ 9 (SC3 ~ SC0): Calibrator of sub frequency (WDT frequency, auto calibration)

Bit 8: Not used, set to “**0**” all the time.

Bit 7: Not used, set to “**1**” all the time.

Bits 6 ~ 5: Not used, set to “**0**” all the time.

Bits 4 ~ 0 (ID4 ~ ID0): Customer’s ID code.

6.19.3.2 EM78F648/548N Code Option Word 2

Word 1													
Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SC3	SC2	SC1	SC0	“0”	“0”	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Bits 14 ~ 11 (SC3 ~ SC0): Calibrator of sub frequency (WDT frequency, auto calibration)

Bits 10 ~ 9: Not used, set to “0” all the time.

Bits 8 ~ 0 (ID8 ~ ID0): Customer’s ID code.

6.20 Instruction Set

Each instruction in the Instruction Set is a 13-bit word for EM78F664N/F662N/F661N /F564N/F562N/F561N and 15-bit for EM78F648/548N, divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instructions "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A", "BS(C) R2,6", "CLR R2", ·etc.). Under this condition, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitableyou’re your certain applications, try to modify the instruction as follows**:**

A) Change one instruction cycle to consist of four oscillator periods.

B) "LJMP", "LCALL", "TBRD", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case (A) is selected by the Code Option bit called CLK1:0. One instruction cycle consists of two oscillator clocks if CLK1:0 is ”01”, and four oscillator clocks if CLK1:0 is ”00”.

Note that once the four oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK = Fosc/4, instead of Fosc/2, as indicated in Figure 6-11 in Section 6.4, TCC/WDT and Prescaler.

In addition, the Instruction Set also has the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.
2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

In addition, the instruction set has the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.
2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

6.20.1 Instruction Set Table

In the following symbols are used in the Instruction Set table shown below**:**

"**R**" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction.

"**b**" represents a bit field designator that selects the value for the bit which is located in the register "**R**", and affects operation.

"**k**" represents an 8 or 10-bit constant or literal value.

■ Instruction Set table

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000 000 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001 000 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None[1]
0 0000 0000 0011 000 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100 000 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None [1, 2]
0 0000 0001 0000 000 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001 000 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010 000 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011 000 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None[1]
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None[1, 2]
0 0000 01rr rrrr 000 0001 rrrr rrrr	00rr 01rr	MOV R,A	A → R	None
0 0000 1000 0000 000 0010 0000 0000	0080 0200	CLRA	0 → A	Z
0 0000 11rr rrrr 000 0011 rrrr rrrr	00rr 03rr	CLR R	0 → R	Z
0 0001 00rr rrrr 000 0100 rrrr rrrr	01rr 04rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr 000 0101 rrrr rrrr	01rr 05rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr 000 0110 rrrr rrrr	01rr 06rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr 000 0111 rrrr rrrr	01rr 07rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr 000 1000 rrrr rrrr	02rr 08rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr 000 1001 rrrr rrrr	02rr 09rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr 000 1010 rrrr rrrr	02rr 0Arr	AND A,R	A & R → A	Z
0 0010 11rr rrrr 000 1011 rrrr rrrr	02rr 0Brr	AND R,A	A & R → R	Z
0 0011 00rr rrrr 000 1100 rrrr rrrr	03rr 0Crr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr 000 1101 rrrr rrrr	03rr 0Drr	XOR R,A	A ⊕ R → R	Z

(Continuation)

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0011 10rr rrrr 000 1110 rrrr rrrr	03rr 0Err	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr 000 1111 rrrr rrrr	03rr 0Frr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr 001 0000 rrrr rrrr	04rr 10rr	MOV A,R	R → A	Z
0 0100 01rr rrrr 001 0001 rrrr rrrr	04rr 11rr	MOV R,R	R → R	Z
0 0100 10rr rrrr 001 0010 rrrr rrrr	04rr 12rr	COMA R	/R → A	Z
0 0100 11rr rrrr 001 0011 rrrr rrrr	04rr 13rr	COM R	/R → R	Z
0 0101 00rr rrrr 001 0100 rrrr rrrr	05rr 14rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr 001 0101 rrrr rrrr	05rr 15rr	INC R	R+1 → R	Z
0 0101 10rr rrrr 001 0110 rrrr rrrr	05rr 16rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr 001 0111 rrrr rrrr	05rr 17rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr 001 1000 rrrr rrrr	06rr 18rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr 001 1001 rrrr rrrr	06rr 19rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr 001 1010 rrrr rrrr	06rr 1Arr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr 001 1011 rrrr rrrr	06rr 1Brr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr 001 1100 rrrr rrrr	07rr 1Crr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr 001 1101 rrrr rrrr	07rr 1Drr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr 001 1110 rrrr rrrr	07rr 1Err	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr 001 1111 rrrr rrrr	07rr 1Frr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr 010 0bbb rrrr rrrr	0xxx 2xrr	BC R,b	0 → R(b)	None[3]
0 101b bbrr rrrr 010 1bbb rrrr rrrr	0xxx 2xrr	BS R,b	1 → R(b)	None[4]
0 110b bbrr rrrr 011 0bbb rrrr rrrr	0xxx 3xrr	JBC R,b	if R(b)=0, skip	None

(Continuation)

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 111b bbrr rrrr 011 1bbb rrrr rrrr	0xxx 3xrr	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk 100 kkkk kkkk kkkk	1kkk 4kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk 101 kkkk kkkk kkkk	1kkk 5kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk 110 0000 kkkk kkkk	18kk 60kk	MOV A,k	k → A	None
1 1001 kkkk kkkk 110 0100 kkkk kkkk	19kk 64kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk 110 1000 kkkk kkkk	1Akk 68kk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk 110 1100 kkkk kkkk	1Bkk 6Ckk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk 111 0000 kkkk kkkk	1Ckk 70kk	RETL k	k → A, [Top of Stack] ® PC	None
1 1101 kkkk kkkk 111 0100 kkkk kkkk	1Dkk 74kk	SUB A,k	k-A → A	Z, C, DC
1 1111 kkkk kkkk 111 1100 kkkk kkkk	1Fkk 7Ckk	ADD A,k	k+A → A	Z, C, DC
1 1110 1001 kkkk	1E9k	BANK k	K → R4(7:6)	None[1]
111 1010 1000 kkkk	7A0k	SBANK k	K → R1(4)	None[5]
111 1010 0100 kkkk	7A4k	GBANK k	K → R1(0)	None[5]
1 1110 1010 kkkk k kkkk kkkk kkkk 111 1010 1000 kkkk kkk kkkk kkkk kkkk	1EAk kkkk 7A8k kkkk	LCALL k	Next instruction : k kkkk kkkk kkkk PC+1 → [SP], k → PC	None
1 1110 1011 kkkk k kkkk kkkk kkkk 111 1010 1100 kkkk kkk kkkk kkkk kkkk	1EBk kkkk 7ACk kkkk	LJMP k	Next instruction: k kkkk kkkk kkkk k → PC	None
1 1110 11rr rrrr 111 1011 rrrr rrrr	1Err 7Brr	TBRD R	ROM[(TABPTR)] → R	None

[1] *This instruction is applicable to EM78F644/642/641/544/542/541N only.*

[2] *This instruction is applicable to IOC5~IOC7, IOCA ~ IOCF only.*

[3] *This instruction is not recommended for Interrupt Status Register operation.*

[4] *This instruction cannot operate under Interrupt Status Register.*

[5] *This instruction is applicable to EM78F648/548N only.*

7 Timing Diagram

7.1 AC Test Input/Output Waveform

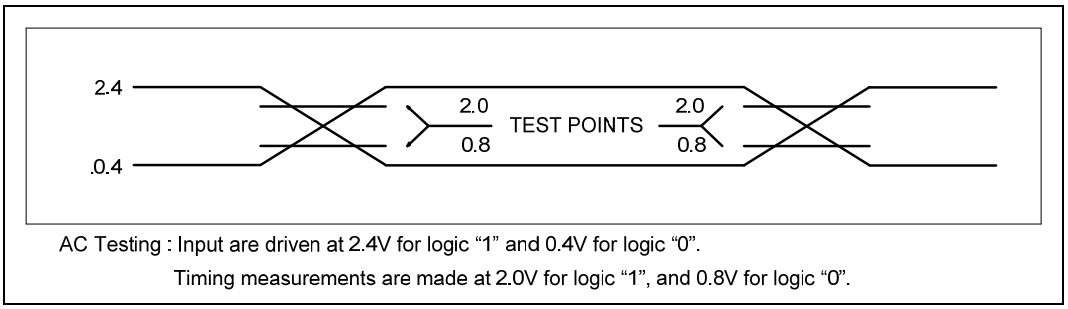


Figure 7-1a AC Test Timing Diagram

7.2 Reset Timing (CLK1:0 = "01")

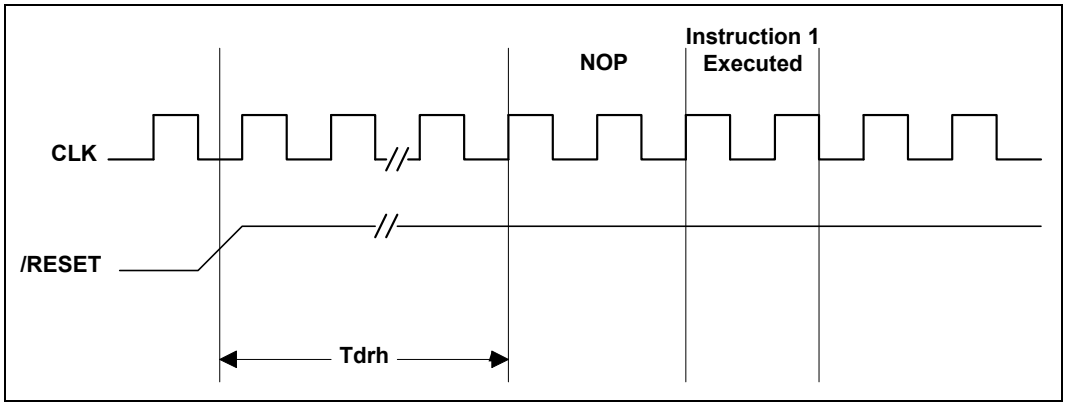


Figure 7-1b Reset Timing Diagram

8 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Working voltage	2.2V	to	5.5V
Working frequency	DC	to	16 MHz
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V

NOTE

These parameters are theoretical values only and have not been tested or verified,

9 DC Electrical Characteristics

9.1 For EM78F648/548N

■ Ta=25°C, VDD=5.0V±5%, VSS=0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	XTAL: VDD to 3V	Two cycle with two clocks	DC	–	8	MHz
	XTAL: VDD to 5V		DC	–	16	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F-30%	370	F+30%	KHz
	IRC: VDD to 5 V	4MHz, 1MHz, 455KHz, 8MHz	F-2.5%	F	F+2.5%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-	-	±1	μA
IRC1	IRC:VDD to 5V	RCM0:RCM1=1:1	2.9	4	5.7	MHz
IRCE	Internal RC oscillator error per stage	-	±4.3	±4.5	±4.7	%
IRC2	IRC:VDD to 5V	RCM0:RCM1=1:0	5.8	8	11.4	MHz
IRC3	IRC:VDD to 5V	RCM0:RCM1=0:1	0.725	1	1.425	MHz
IRC4	IRC:VDD to 5V	RCM0:RCM1=0:0	330	455	645	KHz
VIHRC	Input High Threshold Voltage (Schmitt trigger)	OSCI in RC mode	3.9	4	4.1	V
IERC1	Sink current	VI from low to high , VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt trigger)	OSCI in RC mode	1.7	1.8	1.9	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8, 9	0.7Vdd	-	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8, 9	-0.3V	-	0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.7Vdd	-	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V	-	0.3Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC,INT	0.7Vdd	-	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC,INT	-0.3V	-	0.3Vdd	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V
IOH1	Output High Voltage (Ports 5, 6,7,8,9)	VOH = VDD-0.5V (IOH =3.7mA)	-4.1	-4.45	-5	mA
IOL1	Output Low Voltage (Ports 5, 6,7,8,9)	VOL = GND+0.5V (IOL =10mA)	11	12	13.5	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-70	-75	-80	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	35	40	45	μA

(Continuation)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ISB1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled	0.6	2.0	2.5	μA
ISB2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled	6	7	8	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT disabled	20	22	24	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT enabled	25	27	29	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled	1.5	1.6	1.7	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled	2.1	2.2	2.3	mA

NOTE

- *The parameters shown above are theoretical values only and have not been tested or verified.*
- *Data under "Min", "Typ", & "Max" columns are based on theoretical results at 25℃. These data are for design guidance only and have not been tested or verified.*

9.1.1 Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	–	–	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	100K	–	cycles

9.1.2 Data EEPROM Electrical Characteristics (for EM78F648N only)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.0~ 5.5V Temperature = -40°C ~ 85°C	–	6	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	1000K	–	cycles

9.1.3 Comparator Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage[1]	RL = 5.1K	–	–	10	mV
Vcm	Input common-mode voltages range[2]	–	GND	–	VDD	V
ICO	Supply current of Comparator	–	–	300	–	uA
TRS	Response time[3]	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load), Overdrive = 30mV	–	0.8	–	us
VS	Operating range	–	2.5	–	5.5	V

[1] *The output voltage is in the unit gain circuitry and over the full input common-mode range.*

[2] *The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is VDD.*

[3] *The response time specified is a 100 mV input step with 30 mV overdrive.*

9.2 For EM78F644/544N

■ Ta=25°C, VDD=5.0V±5%, VSS=0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	Crystal: VDD to 3V	Two cycles with two clocks	DC	–	8	MHz
	Crystal: VDD to 5V		DC	–	16	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 300 pF	F-30%	370	F+30%	kHz
	IRC: VDD to 5 V	4 MHz, 16 MHz, 8 MHz, 455kHz	F-2.5%	F	F+2.5%	Hz
IIL	Input Leakage Current for Input pins	VIN = VDD, VSS	–	–	±1	μA
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	3.5	–	V
IERC1	Sink current	VI from low to high, VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	1.5	–	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	0.7VDD	–	VDD+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	-0.3V	–	0.3VDD	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.7VDD	–	VDD+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	-0.3V	–	0.3VDD	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	0.7VDD	–	VDD+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT	-0.3V	–	0.3VDD	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	–	3.0	–	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	–	1.8	–	V

(Continuation)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = VDD-0.5V (IOH =3.7mA)	-3.3	-4.2	–	mA
IOL1	Output Low Voltage (Ports 5, 7, 8)	VOL = GND+0.5V	9	11	–	mA
IOL2	Output Low Voltage (Port 6)	VOL = GND+0.5V	14	18	–	mA
IPH	Pull-high current	Pull-high active, Input pin at VSS	–	-70	-80	μA
IPL	Pull-low current	Pull-low active, Input pin at Vdd	–	20	30	μA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1.0	1.5	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	8	10	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT disabled	–	39	42	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT enabled	–	39	42	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=455kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT enabled (*VDD = 3V)	–	110	120	μA
ICC4	Operating supply current at two clocks	/RESET = 'High', Fosc=455kHz (IRC type, CLKS1:0="01"), Output pin floating, WDT enabled (*VDD = 3V)	–	100	110	μA
ICC5	Operating supply current at two clocks	/RESET = 'High', Fosc = 4 MHz (Crystal type, CLKS1:0 = "01"), Output pin floating, WDT enabled	–	1.1	1.5	mA
ICC6	Operating supply current at two clocks	/RESET = 'High', Fosc = 10 MHz (Crystal type, CLKS1:0 = "01"), Output pin floating, WDT enabled	–	2.6	3	mA

NOTE

- *The parameters shown above are theoretical values only and have not been tested or verified.*
- *Data under "Min", "Typ", & "Max" columns are based on theoretical results at 25°C. These data are for design guidance only and have not been tested or verified.*

9.2.1 Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	–	–	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	100K	–	cycles

9.2.2 Data EEPROM Electrical Characteristics (for EM78F644N only)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.5~ 5.5V Temperature = -40°C ~ 85°C	–	4.5	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	1000K	–	cycles

9.2.3 Comparator Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage[1]	RL = 5.1K	–	–	10	mV
Vcm	Input common-mode voltages range[2]	–	GND	–	VDD	V
ICO	Supply current of Comparator	–	–	200	–	uA
TRS	Response time[3]	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load), Overdrive = 30mV	–	0.7	–	us
TLRS	Large signal response time	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load)	–	300	–	ns
VS	Operating range	–	2.5	–	5.5	V

[1] *The output voltage is in the unit gain circuitry and over the full input common-mode range.*

[2] *The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is VDD.*

[3] *The response time specified is a 100 mV input step with 30 mV overdrive.*

9.3 EM78F642/542N

■ Ta=25°C, VDD=5.0V±5%, VSS=0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	Crystal: VDD to 3V	Two cycles with two clocks	DC	–	8	MHz
	Crystal: VDD to 4.5V		DC	–	16	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 300 pF	F-30%	370	F+30%	kHz
	IRC: VDD to 5 V	4 MHz, 16 MHz, 8 MHz, 455kHz	F-2.5%	F	F+2.5%	Hz
IIL	Input Leakage Current for Input pins	VIN = VDD, VSS	–	–	±1	μA
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	3.5	–	V
IERC1	Sink current	VI from low to high, VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	1.5	–	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	0.7VDD	–	VDD+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	-0.3V	–	0.3VDD	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.7VDD	–	VDD+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	-0.3V	–	0.3VDD	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	0.7VDD	–	VDD+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT	-0.3V	–	0.3VDD	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	–	3.0	–	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	–	1.8	–	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = VDD-0.5V (IOH =3.7mA)	-3.0	-4.2	–	mA
IOL1	Output Low Voltage (Ports 5, 7, 8)	VOL = GND+0.5V	14	18	–	mA
IOL2	Output Low Voltage (Port 6)	VOL = GND+0.5V	18	23	–	mA
IPH	Pull-high current	Pull-high active, Input pin at VSS	–	-70	-80	μA
IPL	Pull-low current	Pull-low active, Input pin at Vdd	–	20	30	μA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1.0	1.5	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	8	10	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT disabled	–	37	40	μA

(Continuation)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT enabled	–	39	43	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=455kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT enabled (VDD = 3V)	–	110	120	μA
ICC4	Operating supply current at two clocks	/RESET = 'High', Fosc=455kHz (IRC type, CLKS1:0="01"), Output pin floating, WDT enabled (VDD = 3V)	–	100	110	μA
ICC5	Operating supply current at two clocks	/RESET = 'High', Fosc = 4 MHz (Crystal type, CLKS1:0 = "01"), Output pin floating, WDT enabled	–	1.1	1.5	mA
ICC6	Operating supply current at two clocks	/RESET = 'High', Fosc = 10 MHz (Crystal type, CLKS1:0 = "01"), Output pin floating, WDT enabled	–	2.8	3	mA

NOTE

- *The parameters shown above are theoretical values only and have not been tested or verified.*
- *Data under "Min", "Typ", & "Max" columns are based on theoretical results at 25℃. These data are for design guidance only and have not been tested or verified.*

9.3.1 Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	–	–	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	100K	–	cycles

9.3.2 Data EEPROM Electrical Characteristics (for EM78F642N only)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.5~ 5.5V Temperature = -40°C ~ 85°C	–	4.5	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	1000K	–	cycles

9.3.3 Comparator Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage[1]	RL = 5.1K	–	–	5	mV
Vcm	Input common-mode voltages range[2]	–	GND	–	VDD	V
ICO	Supply current of Comparator	–	–	200	–	uA
TRS	Response time[3]	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load), Overdrive = 30mV	–	0.7	–	us
TLRS	Large signal response time	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load)	–	260	–	ns
VS	Operating range	–	2.5	–	5.5	V

[1] *The output voltage is in the unit gain circuitry and over the full input common-mode range.*

[2] *The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is VDD.*

[3] *The response time specified is a 100 mV input step with 30 mV overdrive.*

9.4 EM78F641/541N

■ Ta=25°C, VDD=5.0V±5%, VSS=0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	Crystal: VDD to 3V	Two cycle with two clocks	DC	–	8	MHz
	Crystal: VDD to 5V		DC	–	16	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 300 pF	F-30%	370	F+30%	kHz
	IRC: VDD to 5 V	4 MHz, 16 MHz, 8 MHz	F-2.5%	F	F+2.5%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	μA
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	3.5	–	V
IERC1	Sink current	VI from low to high, VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	1.5	–	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 8	0.7VDD	–	VDD+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 8	-0.3V	–	0.3 VDD	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.7VDD	–	VDD+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	-0.3V	–	0.3 VDD	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	INT	0.7VDD	–	VDD + 0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	INT	-0.3V	–	0.3 VDD	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	–	3.0	–	V

(Continuation)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VILX1	Clock Input Low Voltage	OSCI in crystal mode	–	1.8	–	V
IOH1	Output High Voltage (Ports 5, 6, 8)	VOH = VDD-0.5V (IOH =3.7mA)	-3.0	-4.2	–	mA
IOL1	Output Low Voltage (Ports 5, 8)	VOL = GND+0.5V	9	11	–	mA
IOL2	Output Low Voltage (Port 6)	VOL = GND+0.5V	15	18	–	mA
IPH	Pull-high current	Pull-high active, Input pin at VSS	–	-70	-80	μA
IPL	Pull-low current	Pull-low active, Input pin at Vdd	–	20	30	μA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1.0	1.5	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	8	10	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT disabled, HLP=1	–	37	40	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT enabled, HLP=1	–	39	43	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=455kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT enabled, HLP=1 (VDD = 3V)	–	110	120	μA
ICC4	Operating supply current at two clocks	/RESET = 'High', Fosc = 4 MHz (Crystal type, CLKS1:0 = "01"), Output pin floating, WDT enabled	–	1.1	1.5	mA
ICC5	Operating supply current at two clocks	/RESET = 'High', Fosc = 10 MHz (Crystal type, CLKS1:0 = "01"), Output pin floating, WDT enabled	–	2.7	3	mA

NOTE

- *The parameters shown above are theoretical values only and have not been tested or verified.*
- *Data under "Min", "Typ", & "Max" columns are based on theoretical results at 25℃. These data are for design guidance only and have not been tested or verified.*

9.4.1 Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	–	–	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	100K	–	cycles

9.4.2 Data EEPROM Electrical Characteristics (for EM78F641N only)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.5~ 5.5V Temperature = -40°C ~ 85°C	–	4.5	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	1000K	–	cycles

9.4.3 Comparator Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage[1]	RL = 5.1K	–	–	5	mV
Vcm	Input common-mode voltages range[2]	–	GND	–	VDD	V
ICO	Supply current of Comparator	–	–	200	–	uA
TRS	Response time[3]	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load), Overdrive = 30mV	–	0.7	–	us
TLRS	Large signal response time	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load)	–	260	–	ns
VS	Operating range	–	2.5	–	5.5	V

[1] *The output voltage is in the unit gain circuitry and over the full input common-mode range.*

[2] *The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is VDD.*

[3] *The response time specified is a 100 mV input step with 30 mV overdrive.*

10 AC Electrical Characteristics

NOTE

- *The parameters shown below are theoretical values only and have not been tested or verified.*
- *Data under "Min", "Typ", & "Max" columns are based on theoretical results at 25℃. These data are for design guidance only and have not been tested or verified.*

10.1 EM78F648/548N

■ -40 ≤ Ta ≤ 85°C, VDD=5V, VSS=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS1:0="01")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	100	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload = 20 pF	–	50	–	ns

* ***N:*** *Selected prescaler ratio*

10.2 EM78F644/642/641/544/542/541N

■ --40 ≤ Ta ≤ 85°C, VDD=5V, VSS=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS1:0="01")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	14	16	18	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	14	16	18	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload = 20 pF	–	50	–	ns

* ***N:*** *Selected prescaler ratio*

APPENDIX

A Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM78F648/548NQ44J/S	QFP	44	10mm x 10mm
EM78F648/548ND40J/S	DIP	40	600 mil
EM78F648/548NK28J/S	Skinny DIP	28	300 mil
EM78F648/548ND28J/S	DIP	28	600 mil
EM78F648/548NSO28J/S	SOP	28	300 mil
EM78F644/544NK28J/S	Skinny DIP	28	300 mil
EM78F644/544NSO28J/S	SOP	28	300 mil
EM78F644/544NK24J/S	Skinny DIP	24	300 mil
EM78F644/544NSO24J/S	SOP	24	300 mil
EM78F642/542ND20J/S	DIP	20	300 mil
EM78F642/542NSO20J/S	SOP	20	300 mil
EM78F642/542NSS20J/S	SSOP	20	209mil
EM78F642/542ND18J/S	DIP	18	300 mil
EM78F642/542NSO18J/S	SOP	18	300 mil
EM78F641/541NAD16J/S	DIP	16	300 mil
EM78F641/541NASO16AJ/S	SOP	16	150 mil
EM78F641/541NMS10J/S	MSOP	10	118 mil

A.1 Green Products Compliance

These MCUs are Green products which do not contain hazardous substances. They complied with the third edition of Sony SS-00259 standard.

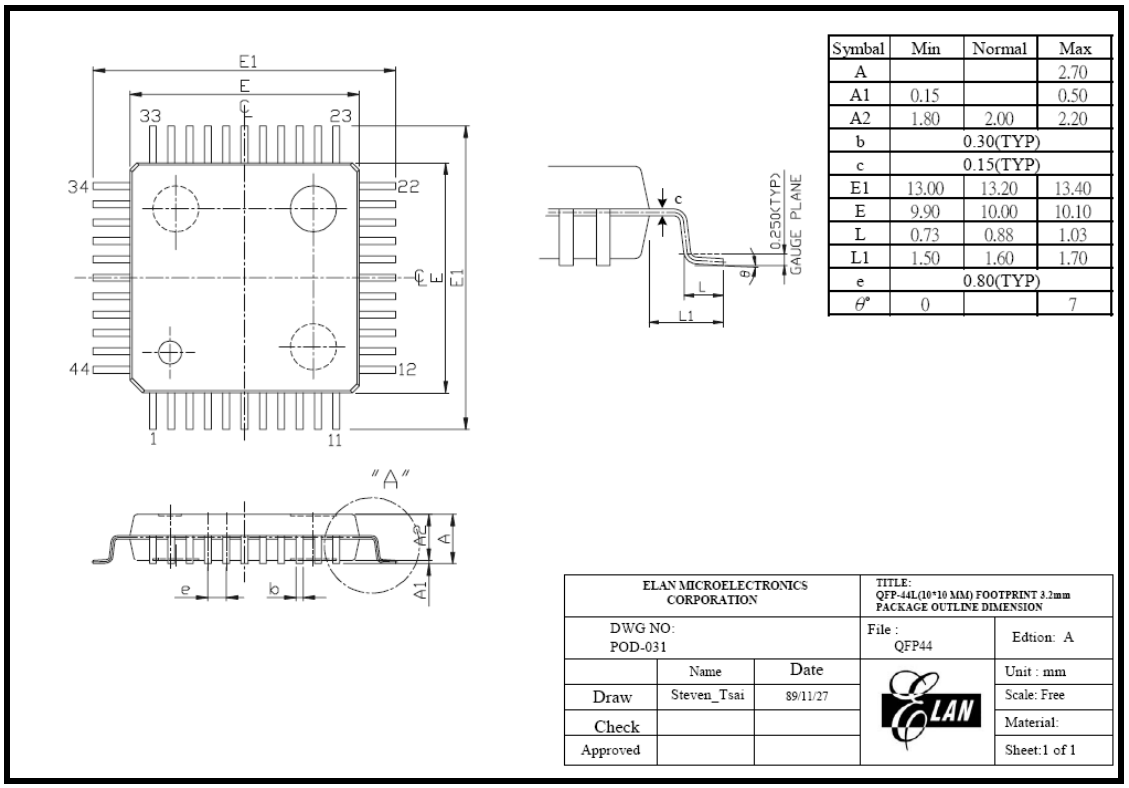
The Pb contents are less the 100ppm and complied with Sony specifications.

Part No.	EM78F64x/54xNxJ/xS
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Packaging Configuration

B.1 EM78F648/548N

B.1.1 44-Pin QFP Package

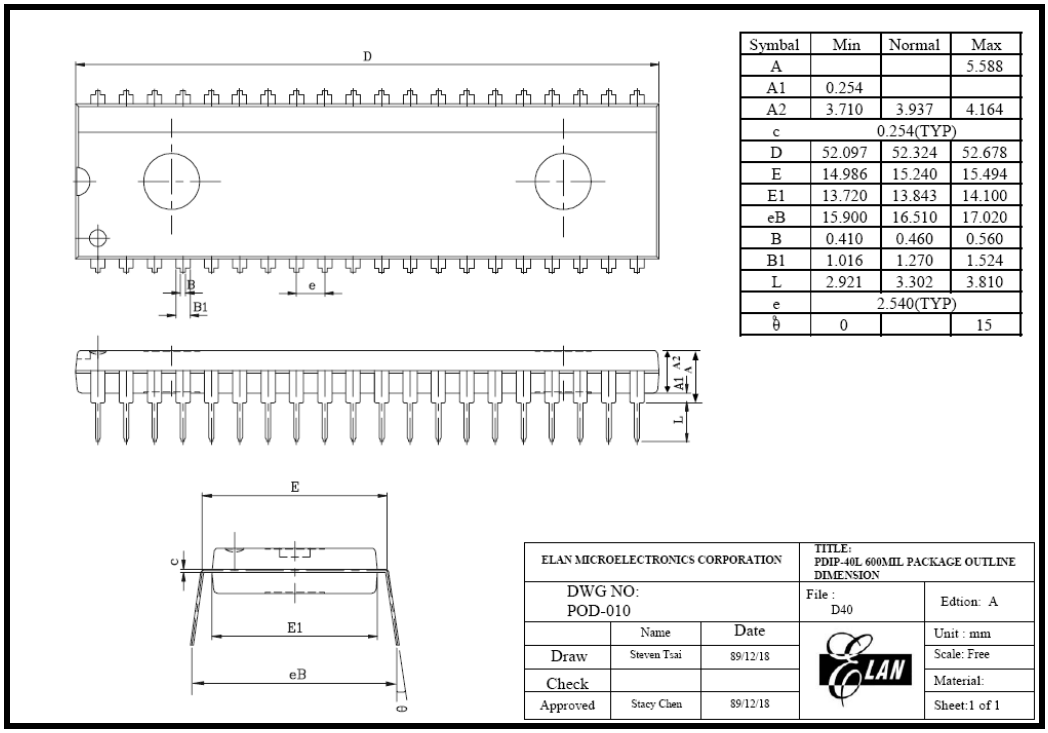


Symbal	Min	Normal	Max
A			2.70
A1	0.15		0.50
A2	1.80	2.00	2.20
b		0.30(TYP)	
c		0.15(TYP)	
E1	13.00	13.20	13.40
E	9.90	10.00	10.10
L	0.73	0.88	1.03
L1	1.50	1.60	1.70
e		0.80(TYP)	
θ°	0		7

ELAN MICROELECTRONICS CORPORATION			TITLE: QFP-44L(10*10 MM) FOOTPRINT 3.2mm PACKAGE OUTLINE DIMENSION	
DWG NO: POD-031			File : QFP44	Edtion: A
	Name	Date		Unit : mm
Draw	Steven_Tsai	89/11/27		Scale: Free
Check				Material:
Approved				Sheet:1 of 1

Figure B-1 EM78F648/548N 44-Pin QFP Package Type

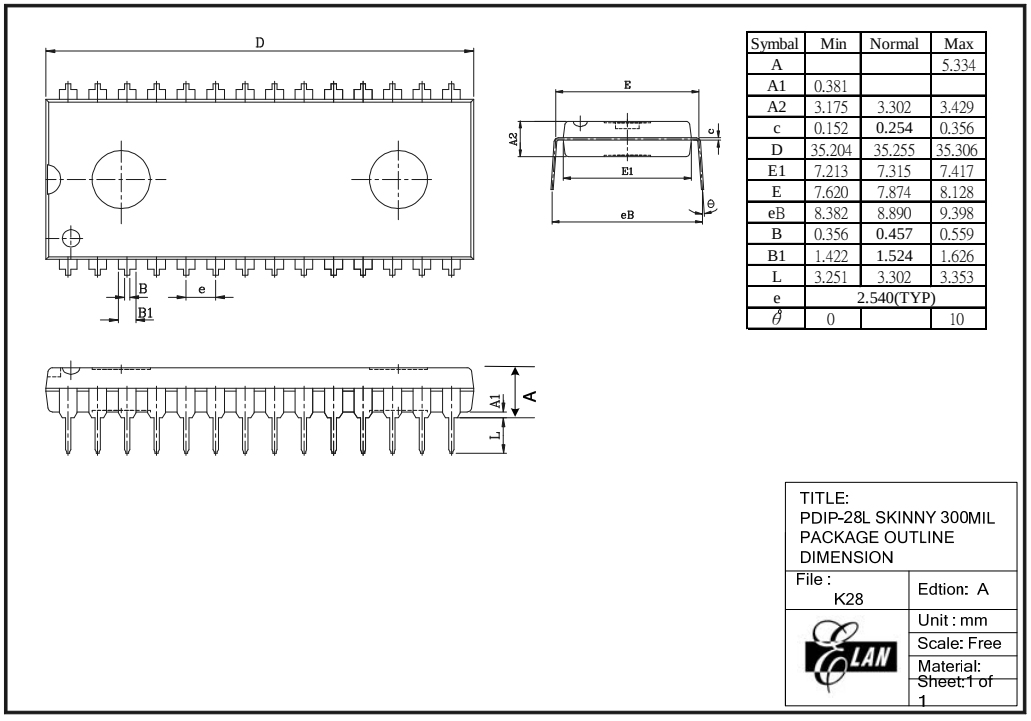
B.1.2 40-Pin DIP Package



Symbal	Min	Normal	Max
A			5.588
A1	0.254		
A2	3.710	3.937	4.164
c		0.254(TYP)	
D	52.097	52.324	52.678
E	14.986	15.240	15.494
E1	13.720	13.843	14.100
eB	15.900	16.510	17.020
B	0.410	0.460	0.560
B1	1.016	1.270	1.524
L	2.921	3.302	3.810
e		2.540(TYP)	
θ	0		15

Figure B-2 EM78F648/548N 40-Pin DIP Package Type

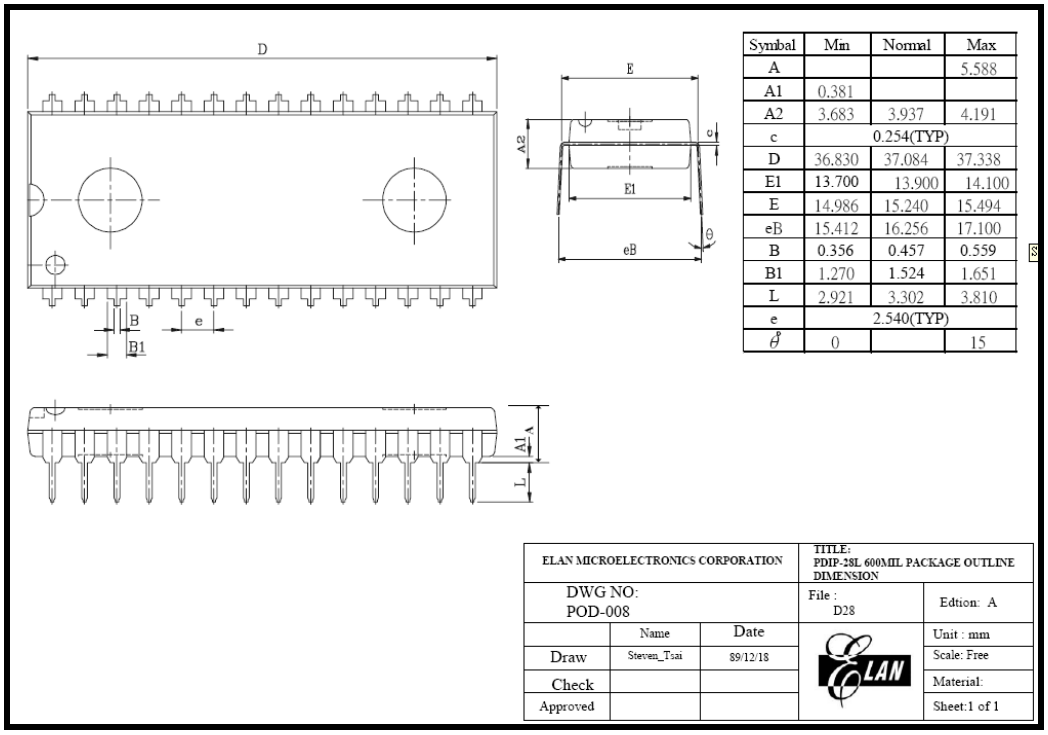
B.1.3 28-Pin Skinny DIP Package



Symbal	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.152	0.254	0.356
D	35.204	35.255	35.306
E1	7.213	7.315	7.417
E	7.620	7.874	8.128
eB	8.382	8.890	9.398
B	0.356	0.457	0.559
B1	1.422	1.524	1.626
L	3.251	3.302	3.353
e		2.540(TYP)	
θ	0		10

Figure B-3 EM78F648/548N 28-Pin Skinny DIP Package Type

B.1.4 28-Pin DIP Package

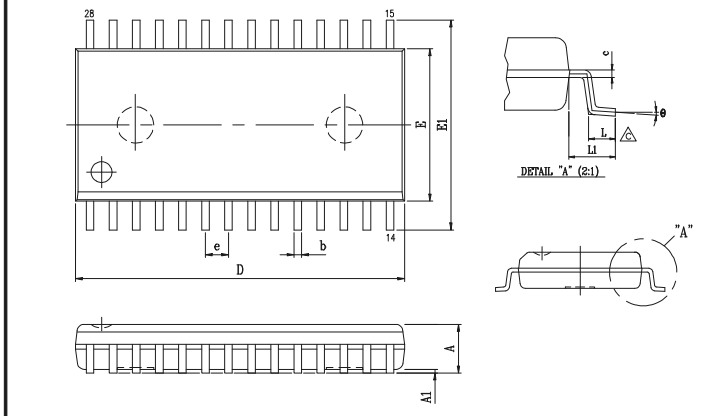


Symbal	Min	Normal	Max
A			5.588
A1	0.381		
A2	3.683	3.937	4.191
c		0.254(TYP)	
D	36.830	37.084	37.338
E1	13.700	13.900	14.100
E	14.986	15.240	15.494
eB	15.412	16.256	17.100
B	0.356	0.457	0.559
B1	1.270	1.524	1.651
L	2.921	3.302	3.810
e		2.540(TYP)	
θ°	0		15

ELAN MICROELECTRONICS CORPORATION			TITLE: PDIP-28L 600MIL PACKAGE OUTLINE DIMENSION
DWG NO: POD-008			File : D28 / Edtion: A
	Name	Date	Unit : mm
Draw	Steven_Tsai	89/12/18	Scale: Free
Check			Material:
Approved			Sheet:1 of 1

Figure B-4 EM78F648/548N 28-Pin DIP Package Type

B.1.5 28-Pin SOP Package



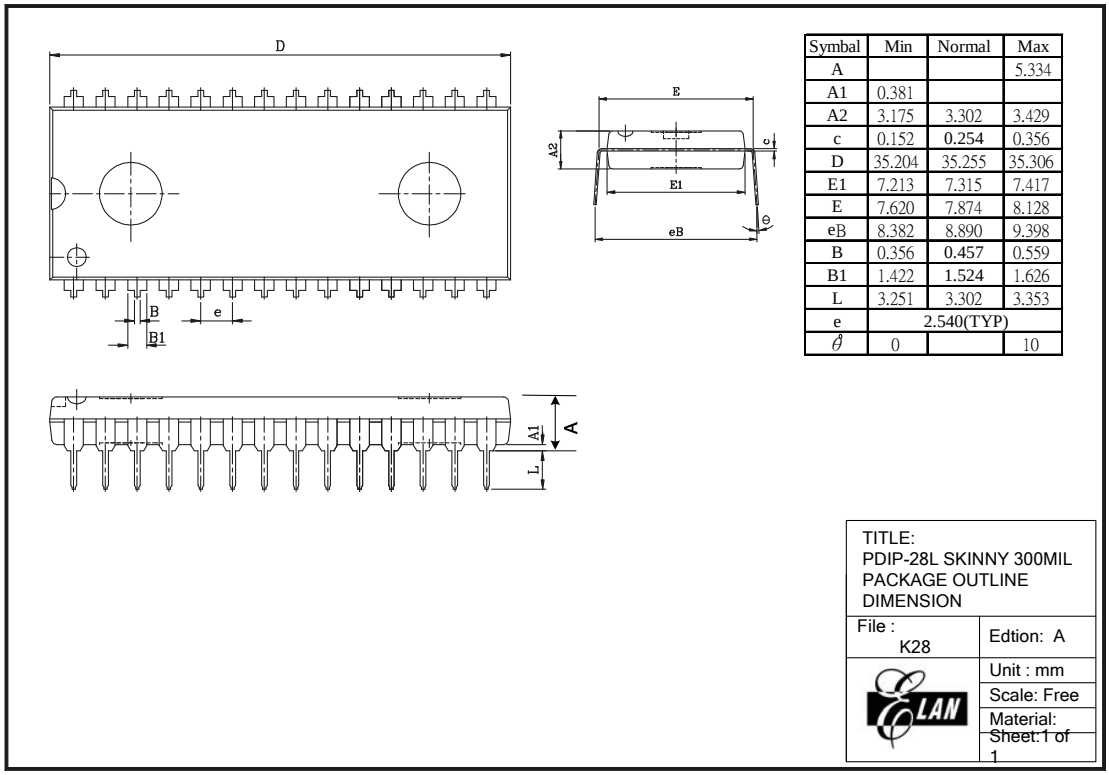
Symbal	Min	Normal	Max
A	2.370	2.500	2.630
A1	0.102		0.300
b	0.350	0.406	0.500
c		0.254(TYP)	
E	7.410	7.500	7.590
E1	10.000	10.325	10.650
D	17.700	17.900	18.100
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e		1.27(TYP)	
θ°	0		8

TITLE: SOP-28L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO28	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-5 EM78F648/548N 28-Pin SOP Package Type

B.2 EM78F644/544N

B.2.1 28-Pin Skinny DIP Package

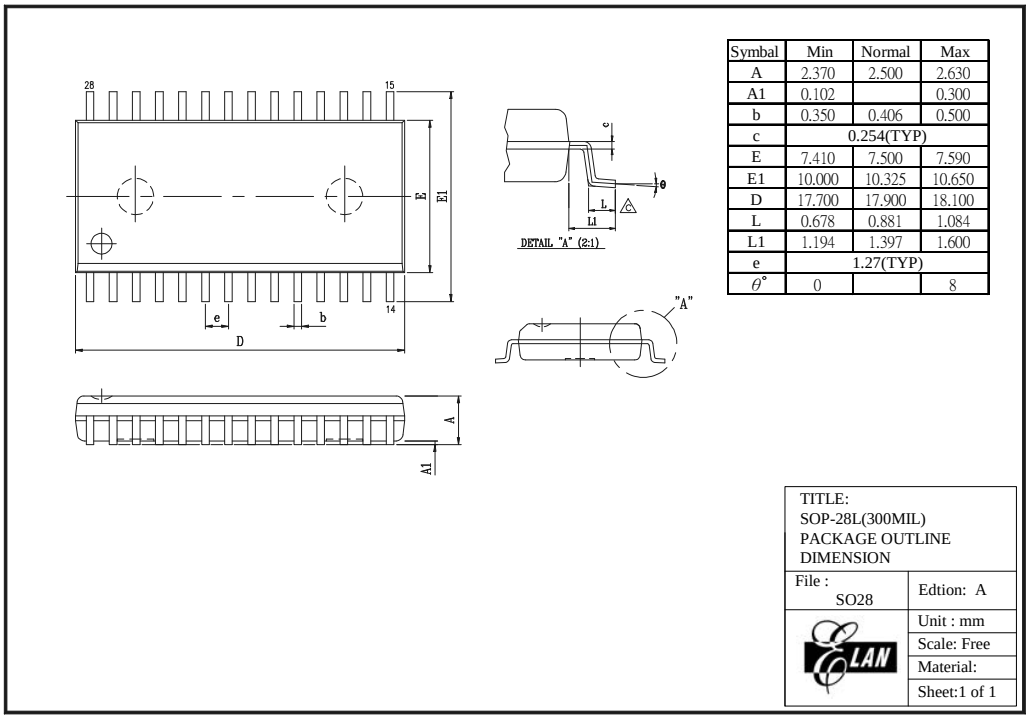


Symbal	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.152	0.254	0.356
D	35.204	35.255	35.306
E1	7.213	7.315	7.417
E	7.620	7.874	8.128
eB	8.382	8.890	9.398
B	0.356	0.457	0.559
B1	1.422	1.524	1.626
L	3.251	3.302	3.353
e	2.540(TYP)		
θ	0		10

TITLE: PDIP-28L SKINNY 300MIL PACKAGE OUTLINE DIMENSION	
File : K28	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-6 EM78F644/544N 28-pin Skinny DIP Package Type

B.2.2 28-Pin SOP Package

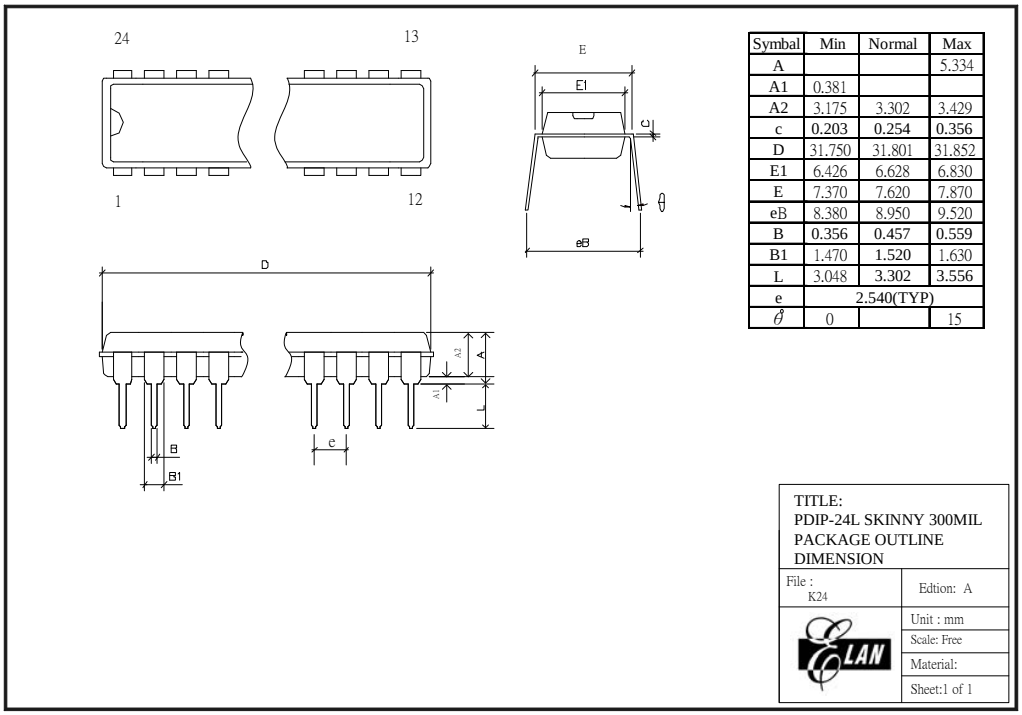


Symbal	Min	Normal	Max
A	2.370	2.500	2.630
A1	0.102		0.300
b	0.350	0.406	0.500
c		0.254(TYP)	
E	7.410	7.500	7.590
E1	10.000	10.325	10.650
D	17.700	17.900	18.100
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e		1.27(TYP)	
θ°	0		8

TITLE: SOP-28L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO28	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-7 EM78F644/544N 28-Pin SOP Package Type

B.2.3 24-Pin Skinny DIP Package

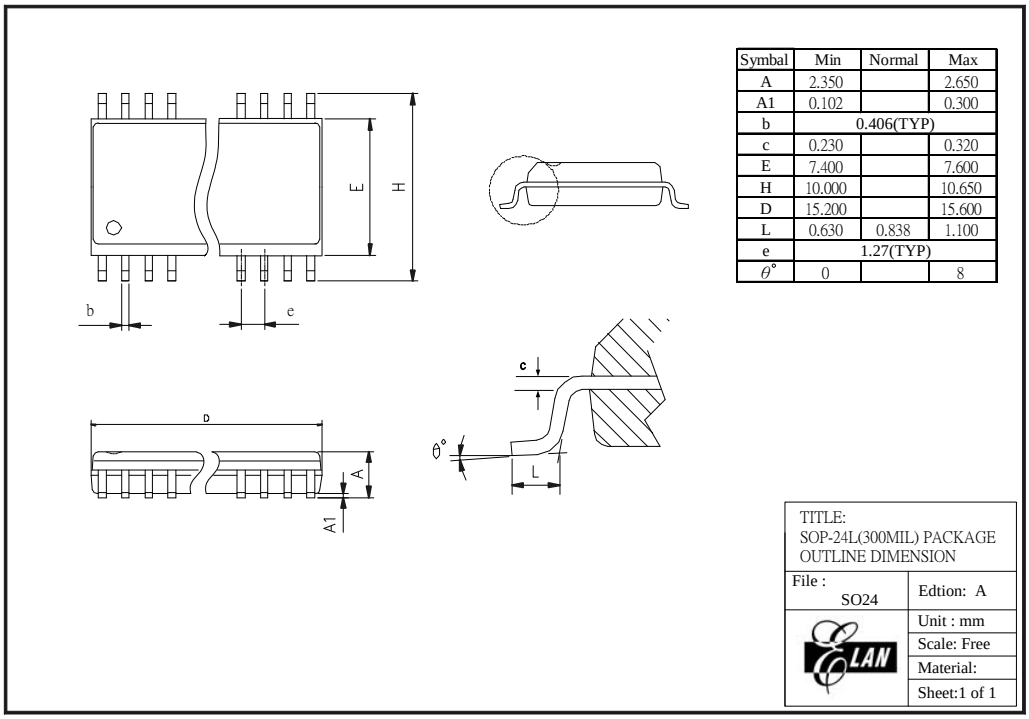


Symbol	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	31.750	31.801	31.852
E1	6.426	6.628	6.830
E	7.370	7.620	7.870
eB	8.380	8.950	9.520
B	0.356	0.457	0.559
B1	1.470	1.520	1.630
L	3.048	3.302	3.556
e		2.540(TYP)	
θ°	0		15

TITLE: PDIP-24L SKINNY 300MIL PACKAGE OUTLINE DIMENSION	
File : K24	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-8 EM78F644/544N 24-Pin Skinny DIP Package Type

B.2.4 24-Pin SOP Package



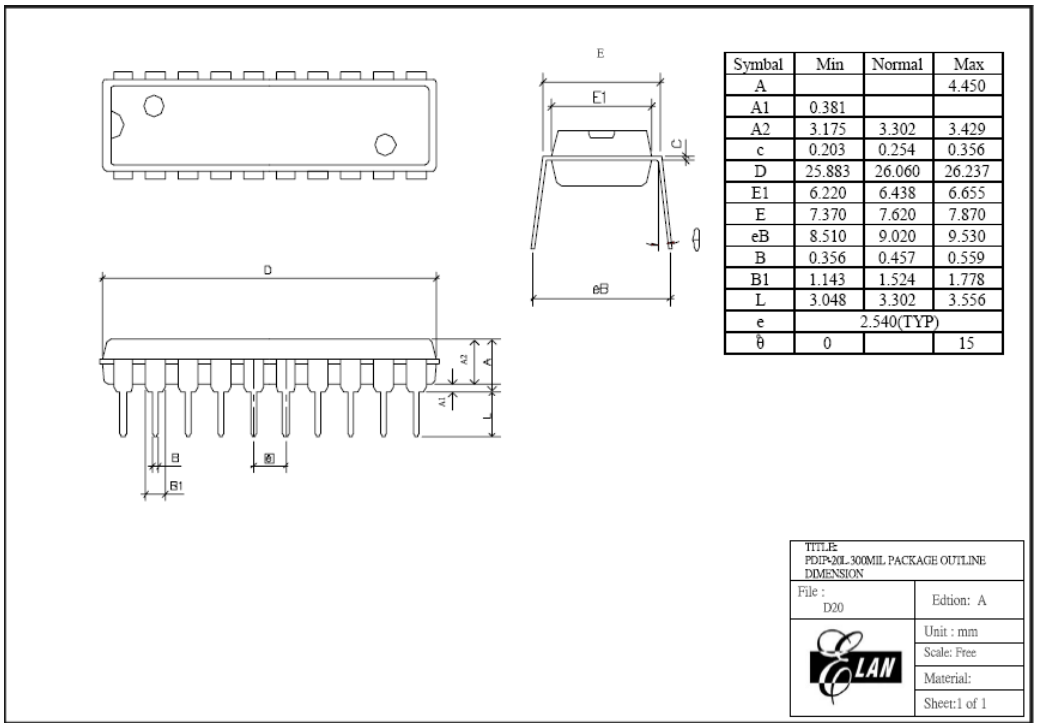
Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	15.200		15.600
L	0.630	0.838	1.100
e		1.27(TYP)	
θ°	0		8

TITLE: SOP-24L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO24	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-9 EM78F644/544N 24-Pin SOP Package Type

B.3 EM78F642/542N

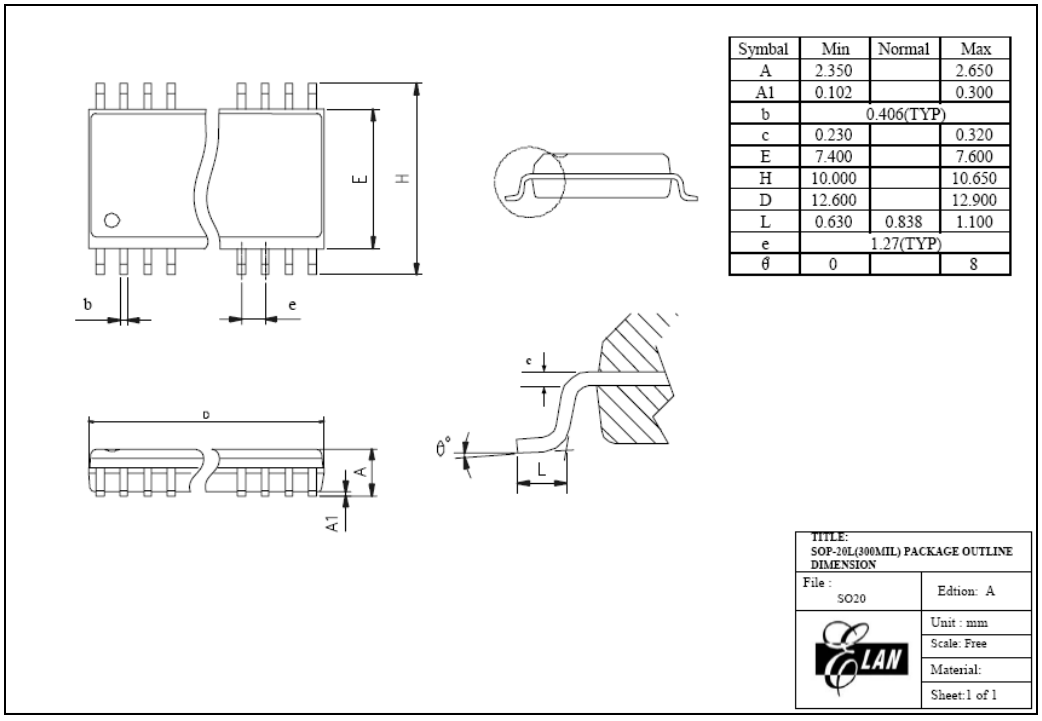
B.3.1 20-Pin DIP Package



Symbal	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	25.883	26.060	26.237
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

Figure B-10 EM78F642/542N 20-Pin DIP Package Type

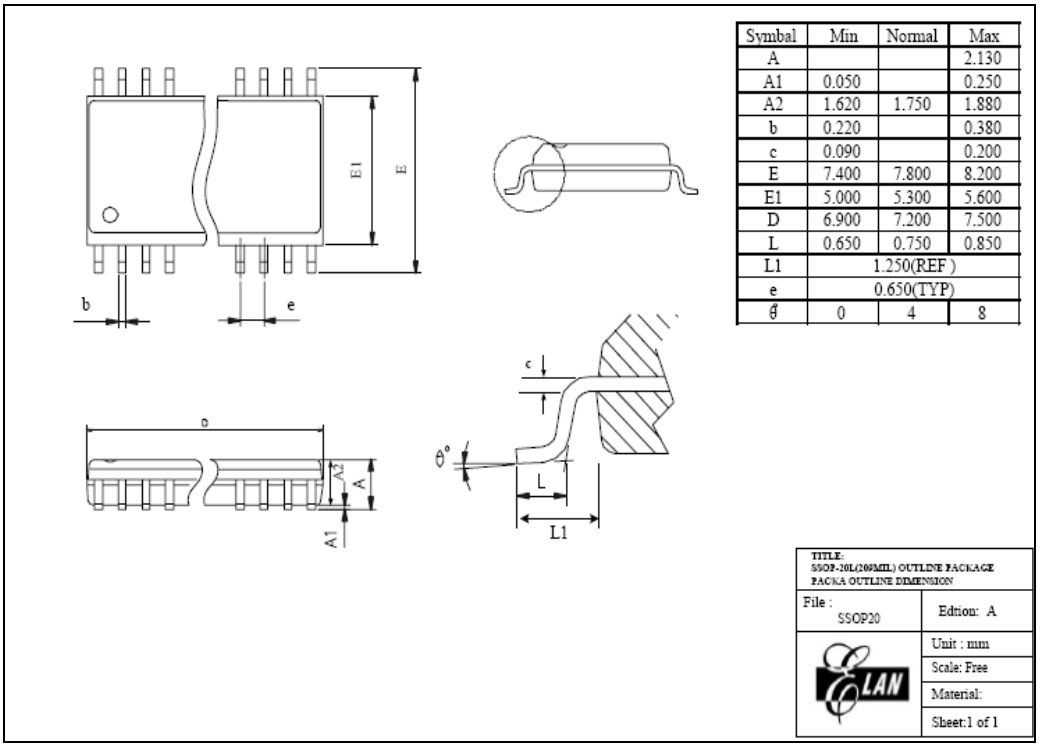
B.3.2 20-Pin SOP Package



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e		1.27(TYP)	
θ	0		8

Figure B-11 EM78F642/542N 20-Pin SOP Package Type

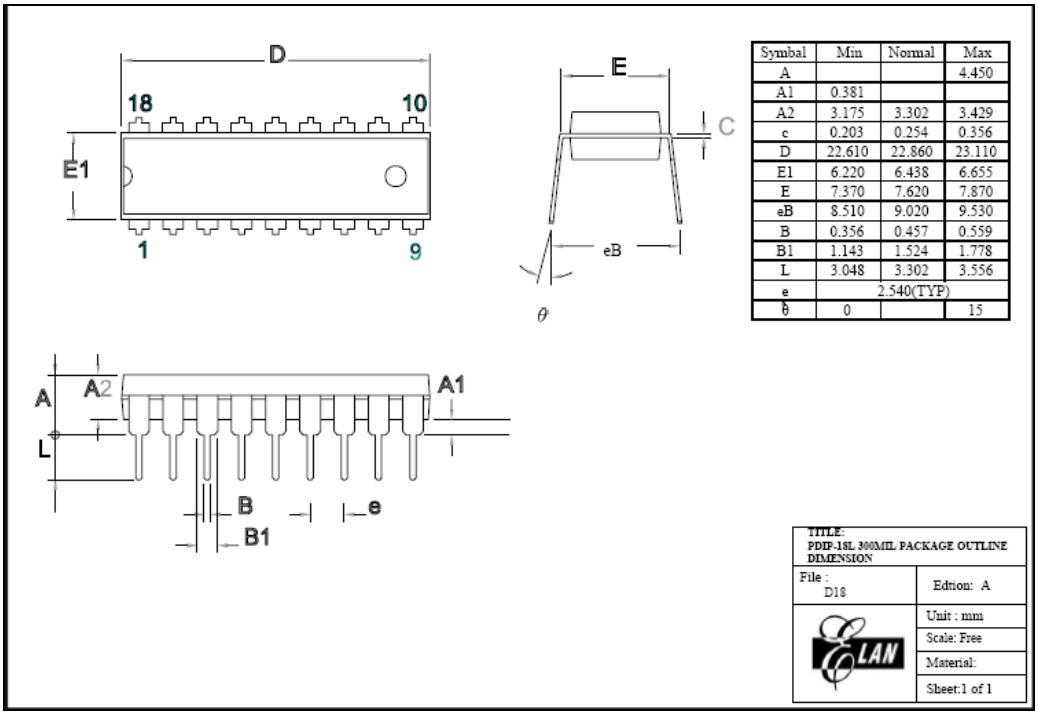
B.3.3 20-Pin SSOP Package



Symbal	Min	Normal	Max
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	6.900	7.200	7.500
L	0.650	0.750	0.850
L1		1.250(REF)	
e		0.650(TYP)	
θ	0	4	8

Figure B-12 EM78F642/542N 20-Pin SSOP Package Type

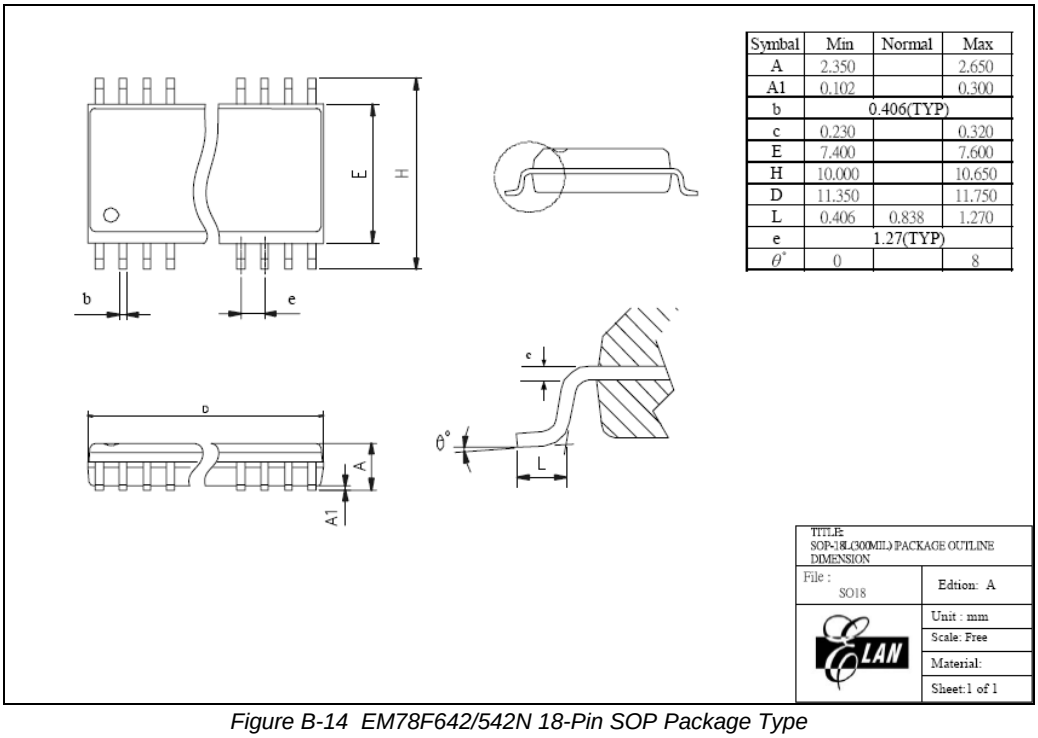
B.3.4 18-Pin DIP Package



Symbal	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

Figure B-13 EM78F642/542N 18-Pin DIP Package Type

B.3.5 18-Pin SOP Package

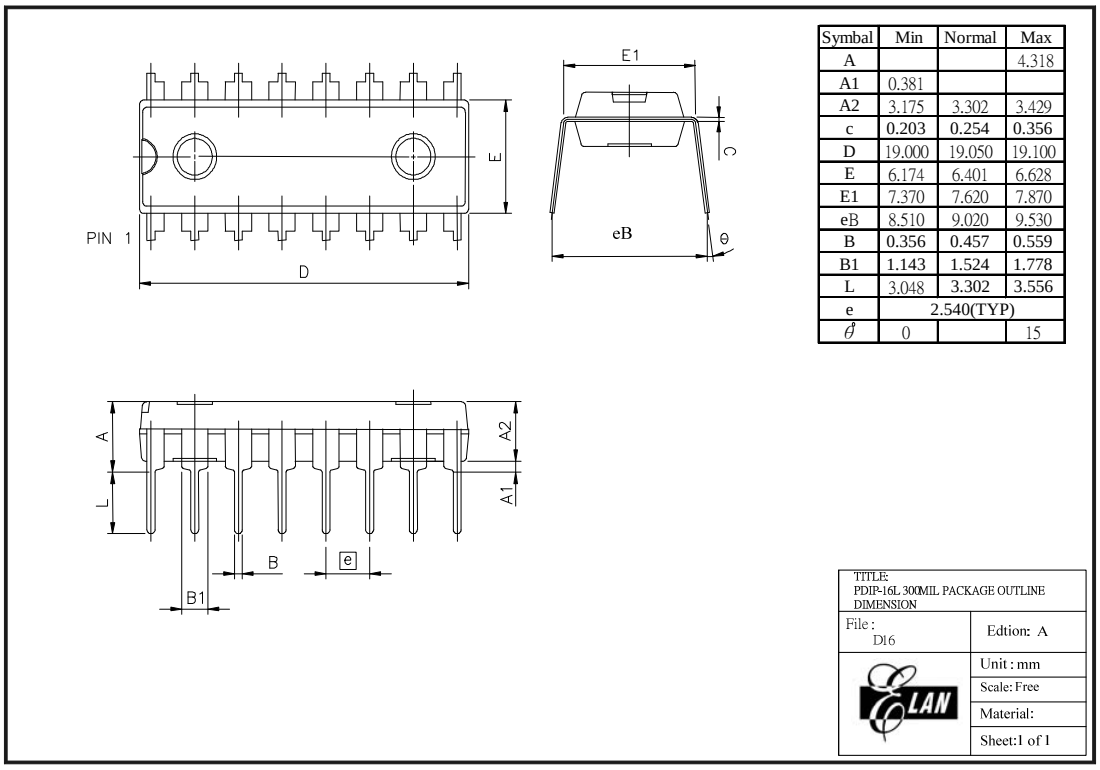


Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e	1.27(TYP)		
θ°	0		8

Figure B-14 EM78F642/542N 18-Pin SOP Package Type

B.4 EM78F641/541N

B.4.1 16-Pin DIP Package

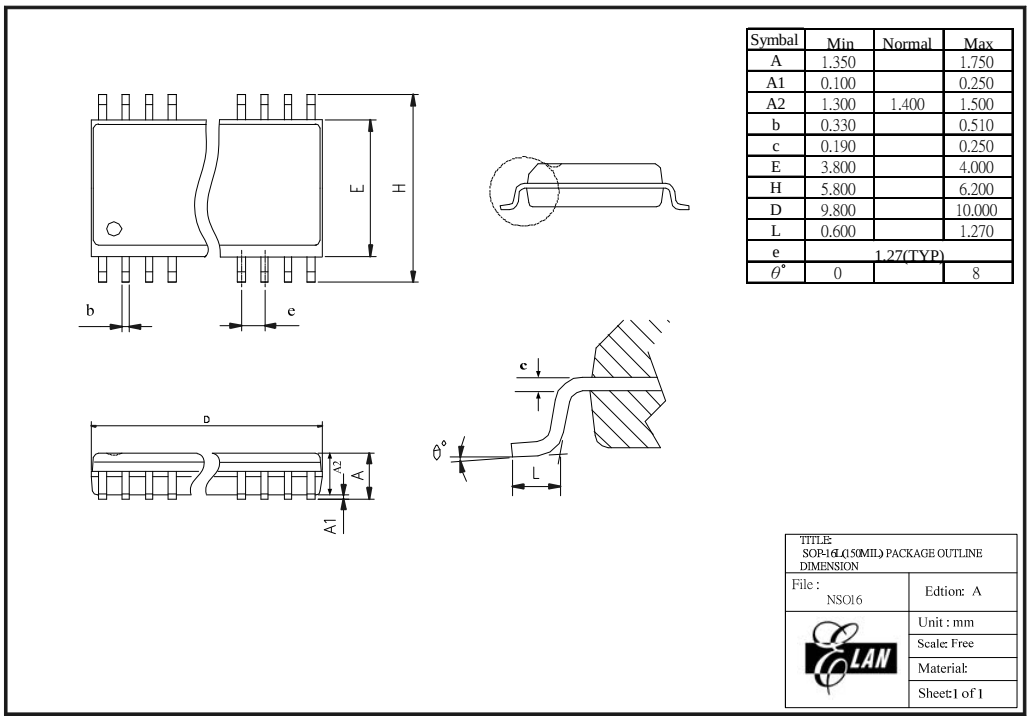


Symbal	Min	Normal	Max
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	19.000	19.050	19.100
E	6.174	6.401	6.628
E1	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ°	0		15

TITLE: PDIP-16L 300MIL PACKAGE OUTLINE DIMENSION	
File : D16	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-15 EM78F641/541N 16-Pin DIP Package Type

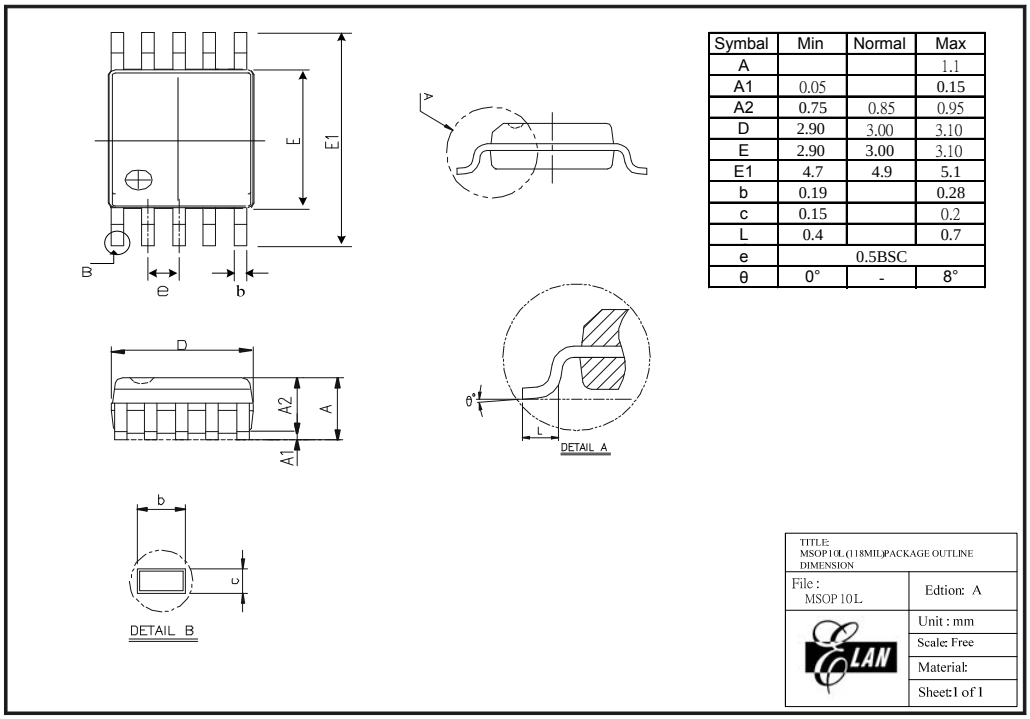
B.4.2 16-Pin SOP Package



Symbal	Min	Normal	Max
A	1.350		1.750
A1	0.100		0.250
A2	1.300	1.400	1.500
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	9.800		10.000
L	0.600		1.270
e	1.27(TYP)		
θ°	0		8

Figure B-16 EM78F641/541N 16-Pin SOP Package Type

B.4.3 10-Pin MSOP Package



Symbal	Min	Normal	Max
A			1.1
A1	0.05		0.15
A2	0.75	0.85	0.95
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.7	4.9	5.1
b	0.19		0.28
c	0.15		0.2
L	0.4		0.7
e	0.5BSC		
θ	0°	-	8°

Figure B-17 EM78F641/541N 10-Pin MSOP Package Type

C Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%，TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 ----225 ± 5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240 ± 5°C)	
Temperature cycle test	-65°C (15 min)~150°C (15 min), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%，TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥ | ± 3KV |	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS(-) mode
ESD (MM)	TA=25°C, ≥ | ± 300V |	

C.1 Address Trap Detect

The MCU is embedded with an “Address Trap Detect” feature. It is one of fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.