義隆電子股份有限公司

ELAN MICROELECTRONICS CORP.

EM78P811

8-BIT MICRO-CONTROLLER

Version 1.0

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I.General Description

The EM78P811 is an 8-bit CID (Call Identification) RISC type microprocessor with low power , high speed CMOS technology . There are 16Kx13 bits Electrical One Time Programmable Read Only Memory (OTP-ROM) within it. It provides Security bits and some One time programmable Option bits to protect the OTP memory code from any external access as well as to meet user's options.

The EM78P811 is Integrated onto a single chip are on_chip watchdog (WDT) , RAM , ROM , programmable real time clock /counter , internal interrupt , power down mode , LCD driver , FSK decoder , DTMF generator and tri-state I/O . The EM78P811 provides a single chip solution to design a CID of calling message_display .

II.Feature

CPU

- Operating voltage range : **2.5V 5.5V**
- **16K×13 Electrical One Time Programmable Read Only Memory (OTP-ROM)**
- 2.8K×8 on chip RAM
- Up to 32 bi-directional tri-state I/O ports
- level stack for subroutine nesting
- 8-bit real time clock/counter (TCC)
- Two sets of 8 bit counters can be interrupt sources
- Selective signal sources and trigger edges , and with overflow interrupt
- Programmable free running on chip watchdog timer
- 99.9% single instruction cycle commands
- Three modes (internal clock 3.679MHz)
    1. Sleep mode : CPU and 3.679MHz clock turn off, 32.768KHz clock turn off
    2. Idle mode : CPU and 3.679MHz clock turn off, 32.768KHz clock turn on
    3. Green mode : 3.679MHz clock turn off, CPU and 32.768KHz clock turn on
    4. Normal mode : 3.679MHz clock turn on , CPU and 32.768KHz clock turn on
- Ring on voltage detector and low battery detector
- Input port wake up function
- 8 interrupt source , 4 external , 4 internal
- 100 pin QFP or chip
- Port key scan function
- Port interrupt , pull high and open drain functions
- Clock frequency 32.768KHz

CID

- Operation Volltage 3.5 5.5V for FSK
- Operation Volltage 2.5 5.5V for DTMF
- Bell 202 , V.23 FSK demodulator
- DTMF generator
- Ring detector on chip

LCD

- LCD operation voltage chosen by software
- Common driver pins : 16
- Segment driver pins : 60
- 1/4 bias
- 1/8,1/16 duty

III.Application

** This specification is subject to be changed without notice.*

1. adjunct units
2. answering machines
3. feature phones

IV.Pin Configuration

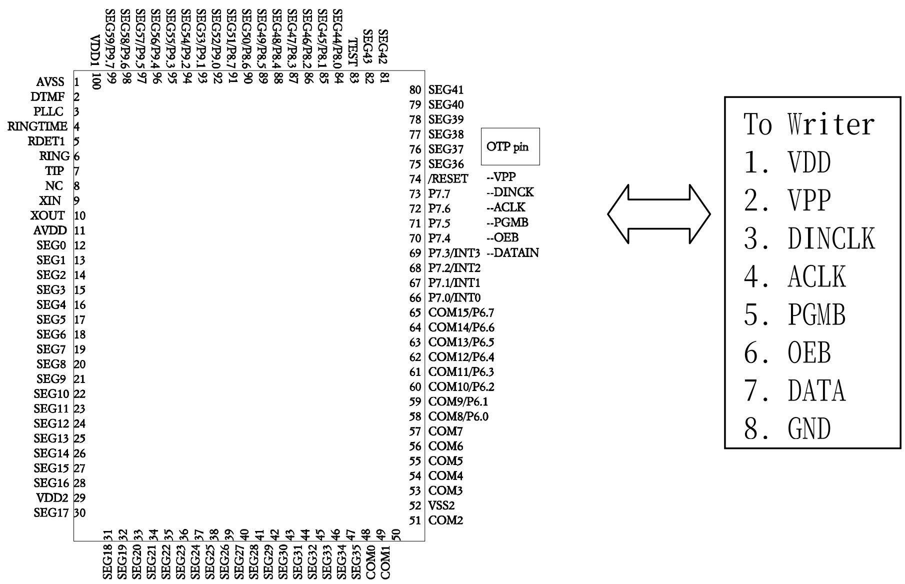


Fig1. Pin Assignment

V.Functional Block Diagram

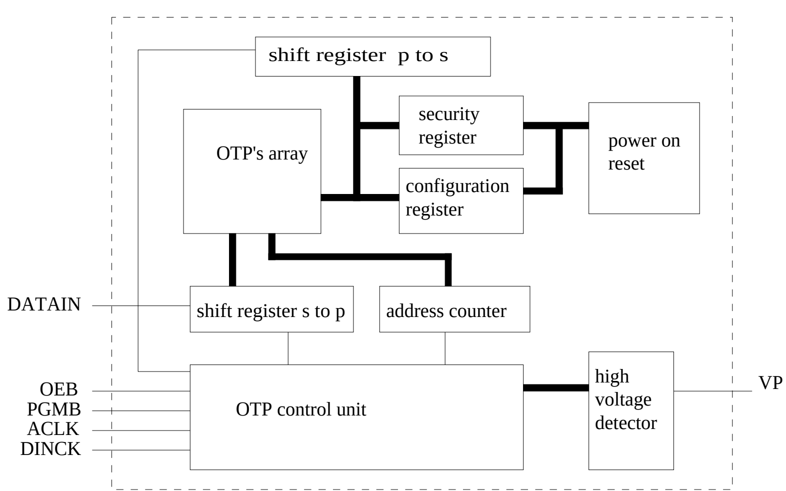


Fig2. Block diagram1

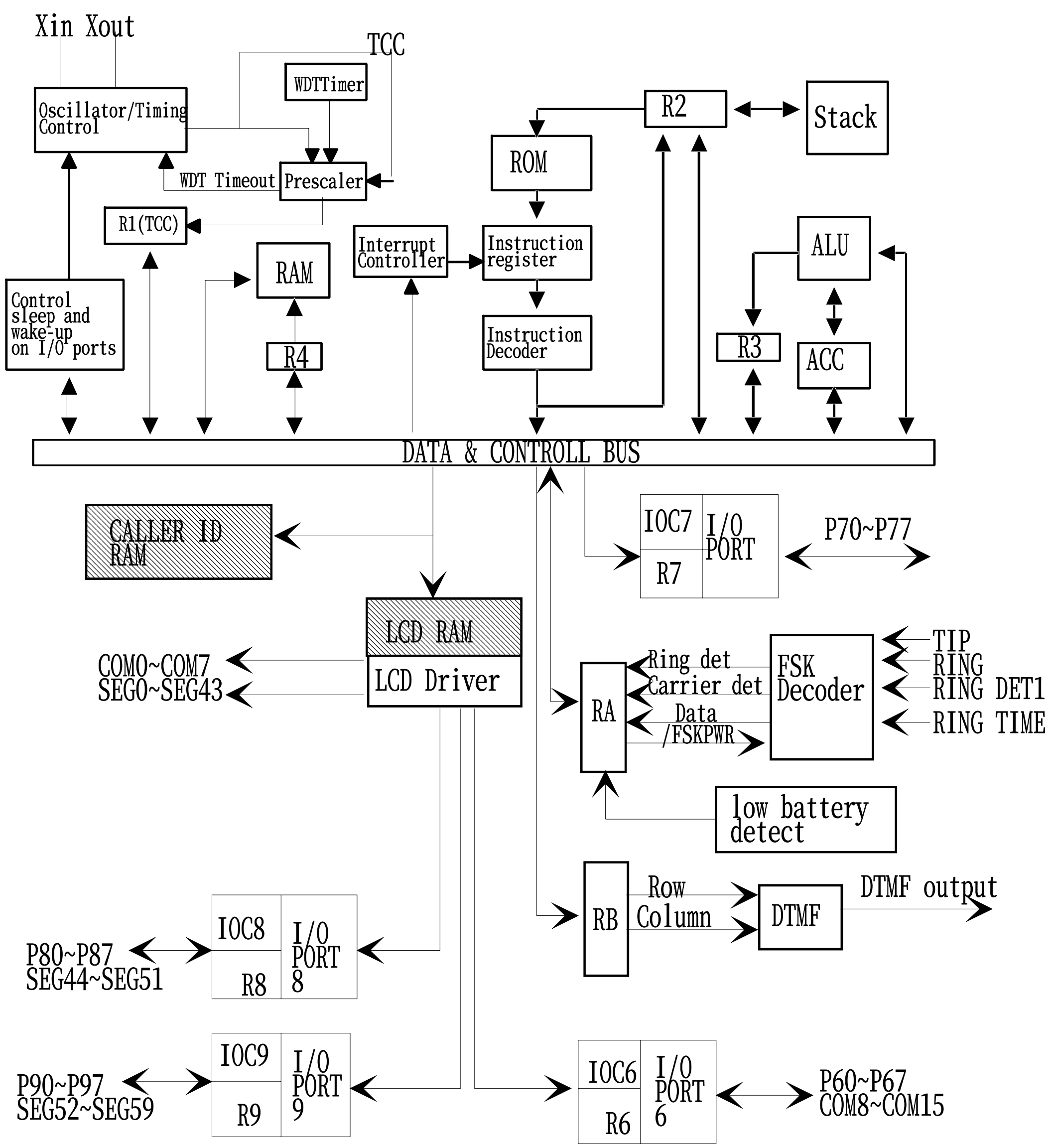


Fig3. Block diagram2

VI.Pin Descriptions

PIN	I/O	DESCRIPTION
VDD1,VDD2 AVDD	POWER	digital power analog power
VSS1,VSS2 AVSS	POWER	digital ground analog ground
Xtin	I	Input pin for 32.768 kHz oscillator
Xtout	O	Output pin for 32.768 kHz oscillator
COM0..COM7 COM8..COM15	O O (PORT6)	Common driver pins of LCD drivers
SEG0...SEG43 SEG44..SEG51 SEG52..SEG59	O O (PORT8) O (PORT9)	Segment driver pins of LCD drivers PORT9 AS FUNCTION KEY CAN WAKE UP WATCHDOG.
PLLC	I	**Phase loop lock capacitor, connect a capacitor 0.01u to 0.047u with AVSS**
TIP	I	Should be connected with TIP side of twisted pair lines
RING	I	Should be connected with TIP side of twisted pair lines
RDET1	I	Detect the energy on the twisted pair lines . These two pins coupled to the twisted pair lines through an attenuating network.
/RING TIME	I	Determine if the incoming ring is valid.An RC network may be connected to the pin.
INT0 INT1 INT2 INT3	PORT7(0) PORT7(1) PORT7(2) PORT7(3) PORT7(4:7)	PORT7(0)~PORT7(3) signal can be interrupt signals. IO port
P7.0 ~P7.7	PORT7	PORT 7 can be INPUT or OUTPUT port each bit. Internal Pull high function. Key scan function. Bit6,7 open drain function
P6.0 ~P6.7	PORT6	PORT 6 can be INPUT or OUTPUT port each bit. And shared with Common signal.
P8.0 ~P8.7	PORT8	PORT 8 can be INPUT or OUTPUT port each bit. And shared with Segment signal.
P9.0 ~P9.7	PORT9	PORT 9 can be INPUT or OUTPUT port each bit. And can be set to wake up watch dog timer. And shared with Segment signal.
TEST	I	Test pin into test mode , normal low
DTMF	O	DTMF tone output
RESET	I	
OTP pin		
DATAIN(P73)	I/O	Data pin
OEB(P74)	I	Output enable. Active low
PGMB(P75)	I	Program write enable. Active low
ACLK(P76)	I	CLK for OTP memory address increment . Increasing a address needs two clocks.
DINCK(P77)	I	Data latch clock. Latch a bit at rising edge

** This specification is subject to be changed without notice.*

VPP(RESET)	I	Programming voltage input. Vpp can be varied from 10.5V to 12.5V

VII.Functional Descriptions

VII.0 OTP ROM

1. OTP ROM
   * The OTP ROM's size is 16k x13 bits which can be serially writen and read.
2. Operation Mode

mode	DATAIN(p73)	OEB(p74)	PGMB(p75)
1.Regular mode	0	0	0
2.OTP row mode	1	0	0
3.Option mode	0	1	0
4.Bit line stress	1	1	0
5.Word line stress	0	0	1
6.Test mode	1	0	1

1.Regular mode: This mode is provided to program and verify OTP memory only.

2.OTP row mode: This mode is designed to provide capability programming and verifying of ROM data for the plastic OTP packages. One external row is added in addition to the regular ROM array. The user's data can be sequentially written into the ROM memory in OTP row by advancing the consecutive address to avoid the circuit change of program counter in microcontroller.

3.Option mode(Option register) :

The mode provides user a special mode for selecting option.

Bit12..Bit2	….	Bit1	Bit0
Code	….	/PT	MCLK

Bit0 :MCLK : main clock
  0: 1.84MHz
  1: 3.68MHz
Bit1 :/PT :Protect bit
  0:enable
  1:disable
Bit2..Bit12: code for user ID

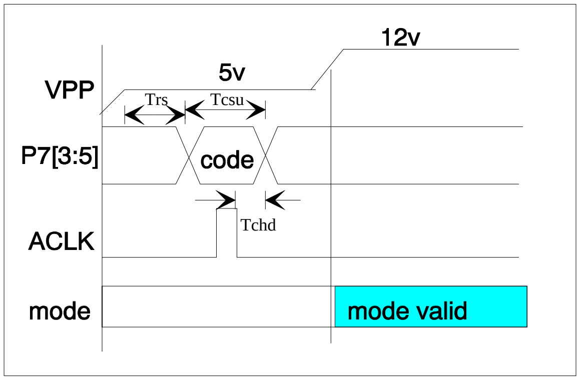
4.Bit line stress mode : This mode is provides to test the reliability of ROM cells. Bit line mode is to apply the programmed drain voltage on all bit lines but all word lines are ground.

5.Word line stress mode : This mode is provides to test the reliability of ROM cells. Word line mode is to apply the programming gate voltage on all word lines but all bit lines are ground.

6.Test mode : This mode is provided for verifying the speed of data from OTP memory.

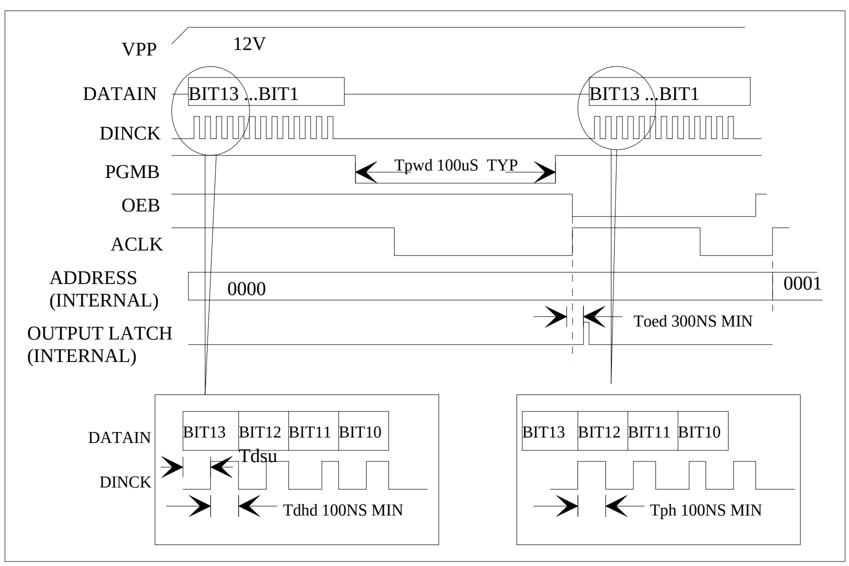
3. Mode selection

Mode is selected by voltage switch on VPP pin. The timing is as follow.



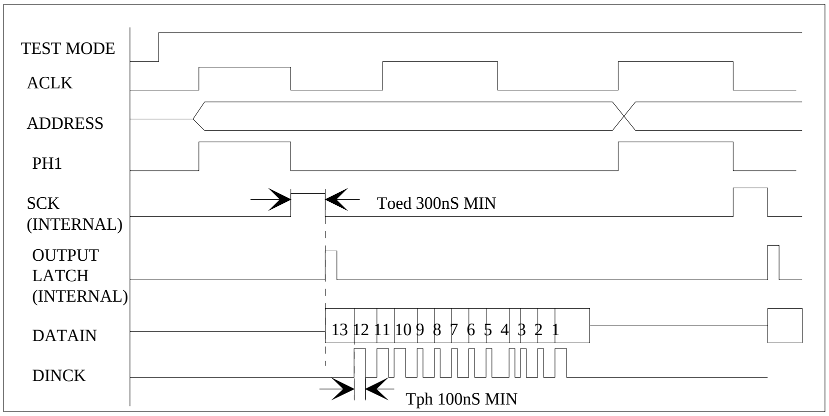
4. Regular mode: Program and Verify

After selecting the regular mode, writer can program instruction into OTP by following timing chart . The OTP 's address is increased by internal counter.



5. Test mode: Verify

After selecting the test mode, writer can verify instruction by following timing chart . The OTP 's address is increased by internal counter.


TEST MODE
ACLK
ADDRESS
PH1
SCK
(INTERNAL)
Toed 300nS MIN
OUTPUT
LATCH
(INTERNAL)
DATAIN
13 12 11 10 9 8 7 6 5 4 3 2 1
DINCK
Tph 100nS MIN

VII.1 Operational Registers

1. R0 (Indirect Addressing Register)

   * R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

2. R1 (TCC)

   * Increased by an external signal edge applied to TCC , or by the instruction cycle clock. Written and read by the program as any other register.

3. R2 (Program Counter)

   * The structure is depicted in Fig. 4.
   * Generates 16K × 13 on-chip ROM addresses to the relative programming instruction codes.
   * "JMP" instruction allows the direct loading of the low 10 program counter bits.
   * "CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.
   * "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.
   * "MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".
   * "ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".
   * "TBL" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change. The most significant bit (A10~A13) will be loaded with the content of bit PS0~PS3 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2,A", or "MOV R2,A" instruction.

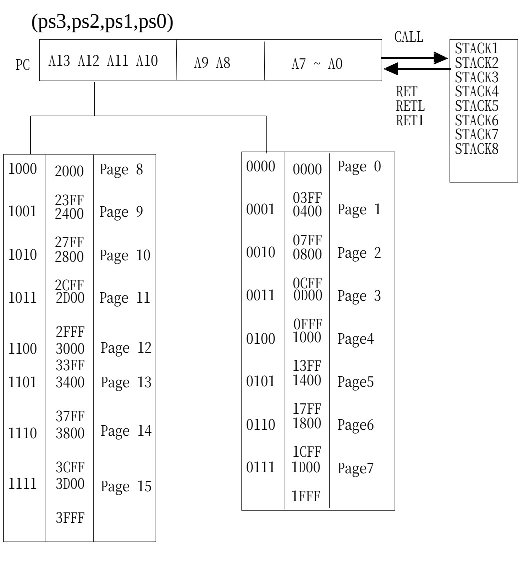


Fig.4 Program counter organization

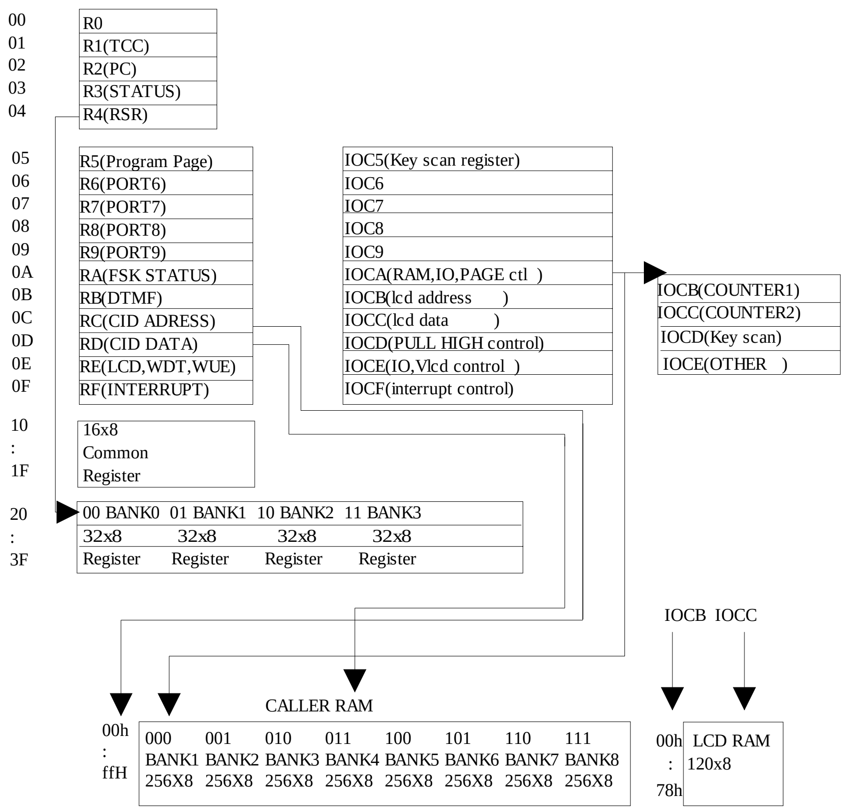


Fig.5 Data memory configuration

4. R3 (Status Register)

7	6	5	4	3	2	1	0
-	page	-	T	P	Z	DC	C

* Bit 0 (C) Carry flag
* Bit 1 (DC) Auxiliary carry flag
* Bit 2 (Z) Zero flag
* Bit 3 (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.
* Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

EVENT	T	P	REMARK
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode	0	1	
/RESET wake up from sleep	1	0	

power up	1	1	
Low pulse on /RESET	x	x	x .. don't care

* Bit 5 unused
*** Bit 6 PAGE : change IOCB ~ IOCE to another page , 0/1 => page0 / page1**
* Bit 7 unused

5. R4 (RAM Select Register)

* Bits 0 ~ 5 are used to select up to 64 registers in the indirect addressing mode.
* Bits 6 ~ 7 determine which bank is activated among the 4 banks.
* See the configuration of the data memory in Fig. 5.

6. R5 (Program Page Select Register)

7	6	5	4	3	2	1	0
-	-	-	-	PS3	PS2	PS1	PS0

* Bit 0 (PS0) ~ 3 (PS3) Page select bits

Page select bits

PS3	PS2	PS1	PS0	Program memory page (Address)
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
0	0	1	1	Page 3
0	1	0	0	Page 4
0	1	0	1	Page 5
0	1	1	0	Page 6
0	1	1	1	Page 7
1	0	0	0	Page 8
1	0	0	1	Page 9
1	0	1	0	Page 10
1	0	1	1	Page 11
1	1	0	0	Page 12
1	1	0	1	Page 13
1	1	1	0	Page 14
1	1	1	1	Page 15

*User can use PAGE instruction to change page. To maintain program page by user. Otherwise, user can use far jump (FJMP) or far call (FCALL) instructions to program user's code. And the program page is maintained by EMC's complier. It will change user's program by inserting instructions within program.

*Bit4~7 : unused

6. R6 ~ R9 (Port 6 ~ Port 9)

* Five 8-bit I/O registers.

7. RA (FSK Status Register)(bit 0,1,2,4 read only)

7	6	5	4	3	2	1	0
IDLE	/358E	/LPD	/LOW_BAT	/FSKPWR	DATA	/CD	/RD

* Bit0 (Read Only) (Ring detect signal)   0/1 : Ring Valid/Ring Invalid
* Bit1(Read Only)(Carrier detect signal)   0/1 : Carrier Valid/Carrier Invalid
* Bit2(Read Only)(FSK demodulator output signal)
  Fsk data transmitted in a baud rate 1200 Hz. Data from FSK demodulator when /CD is low.
* Bit3(read/write)(FSK block power up signal)
  1/0 : FSK demodulator block power up/FSK demodulator power down
* The relation between Bit0 to Bit3 is shown in Fig.6.

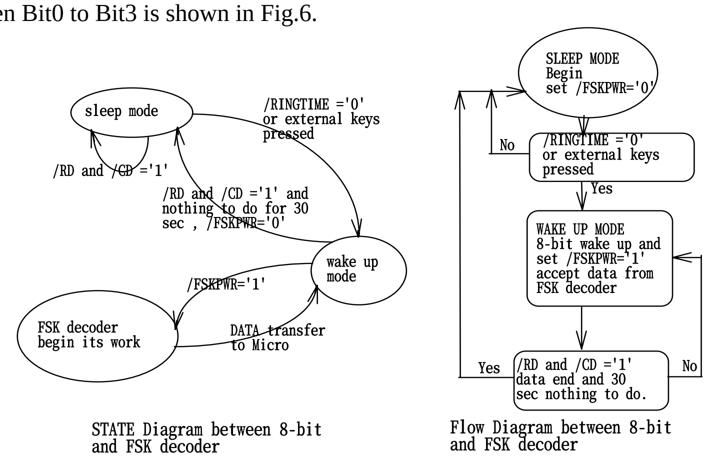


Fig6. The relation between Bit0 to Bit3.

* Bit4(Read Only)(Low battery signal)   0/1 = Battery voltage is low/Normal .
  If the battery voltage is under 4.2V then sends a '0' signal to RA register bit4 or a '1' signal to this Bit:.
* Bit5(read/Write)(Low battery detect enable)
0/1 = low battery detect DISABLE/ENABLE.
The relation between /LPD,/POVD and /LOW_BAT can see Fig7.

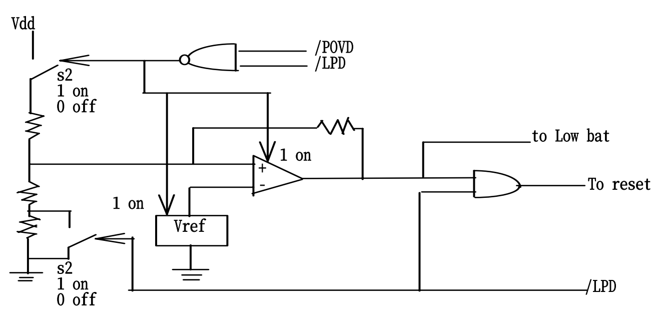


Fig7. The relation between /LPD,/POVD

* Bit6(read/write)(PLL enable signal)
  0/1=DISABLE/ENABLE
  The relation between 32.768K and 3.679M can see Fig8.

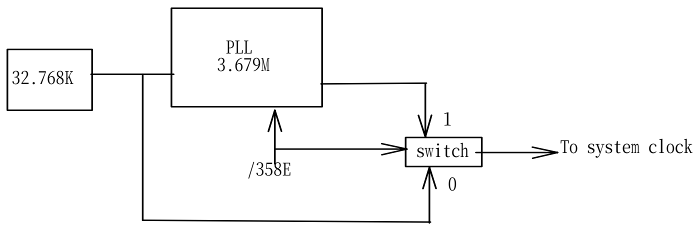


Fig8. The relation between 32.768K and 3.679K .

*** Bit7 IDLE: sleep mode selection bit**

0/1=sleep mode/IDLE mode. This bit will decide SLEP instruction which mode to go.

These two modes can be waken up by TCC clock or Watch Dog or PORT9 and run from "SLEP" next instruction.

	SLEEP mode	IDLE mode	GREEN mode	NORMAL mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(1,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out	X	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt
WDT time out	RESET	Wake-up + Next instruction	RESET	RESET
Port9 wake-up	RESET	Wake-up + Next instruction	RESET	RESET

8. RB(DTMF tone row and column register) (read/write)

7	6	5	4	3	2	1	0
c7	c6	c5	c4	r3	r2	r1	r0

* Bit 0 - Bit 3 are row-frequency tone.
* Bit 4 - Bit 7 are column-frequency tone.
* Initial RB is equal to high. Bit 7 ~ 0 are all "1" , turn off DTMF power .

bit 3~0	Row freq				
1110	699.2Hz	1	2	3	A
1101	771.6Hz	4	5	6	B
1011	854Hz	7	8	9	C
0111	940.1Hz	*	0	#	D
Column freq		1203Hz	1331.8Hz	1472Hz	1645.2Hz
bit 7~4		1110	1101	1011	0111

9. RC(CALLER ID address)(read/write)

7	6	5	4	3	2	1	0
CIDA7	CIDA6	CIDA5	CIDA4	CIDA3	CIDA2	CIDA1	CIDA0

* Bit 0 ~ Bit 7 select CALLER ID RAM address up to 256.

10. RD(CALLER ID RAM data)(read/write)

* Bit 0 ~ Bit 8 are CALLER ID RAM data transfer register.

User can see IOCA register how to select CID RAM banks.

11. RE(LCD Driver,WDT Control)(read/write)

7	6	5	4	3	2	1	0
-	/WDTE	/WUP9H	/WUP9L	/WURING	LCD_C2	LCD_C1	LCD_M

* Bit0 (LCD_M):LCD_M decides the methods, including duty, bias, and frame frequency.
* Bit1~Bit2 (LCD_C#):LCD_C# decides the LCD display enable or blanking. change the display duty must set the "LCD_C2,LCD_C1" to "00".

LCD_C2,LCD_C1	LCD Display Control	LCD_M	duty	bias
0 0	change duty Disable(turn off LCD)	0 1	1/16 1/8	1/4 1/4
0 1	Blanking	:	:	
1 1	LCD display enable	:	:	

* Bit3 (/WURING, RING Wake Up Enable): used to enable the wake-up function of /RINGTIME input pin. (1/0=enable/disable)
* Bit4 (/WUP9L, PORT9 low nibble Wake Up Enable): used to enable the wake-up function of low nibble in PORT9.(1/0=enable/disable)
* Bit5 (/WUP9H, PORT9 high nibble Wake Up Enable): used to enable the wake-up function of high nibble in PORT9.(1/0=enable/disable)
* Bit6 (/WDTE,Watch Dog Timer Enable)

Control bit used to enable Watchdog timer.(1/0=enable/disable)

The relation between Bit3 to Bit6 can see the diagram 9.

* Bit7 unused

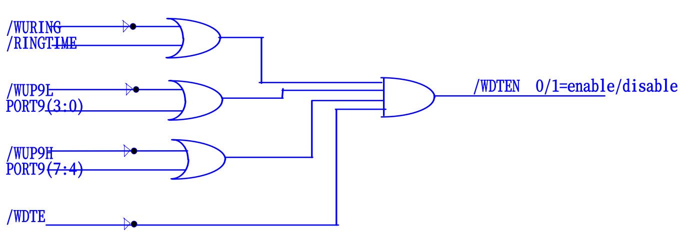


fig.9 Wake up function and control signal

12. RF (Interrupt Status Register)

7	6	5	4	3	2	1	0
INT3	FSKDATA	C8_2	C8_1	INT2	INT1	INT0	TCIF

* "1" means interrupt request, "0" means non-interrupt
* Bit 0 (TCIF) TCC timer overflow interrupt flag. Set when TCC timer overflows .

* Bit 1 (INT0) external INT0 pin interrupt flag .
* Bit 2 (INT1) external INT1 pin interrupt flag .
* Bit 3 (INT2) external INT2 pin interrupt flag .
* Bit 4 (C8_1) internal 8 bit counter interrupt flag .
* Bit 5 (C8_2) internal 8 bit counter interrupt flag .
* Bit 6 (FSKDATA) FSK data interrupt flag
* Bit 7 (INT3) external INT3 pin interrupt flag.
* High to low edge trigger , Refer to the Interrupt subsection.
* IOCF is the interrupt mask register. User can read and clear.

13. R10~R3F (General Purpose Register)

* R10~R3F (Banks 0~3) all are general purpose registers.

VII.2 Special Purpose Registers

1. A (Accumulator)

* Internal data transfer, or instruction operand holding
* It's not an addressable register.

2. CONT (Control Register)

7	6	5	4	3	2	1	0
-	INT	TS	-	PAB	PSR2	PSR1	PSR0

* Bit 0 (PSR0) ~ Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

* Bit 3 (PAB) Prescaler assignment bit.
  0/1 : TCC/WDT
* **Bit 4 unused**

* Bit 5 (TS) TCC signal source
  0: internal instruction cycle clock
  1: 16.38KHz

* **Bit 6 : (INT)INT enable flag**
  0: interrupt masked by DISI or hardware interrupt
  1: interrupt enabled by ENI/RETI instructions

* Bit 7 : unused

* CONT register is readable and writable.

3. IOC6 ~ IOC9 (I/O Port Control Register)
   * Five I/O direction control registers.
   * "1" put the relative I/O pin into high impedance, while "0" put the relative I/O pin as output.
   * User can see IOCB register how to switch to normal I/O port.

4. IOCA (CALLER ID RAM,IO ,PAGE Control Register)(read/write,initial "00000000")

7	6	5	4	3	2	1	0
P8SH	P8SL	-	CALL_4	CALL_3	CALL_2	CALL_1	**0**

* **Bit0 unused**
* Bit4~Bit1:"000" to "1001" are ten blocks of CALLER ID RAM area. User can use 2.5K RAM with RC ram address.
* Bit 5 unused
* Bit6: port8 low nibble switch, 0/1= normal I/O port/SEGMENT output .
* Bit7: port8 high nibble switch , 0/1= normal I/O port/SEGMENT output

5. IOCB (LCD ADDRESS)

PAGE0 : Bit6 ~ Bit0 = LCDA6 ~ LCDA0

The LCD display data is stored in the data RAM . The relation of data area and COM/SEG pin is as below:

COM15 ~ COM8	COM7 ~ COM0	
40H (Bit15 ~ Bit8)	00H (Bit7 ~ Bit0)	SEG0
41H	01H	SEG1
:	:	:
:	:	:
7BH	3BH	SEG59
7CH	3CH	Empty
7DH	3DH	Empty
7EH	3EH	Empty
7FH	3FH	Empty

PAGE1 : 8 bit up-counter (COUNTER1) preset and read out register . (write = preset) . After a interruption , it will count from “00”.

6. IOCC (LCD DATA)

PAGE0 : Bit7 ~ Bit0 = LCD RAM data register

PAGE1 : 8 bit up-counter (COUNTER2) preset and read out register . (write = preset) After a interruption , it will count from “00”.

7. IOCD (Pull-high Control Register)

PAGE0:

7	6	5	4	3	2	1	0
PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0

* Bit 0 ~ 7 (/PH#) Control bit used to enable the pull-high of PORT7(#) pin.
  1: Enable internal pull-high
  0: Disable internal pull-high

8. IOCE (Bias,PLL Control Register)

PAGE0 :

7	6	5	4	3	2	1	0
P9SH	P9SL	P6S	Bias3	Bias2	Bias1	**0**	**SC**

* Bit 0 :SC (SCAN KEY signal) 0/1 = disable/enable. Once you enable this bit , all of the LCD signal will have a low pulse during a common period. This pulse has 30us width. Please use the procedure to implement the key scan function. NOTE! Please connect a transistor with common signal to separate IO PORT.

a. set port7 as input port
b. set IOCD page0 port7 pull high
c. enable scan key signal
d. Once push a key . Set RA(6)=1 and switch to normal mode.
e. **Blank** LCD. Disable scan key signal.
f. Set P6S =0. Port6 sent probe signal to port7 and read port7. Get the key.
g. Note!! A probe signal should be delay a instruction at least to another probe signal.
h. Set P6S =1. Port6 as LCD signal. Enable LCD.

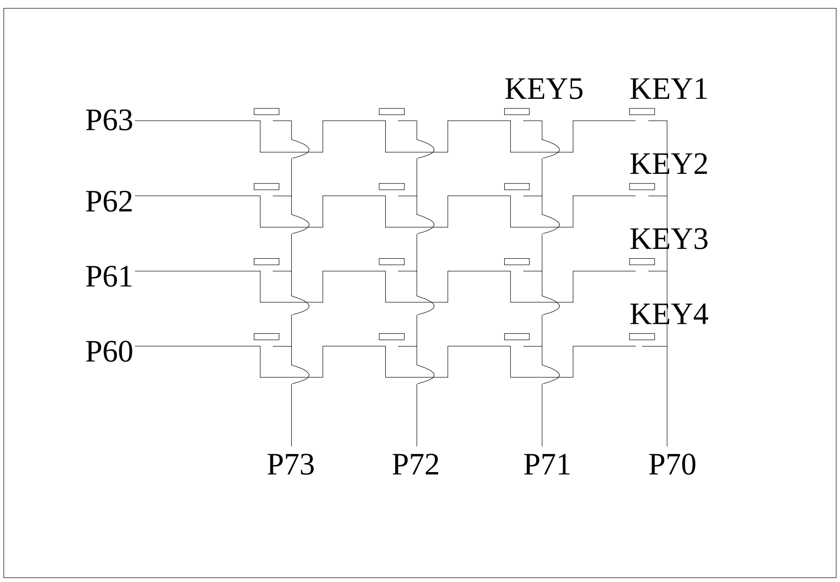


Fig.10. Key scan circuit

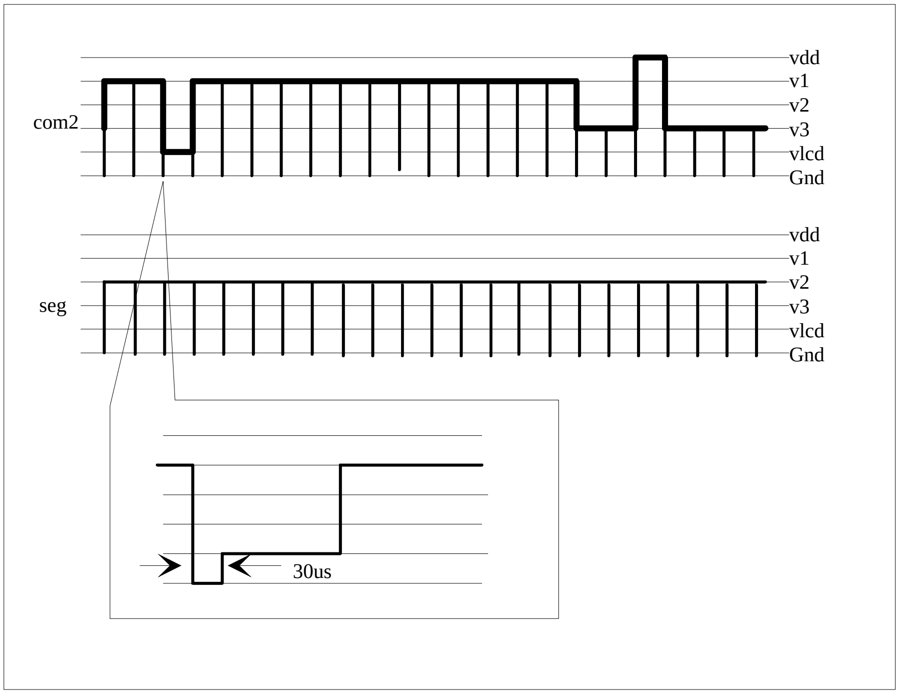


Fig.11.key scan signal

* **Bit 1 : zero**
* Bit 2~4 (Bias1~Bias3) Control bits used to choose LCD operation voltage .

LCD operate voltage	Vop (VDD 5V)	VDD=5V
000	0.60VDD	3.0V
001	0.66VDD	3.3V
010	0.74VDD	3.7V
011	0.82VDD	4.0V
100	0.87VDD	4.4V
101	0.93VDD	4.7V
110	0.96VDD	4.8V
111	1.00VDD	5.0V

* Bit5:port6 switch , 0/1= normal I/O port/COMMON output
* Bit6:port9 low nibble switch , 0/1= normal I/O port/SEGMENT output . Bit7:port9 high nibble switch

PAGE1 :

7	6	5	4	3	2	1	0
OP77	OP76	C2S	C1S	PSC1	PSC0	CDRD	-

* Bit0: unused
* Bit1: cooked data or raw data select bit , 0/1 ==> cooked data/raw data
* Bit3~Bit2: counter1 prescaler , reset=(0,0)
  (PSC1,PSC0) = (0,0)=>1:1 , (0,1)=>1:2 , (1,0)=>1:4 , (1,1)=>1:8
* Bit4**:counter1 source , (0/1)=(32768Hz/3.679MHz if enable)**
* Bit5:counter2 source , (0/1)=(32768Hz/3.679MHz if enable)   scale=1:1
* Bit6:P76 opendrain control   (0/1)=(disable/enable)
* Bit7:P77 opendrain control   (0/1)=(disable/enable)

9. IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
INT3	FSKDATA	C8_2	C8_1	INT2	INT1	INT0	TCIF

* Bit 0 ~ 7   interrupt enable bit.
  0: disable interrupt
  1: enable   interrupt
* IOCF Register is readable and writable.

VII.3 TCC/WDT Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

- An 8 bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register.
- See the prescaler ratio in CONT register.
- Fig. 12 depicts the circuit diagram of TCC/WDT.
- Both TCC and prescaler will be cleared by instructions which write to   TCC each time.
- The prescaler will be cleared by the WDTC and SLEP instructions, when assigned to WDT mode.
- **The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.**

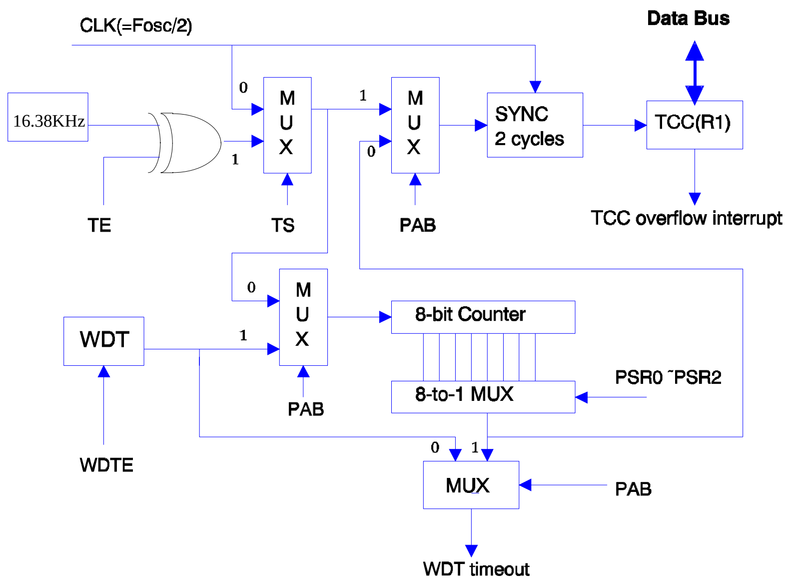


Fig. 12   Block diagram of TCC WDT

VII.4 I/O Ports

The I/O registers, Port 6 ~ Port 9, are bi-directional tri-state I/O ports. Port 7 can be pulled-high internally by software control. The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC6 ~ IOC9) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.13.

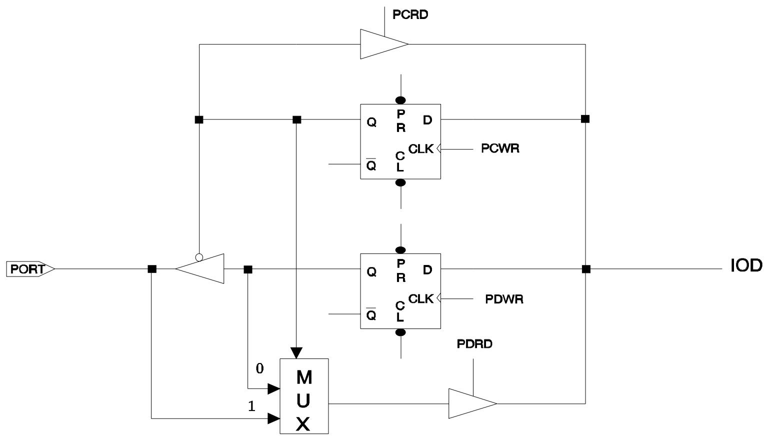


Fig. 13 The circuit of I/O port and I/O control register

VII.5 RESET and Wake-up

The RESET can be caused by

(1) Power on reset, or Voltage detector

(2) WDT timeout. (if enabled and in GREEN or NORMAL mode)

Note that only Power on reset, or only Voltage detector in Case(1) is enabled in the system by CODE Option bit. If Voltage detector is disabled, Power on reset is selected in Case (1). Refer to Fig. 14.

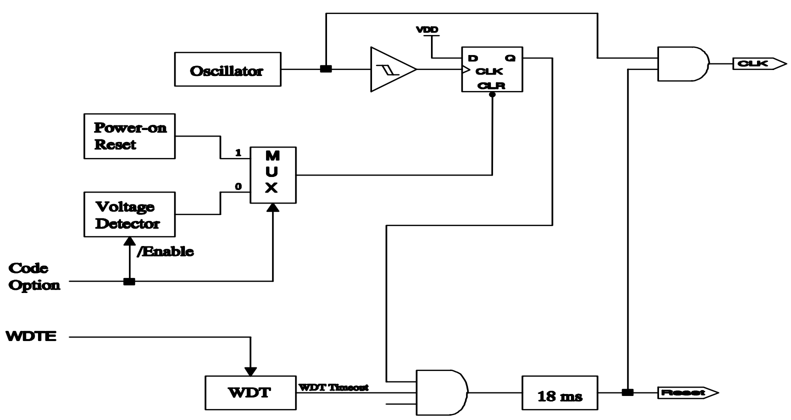


Fig. 14 Block diagram of Reset of controller

Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"
- The other register (bit7..bit0)

R5 = "00000000"		
R6 = PORT	IOC6 = "11111111"	
R7 = PORT	IOC7 = "11111111"	
R8 = PORT	IOC8 = "11111111"	
R9 = PORT	IOC9 = "11111111"	
RA = "000x0xxx	IOCA = "00000000"	
RB = "11111111"	Page0 IOCB = "00000000"	Page1 IOCB = "00000000"
RC = "00000000"	Page0 IOCC = "0xxxxxxx"	Page1 IOCC = "00000000"
RD = "xxxxxxxx"	Page0 IOCD = "00000000"	
RE = "00000000"	Page0 IOCE = "00000000"	Page1 IOCE = "00000000"
RF = "00000000"	IOCF = "00000000"	

The controller can be awakened from SLEEP mode or IDLE mode (execution of "SLEP" instruction, named as SLEEP MODE or IDLE mode) by (1)TCC time out (IDLE mode only) (2) WDT time-out (if enabled) or, (3) external input at PORT9 (4)RINGTIME pin. The four cases will cause the controller wake up and run from next instruction in IDLE mode , reset in SLEEP mode . After wake-up , user should control WATCH DOG in case of reset in GREEN mode or NORMAL mode. The last three should be open RE register before into SLEEP mode or IDLE mode . The first one case will set a flag in RF bit0 . And it will go to address 0x08 when TCC generate a interrupt .

VII.6 Interrupt

The CALLER ID IC has internal interrupts which are falling edge triggered, as followed : TCC timer overflow interrupt (internal) , two 8-bit counters overflow interrupt .

If these interrupt sources change signal from high to low , then RF register will generate '1' flag to corresponding register if you enable IOCF register.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

There are four external interrupt pins including INT0 , INT1 , INT2 , INT3 . And four internal counter interrupt available.

External interrupt INT0 , INT1 , INT2 , INT3 signals are from PORT7 bit0 to bit3 . If IOCF is enable then these signal will cause interrupt , or these signals will be treated as general input data .

After reset, the next instruction will be fetched from address 000H and the instruction inturrept is 001H and the hardware inturrept is 008H.

TCC will go to address 0x08 in GREEN mode or NORMAL mode after time out. And it will run next instruction from "SLEP" instruction and then go to address 0x08 in IDLE mode . These two cases will set a RF flag.

VII.7 Instruction Set

Instruction set has the following features:
(1). Every bit of any register can be set, cleared, or tested directly.
(2). The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z

0	0011	10rr	rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0	0011	11rr	rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0	0100	00rr	rrrr	04rr	MOV A,R	R → A	Z
0	0100	01rr	rrrr	04rr	MOV R,R	R → R	Z
0	0100	10rr	rrrr	04rr	COMA R	/R → A	Z
0	0100	11rr	rrrr	04rr	COM R	/R → R	Z
0	0101	00rr	rrrr	05rr	INCA R	R+1 → A	Z
0	0101	01rr	rrrr	05rr	INC R	R+1 → R	Z
0	0101	10rr	rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0	0101	11rr	rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0	0110	00rr	rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C
0	0110	01rr	rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C
0	0110	10rr	rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C
0	0110	11rr	rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C
0	0111	00rr	rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None
0	0111	01rr	rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0	0111	10rr	rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0	0111	11rr	rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0	100b	bbrr	rrrr	0xxx	BC R,b	0 → R(b)	None
0	101b	bbrr	rrrr	0xxx	BS R,b	1 → R(b)	None
0	110b	bbrr	rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0	111b	bbrr	rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1	00kk	kkkk	kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None
1	01kk	kkkk	kkkk	1kkk	JMP k	(Page, k) → PC	None
1	1000	kkkk	kkkk	18kk	MOV A,k	k → A	None
1	1001	kkkk	kkkk	19kk	OR A,k	A ∨ k → A	Z
1	1010	kkkk	kkkk	1Akk	AND A,k	A & k → A	Z
1	1011	kkkk	kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1	1100	kkkk	kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1	1101	kkkk	kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1	1110	0000	0001	1E01	INT	PC+1 → [SP] 001H → PC	None
1	**1110**	**1000**	**kkkk**	**1E8k**	**PAGE k**	**K->R5**	**None**
1	1111	kkkk	kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

VII.9 FSK FUNCTION

VII.9.1 Functional Block Diagram

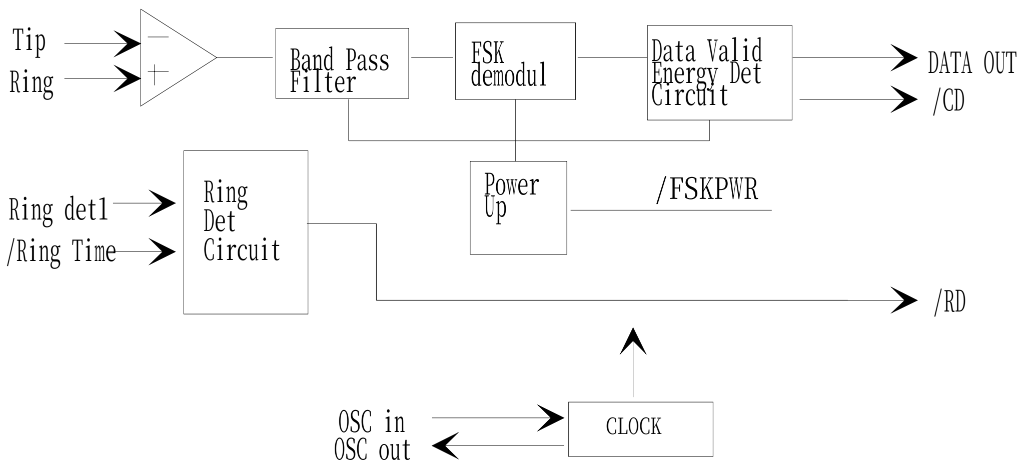


Fig15. FSK Block Diagram

VII.9.2 Function Descriptions

The CALLER ID IC is a CMOS device designed to support the Caller Number Deliver feature which is offered by the Regional Bell Operating Companies.The FSK block comprises two paths: the signal path and the ring indicator path. The signal path consist of an input differential buffer,a band pass filter, an FSK demodulator and a data valid with carrier detect circuit. The ring detector path includes a clock generator, a ring detect circuit .

In a typical application, the ring detector maintains the line continuously while all other functions of the chip are inhibited. If a ring signal is sent, the /RINGTIME pin will has a low signal. User can use this signal to wake up whole chip or read /RD signal from RA register.

A /FSKPWR input is provided to activate the block regardless of the presence of a power ring signal. If /FSKPWR is sent low, the FSK block will power down whenever it detects a valid ring signal, it will power on when /FSKPWR is high.

The input buffer accepts a differential AC coupled input signal through the TIP and RING input and feeds this signal to a band pass filter. Once the signal is filtered, the FSK demodulator decodes the information and sends it to a post filter. The output data is then made available at DATA OUT pin. This data, as sent by the central office, includes the header information (alternate "1" and "0") and 150 ms of marking which precedes the date , time and calling number. If no data is present, the DATA OUT pin is held in a high state. This is accomplished by an carrier detect circuit which determines if the in-band energy is high enough. If the incoming signal is valid and thus the demodulated data is transferred to DATA OUT pin . If it is not, then the FSK demodulator is blocked.

VII.9.3 Ring detect circuit

When Vdd is applied to the circuit, the RC network will charge cap C1 to Vdd holding /RING TIME off . The resistor network R2 to R3 attenuates the incoming power ring applied to the top of R2. The values given have been chosen to provide a sufficient voltage at DET1 pin, to turn on the Schmitt trigger input. When Vt+ of the Schmitt is exceeded, cap C1 will discharge.

The value of R1 and C1 must be chosen to hold the /RING TIME pin voltage below the Vt+ of the Schmitt between the individual cycle of the power ring. With /RINGTIME enabled, this signal will be a /RD signal in RA throught a buffer.

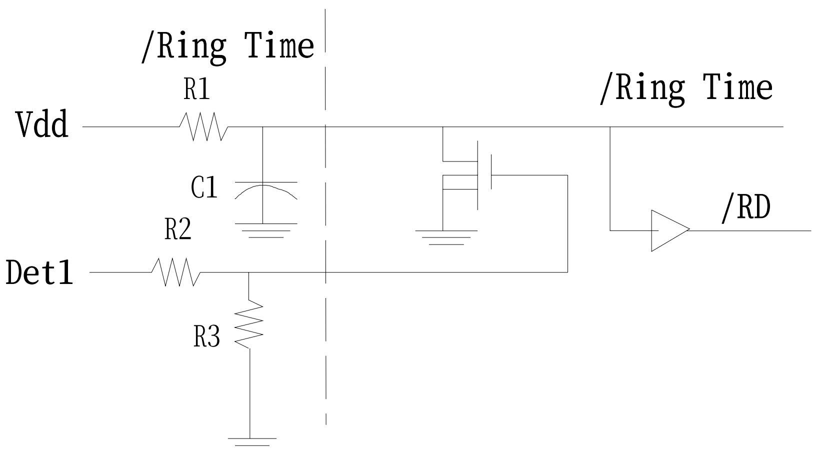


Fig16. ring detect circuit

VII.10 DTMF (Dual Tone Multi Frequency) Tone Generator

Built-in DTMF generator can generate dialing tone signals for telephone of dialing tone type. There are two kinds of DTMF tone . One is the group of row frequency, the other is the group of column frequency, each group has 4 kinds of frequency , user can get 16 kinds of DTMF frequency totally. DTMF generator contains a row frequency sine wave generator for generating the DTMF signal which selected by low order 4 bits of RB and a column frequency sine wave generator for generating the DTMF signal which selected by high order 4 bits of RB. This block can generate single tone by filling one bit zero to this register.

If all the values are high , the power of DTMF will turn off until one or two low values.

Either high or low 4 bits must be set by an effective value, otherwise, if any ineffective value or both 4 bits are load effective value, tone output will be disable. Recommend value refer to table as follow please :

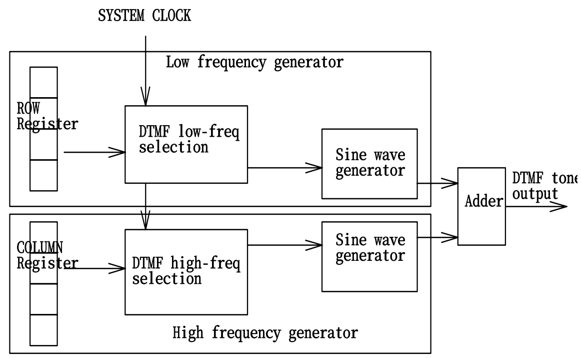


Fig17. DTMF Block Diagram

* RB (DTMF Register)

. Bit 0 - Bit 3 are row-frequency tone.
. Bit 4 - Bit 7 are column-frequency tone.
. Initial RB is equal to HIGH.
. Except below values of RB ,the other values of RB are not effect. If RB is set by ineffective value, the DTMF output will be disable and there is no tone output.
. Bit 7 ~ 0 are all "1" , turn off DTMF power .

bit 3~0	Row freq				
1110	699.2Hz	1	2	3	A
1101	771.6Hz	4	5	6	B
1011	854Hz	7	8	9	C
0111	940.1Hz	*	0	#	D
Column freq		1203Hz	1331.8Hz	1472Hz	1645.2Hz
bit 7~4		1110	1101	1011	0111

VII.11 LCD Driver

The CALLER ID IC can drive LCD directly and has 60 segments and 16 commons that can drive 60*16 dots totally. LCD block is made up of LCD driver , display RAM, segment output pins , common output pins and LCD operating power supply pins.

Duty , bias , the number of segment , the number of common and frame frequency are determined by LCD mode register . LCD control register.

The basic structure contains a timing control which uses the basic frequency 32.768KHz to generate the proper timing for different duty and display access. RE register is a command register for LCD driver, the LCD display(disable, enable, blanking) is controlled by LCD_C and the driving duty and bias is decided by LCD_M and the display data is stored in data RAM which address and data access controlled by registers RC and RD.

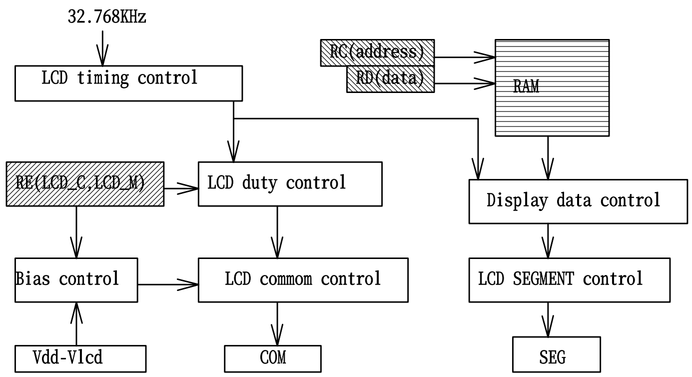


Fig18. LCD DRIVER CONTROL

VII.11.1 LCD Driver Control

1. RE(LCD Driver Control)(initial state "00000000")

7	6	5	4	3	2	1	0
-	-	-	-	-	LCD_C2	LCD_C1	LCD_M

*Bit0 (LCD_M):LCD_M decides the methods, including duty, bias, and frame frequency.

*Bit1~Bit2 (LCD_C#):LCD_C# decides the LCD display enable or blanking. change the display duty must set the LCD_C to "00".

LCD_C2,LCD_C1	LCD Display Control	LCD_M	duty	bias
0 0	change duty Disable(turn off LCD)	0 1	1/16 1/8	1/4 1/4
0 1	Blanking	:	:	
1 1	LCD display enable	:	:	

VII.11.2 LCD display area

The LCD display data is stored in the data RAM . The relation of data area and COM/SEG pin is as below:

COM15 ~ COM8	COM7 ~ COM0	
40H (Bit15 ~ Bit8)	00H (Bit7 ~ Bit0)	SEG0
41H	01H	SEG1
:	:	:
:	:	:
7BH	3BH	SEG59
7CH	3CH	empty
7DH	3DH	empty
7EH	3EH	empty
7FH	3FH	empty

*IOCB(LCD Display RAM address)

7	6	5	4	3	2	1	0

-	LCDA6	LCDA5	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0

Bit 0 ~ Bit 6 select LCD Display RAM address up to 120.
LCD RAM can be write whether in enable or disable mode and read only in disable mode.

*IOCC(LCD Display data) : Bit 0 ~ Bit 8 are LCD data.

VII.11.3 LCD COM and SEG signal

* COM signal : The number of COM pins varies according to the duty cycle used, as following: in 1/8 duty mode COM8 ~ COM15 must be open. in 1/16 duty mode COM0 ~ COM15 pins must be used.

	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8	..	COM15
1/8	o	o	o	o	o	o	o	o	x	..	x
1/16	o	o	o	o	o	o	o	o	o	..	o

x:open,o:select

* SEG signal: The 60 segment signal pins are connected to the corresponding display RAM address 00h to 3Bh. The high byte and the low byte bit7 down to bit0 are correlated to COM15 to COM0 respectively .
When a bit of display RAM is 1, a select signal is sent to the corresponding segment pin, and when the bit is 0 , a non-select signal is sent to the corresponding segment pin.
*COM, SEG and Select/Non-select signal is shown as following:

Refer to EM78811 spec.
Fig.19 Lcd wave 1/4 bias , 1/8 duty

Refer to EM78811 spec.
Fig.20 Lcd wave 1/4 bias , 1/16 duty

VII.11.4 LCD Bias control

IOCE (Bias Control Register)

7	6	5	4	3	2	1	0
			Bias3	Bias2	Bias1		

* Bit 2~4 (Bias1~Bias3) Control bits used to choose LCD operation voltage . The circuit can refer ti figure15.

LCD operate voltage	Vop (VDD 5V)	VDD=5V
000	0.60VDD	3.0V
001	0.66VDD	3.3V
010	0.74VDD	3.7V
011	0.82VDD	4.0V
100	0.87VDD	4.4V
101	0.93VDD	4.7V
110	0.96VDD	4.8V
111	1.00VDD	5.0V

* Bit 5~7 unused

Refer to EM78811 spec.
Fig.21 LCD bias circuit

VIII.Absolute Operation Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC SUPPLY VOLTAGE	Vdd	-0.3 To 6	V
INPUT VOLTAGE	Vin	-0.5 TO Vdd +0.5	V
OPERATING TEMPERATURE RANGE	Ta	0 TO 70	℃

IX DC Electrical Characteristic

(Ta=0°C ~ 70°C, VDD=5V±5%, VSS=0V)
(VDD=2.5V to 5.5V for CPU ; VDD=3.5V to 5.5V for FSK ; VDD=2.5V to 5.5V for DTMF)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IIL1	Input Leakage Current for input pins	VIN = VDD, VSS			±1	μA
IIL2	Input Leakage Current for bi-directional pins	VIN = VDD, VSS			±1	μA
VIH	Input High Voltage		2.5			V
VIL	Input Low Voltage				0.8	V
VIHT	Input High Threshold Voltage	/RESET, TCC, RDET1	2.0			V
VILT	Input Low Threshold Voltage	/RESET, TCC,RDET1			0.8	V
VIHX	Clock Input High Voltage	OSCI	3.5			V
VILX	Clock Input Low Voltage	OSCI			1.5	V
VHscan	Key scan Input High Voltage	Port6 for key scan	3.5			V
VLscan	Key scan Input Low Voltage	Port6 for key scan			1.5	V
VOH1	Output High Voltage (port6,7,8)	IOH = -1.6mA	2.4			V
	(port9)	IOH = -6.0mA	2.4			V
VOL1	Output Low Voltage (port6,7,8)	IOL = 1.6mA			0.4	V
	(port9)	IOL = 6.0mA			0.4	V
Vcom	Com voltage drop	Io=+/- 50 uA	-	-	2.9	V
Vseg	Segment voltage drop	Io=+/- 50 uA	-	-	3.8	V
Vlcd	LCD drive reference voltage	Contrast adjustment				
IPH	Pull-high current	Pull-high active input pin at VSS	-50	-100	-240	μA
ISB1	Power down current	All input and I/O pin at VDD, output pin floating, WDT disabled			4	μA
ISB2	Low clock current	CLK=32.768KHz, FSK, DTMF block disable , All input and I/O pin at VDD, output pin floating, WDT disabled, LCD enable			100	μA
ICC	Operating supply current	/RESET=High,			2.8	mA

		CLK=3.679MHz, output pin floating, FSK, DTMFblock disable				

IX AC Electrical Characteristic

(Ta=0°C ~ 70°C, VDD=5V, VSS=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time	32.768K 3.679M		60 550		us ns
Tdrh	Device delay hold time			18		ms
Ttcc	TCC input period	Note 1	(Tins+20)/N			ns
Twdt	Watchdog timer period	Ta = 25°C		18		ms

Note 1: N= selected prescaler ratio.

(FSK AC Characteristic)

Description	Symbol	Min	Typ	Max	Unit
OSC start up(32.768KHz) (3.679MHz PLL)	Tosc	--		400 10	ms
Carrier detect low	Tcdl	--	10	14	ms
Data out to Carrier det low	Tdoc	--	10	20	ns
Power up low to FSK(setup time)	Tsup	--	15	20	ms
/RD low to Ringtime low	Trd			10	ms
End of FSK to Carrier Detect high	Tcdh	8	--	--	ms

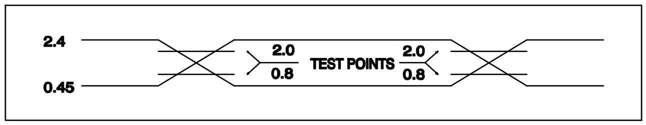
Please watch out the FSK setup time

(OTP AC Characteristic)

Description	Symbol	Min	Typ	Max	Unit
Vpp to VDD level setup time	Trs	2			uS
Mode code setup time	Tcsu	3			uS
Mode code hold time	Tchd	2			uS
Data setup time	Tdsu	100			nS
Data hold time	Tdhd	100			nS
Program write pulse width	Tpwd		200		uS
Output enable setup time	Toed	300			nS
Data clock pulse width	Tph	100			nS

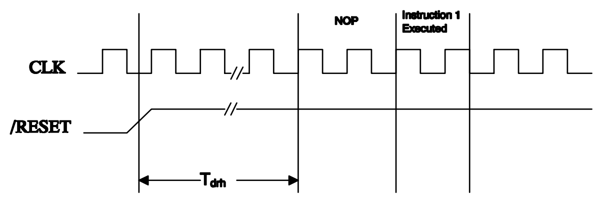
XI. Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

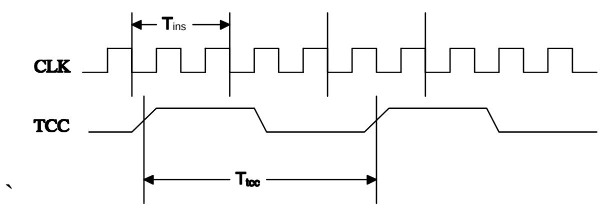


Fig.22 AC timing

XII. Application Circuit

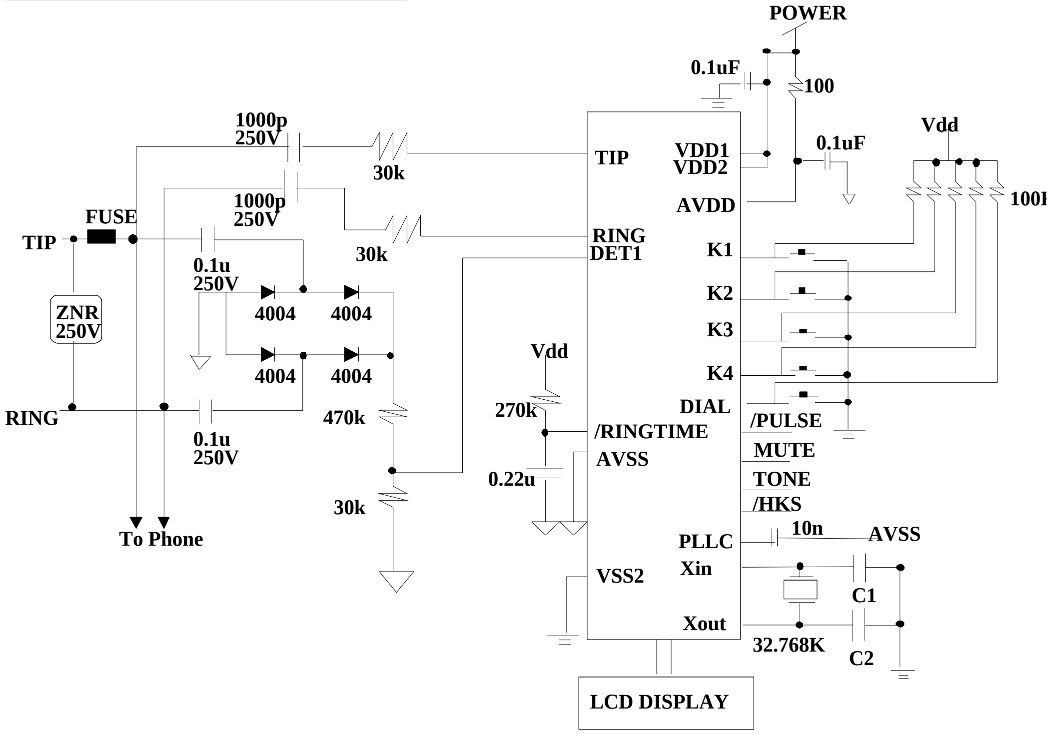


Fig.24.application circuit