SL2101

Synthesized Broadband Converter with Programmable Power

Data Sheet

August 2004

Features

- Single chip synthesized broadband solution
- Configurable as both up converter and downconverter requirements in double conversion tuner applications
- Incorporates 8 programmable mixer power settings
- Compatible with digital and analogue system requirements
- CSO -65 dBc, CTB -68 dBc (typical)
- Extremely low phase noise balanced local oscillator, with very low fundamental and harmonic radiation
- PLL frequency synthesizer designed for high comparison frequencies and low phase noise
- Buffered crystal output for pipelining system reference frequency
- I^2C Controlled

Applications

- Double conversion tuners
- Digital Terrestrial tuners
- Cable telephony
- Cable Modems
- MATV

Ordering Information

SL2101C/KG/NP1P	SSOP	Tubes
SL2101C/KG/NP1Q	SSOP	Tape & Reel
SL2101C/KG/NP2P	SSOP*	Tubes
SL2101C/KG/NP2Q	SSOP*	Tape & Reel
SL2101C/KG/LH2N	MLP*	Trays
SL2101C/KG/LH2Q	MLP*	Tape& Reel

* Pb free

All codes baked and drypacked

-40°C to +85°C

Description

The SL2101 is a fully integrated single chip broadband mixer oscillator with low phase noise PLL frequency synthesizer. It is intended for use in double conversion tuners as both the up and down converter and is compatible with HIIF frequencies up to 1.4 GHz and all standard tuner IF output frequencies. It also contains a programmable power facility for use in systems where power consumption is important.

The device contains all elements necessary, with the exception of local oscillator tuning network, loop filter and crystal reference to produce a complete synthesized block converter, compatible with digital and analogue requirements.

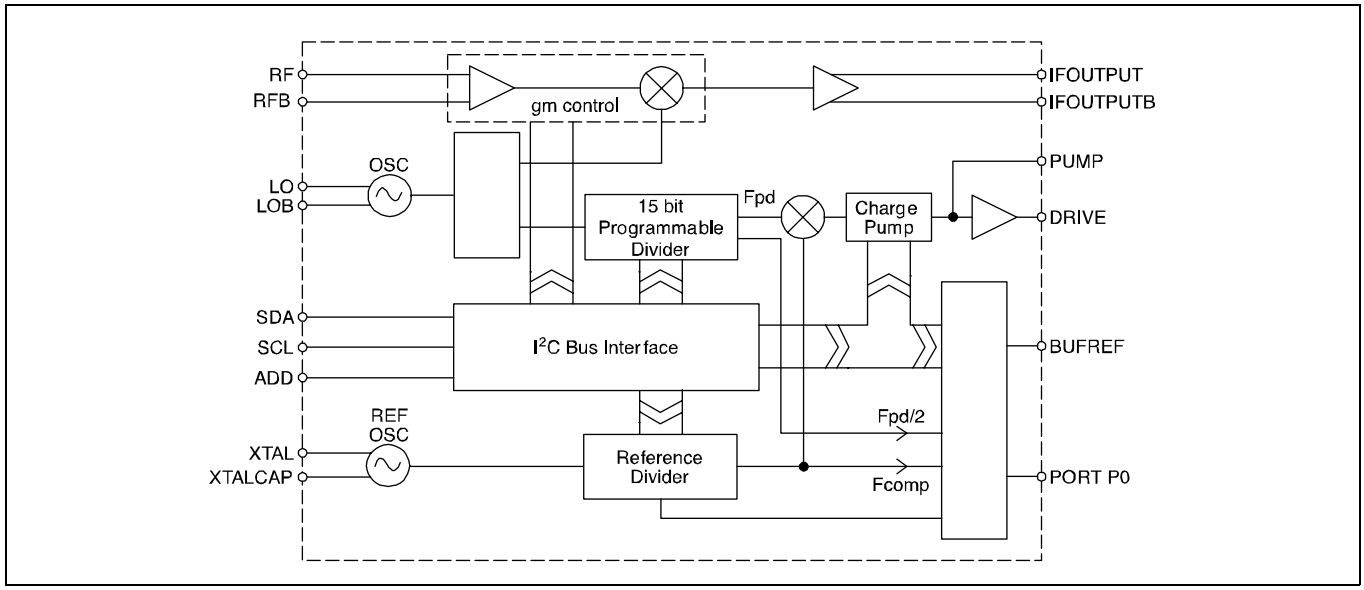


Figure 1 - Functional Block Diagram

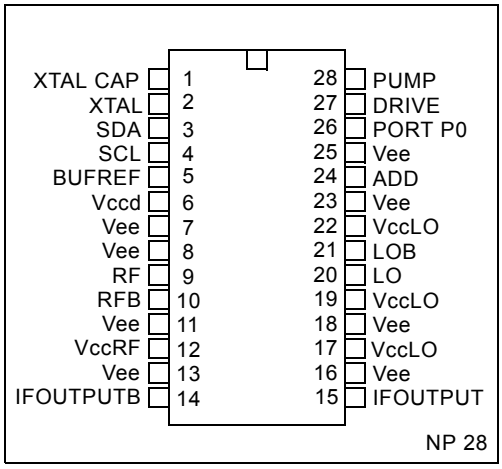


Figure 2 - Pin Diagram SSOP Package

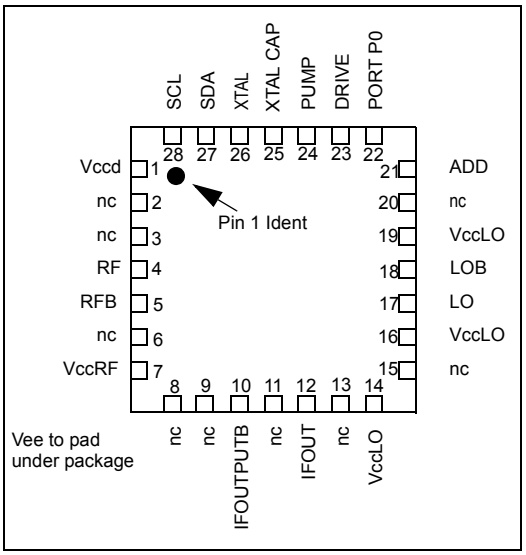


Figure 3 - Pin Diagram MLP Package

Quick Reference Data

All data applies at maximum power setting with the following conditions unless otherwise stated;

a) nominal loads as follows;

1220 MHz output load as in Figure 4

44 MHz output load as in Figure 5

b) input signal per carrier of 63 dBμV

Characteristic		Units
RF input operating range	50-1400	MHz
Input noise figure, SSB, 50-860 MHz 860-1400	 6.5 - 8.5 8.5 - 12	 dB dB
Conversion gain	12	dB
CTB (fully loaded matrix)	-68	dBc
CSO (fully loaded matrix)	-65	dBc
P1 dB input referred	110	dBμV
Local oscillator phase noise as upconverter SSB @ 10 kHz offset SSB @ 100 kHz offset	 -90 -112	 dBc/Hz dBc/Hz
Local oscillator phase noise as downconverter SSB @ 10 kHz offset SSB @ 100 kHz offset	 -93 -115	 dBc/Hz dBc/Hz
Local oscillator phase noise floor	-136	dBc/Hz
PLL spurs on converted output with input @ 60 dBμV	<-70	dBc
PLL maximum comparison frequency	4	MHz
PLL phase noise at phase detector	-152	dBc/Hz

*dBm assumes a 75 Ω characteristic impedance, and 0 dBm = 109 dBμV

Functional Description

The SL2101 is a broadband wide dynamic range mixer oscillator with on-board I^2C bus controlled PLL frequency synthesizer, optimized for application in double conversion tuner systems as both the up and down converter. It also has application in any system where a wide dynamic range broadband synthesized frequency converter is required.

The SL2101 is a single chip solution containing all necessary active circuitry and simply requires an external tuneable resonant network for the local oscillator sustaining network. The pin assignment is contained in Figures 2 and 3 for the SSOP and MLP packages and the block diagram in Figure 1.

The device also contains a programmable facility to adjust the power in the lna/mixer so allowing power to be traded against intermodulation performance for power critical applications, such as telephony modems.

Converter Section

In normal application the RF input is interfaced through appropriate impedance matching and an AGC front end to the device input. The RF input preamplifier of the device is designed for low noise figure, within the operating region of 50 to 1400 MHz and for high intermodulation distortion intercept so offering good signal to noise plus composite distortion spurious performance when loaded with a multi carrier system. The preamplifier also provides gain to the mixer section and back isolation from the local oscillator section.

The lna/mixer current and hence signal handling and device power consumption are programmable through the I^2C bus as tabulated in Figure 7.

The typical RF input impedance and matching network for broadband upconversion are contained in Figures 8 and 9 respectively and for narrow band downconversion in Figures 10 and 11 respectively. The input referred two tone intermodulation test condition spectrum at maximum power setting is shown in Figure 12. The typical input NF and gain versus frequency and NF specification limits, over selectable power settings are contained in Figures 13, 14 and 15 respectively.

The output of the preamplifier is fed to the mixer section which is optimized for low radiation application. In this stage the RF signal is mixed with the local oscillator frequency, which is generated by the on-board oscillator. The oscillator block uses an external tuneable network and is optimized for low phase noise. The typical oscillator application as an upconverter is shown in Figure 16 and the typical phase noise performance in Figure 17. The typical oscillator application as a downconverter is shown in Figure 18, and the phase noise performance in Figure 19. This oscillator block interfaces direct with the internal PLL to allow for frequency synthesis of the local oscillator.

Finally the output of the mixer provides an open collector differential output drive. The device allows for selection of an IF in the range 30-1400 MHz so covering standard HIIFs between 1 and 1.4 GHz and all conventional tuner output IFs. When used as a broadband upconverter to a HIIF the output should be differentially loaded, for example with a differential SAW filter, to maximize intermodulation performance. A nominal load in maximum power setting is shown in Figure 4, which will typically be terminated with a differential 200 load. When used as a narrowband downconverter the output should be differentially loaded with a discrete differential to single ended converter as in Figure 5, shown tuned to 44 MHz IF. Alternatively loading can be direct into a differential input amplifier or SAWF, in which case external loads to Vcc will be required. An example load for 44 MHz application with a gain of 16 dB is contained in Figure 6. The NF and gain with recommended load versus power setting are contained in Figure 20.

The typical IF output impedance as upconverter and downconverter are contained in Figures 21 and 22 respectively.

In all applications care should be taken to achieve symmetric balance to the IF outputs to maximize intermodulation performance.

The typical key performance data at 5V Vcc and 25 deg C ambient are shown in the section 'Quick Reference Data'.

PLL Frequency Synthesizer

The PLL frequency synthesizer section contains all the elements necessary, with the exception of a reference frequency source and loop filter to control the oscillator, so forming a complete PLL frequency synthesized source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance.

The LO signal from the oscillator drives an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier interfaces direct with the 15-bit fully programmable divider. The programmable divider is of MN+A architecture, where the dual modulus prescaler is 16/17, the A counter is 4-bits, and the M counter is 11 bits.

The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on-board crystal controlled oscillator or from an external reference source. In both cases the reference frequency is divided down to

the comparison frequency by the reference divider which is programmable into 1 of 29 ratios as detailed in figure 23. Typical applications for the crystal oscillator are contained in Figure 24 and Figure 25. Figure 25 is used when driving a second SL2101 as a downconverter.

The output of the phase detector feeds a charge pump and loop amplifier, which when used with an external loop filter and high voltage transistor, integrates the current pulses into the varactor line voltage, used for controlling the oscillator.

The programmable divider output Fpd divided by two and the reference divider output Fcomp can be switched to port P0 by programming the device into test mode. The test modes are described in Figure 26.

The crystal reference frequency can be switched to BUFREF output by bit RE as described in Figure 27. The BUFREF output is not available on the MLP package.

Programming

The SL2101 is controlled by an I^2C data bus and is compatible with both standard and fast mode formats.

Data and Clock are fed in on the SDA and SCL lines respectively as defined by I^2C bus format. The device can either accept data (write mode), or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low, and read mode if it is high. Tables 1 and 2 in Figure 28 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one device in an I^2C bus system. Figure 28, Table 3 shows how the address is selected by applying a voltage to the 'ADD' input. When the device receives a valid address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are received. When the device is programmed into read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

Write Mode

With reference to Figure 28, Table 1, bytes 2 and 3 contain frequency information bits 2^{14} -2^0 inclusive.

Byte 4 controls the synthesizer reference divider ratio, see Figure 23 and the charge pump setting, see Figure 29. Byte 5 controls the test modes, see Figure 26, the buffered crystal reference output select RE, see Figure 27, the power setting, see Figure 7 and the output port P0.

After reception and acknowledgement of a correct address (byte 1), the first bit of the following byte determines whether the byte is interpreted as a byte 2 or 4, a logic '0' indicating byte 2, and a logic '1' indicating byte 4. Having interpreted this byte as either byte 2 or 4 the following data byte will be interpreted as byte 3 or 5 respectively. Having received two complete data bytes, additional data bytes can be entered, where byte interpretation follows the same procedure, without re-addressing the device. This procedure continues until a STOP condition is received. The STOP condition can be generated after any data byte, if however it occurs during a byte transmission, the previous byte data is retained. To facilitate smooth fine tuning, the frequency data bytes are only accepted by the device after all 15 bits of frequency data have been received, or after the generation of a STOP condition.

Read Mode

When the device is in read mode, the status byte read from the device takes the form shown in Figure 28, Table 2.

Bit 1 (POR) is the power-on reset indicator, and this is set to a logic '1' if the Vcc supply to the device has dropped below 3V (at 25° C), e.g., when the device is initially turned ON. The POR is reset to '0' when the read sequence is terminated by a STOP command. When POR is set high this indicates that the programmed information may have been corrupted and the device reset to the power up condition.

Bit 2 (FL) indicates whether the synthesizer is phase locked, a logic '1' is present if the device is locked, and a logic '0' if the device is unlocked.

Programmable Features

Synthesizer programmable divider	Function as described above
Reference programmable divider	Function as described above.
Charge pump current	The charge pump current can be programmed by bits C1 & C0 within data byte 4, as defined in Figure 29.
Power setting	The device power and hence signal handling can be programmed by bits I2 - I0 within data byte 5, as defined in Figure 7. In all power settings the synthesizer remains enabled to facilitate rapid PLL lock reacquisition
Test mode	The test modes are defined by bits T2 - T0 as described in Figure 26.
General purpose ports, P0	The general purpose port can be programmed by bits P0; Logic '1' = on Logic '0' = off (high impedance) - this is the default state at device power on
Buffered crystal reference output, BUFREF	The buffered crystal reference frequency can be switched to the BUFREF output by bit RE as described in Figure 27. The BUFREF output defaults to the 'ON' condition at device power up. This output is only available on the SSOP package.

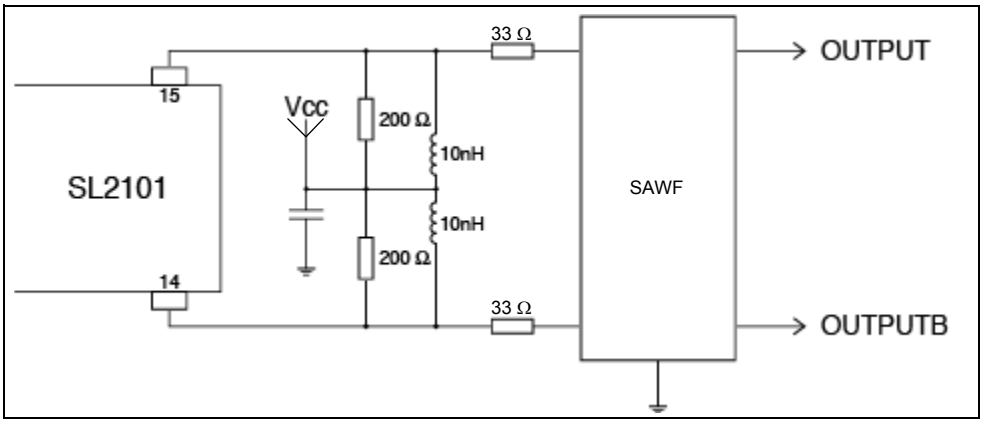


Figure 4 - Nominal Output Load as Upconverter into Differential SAWF

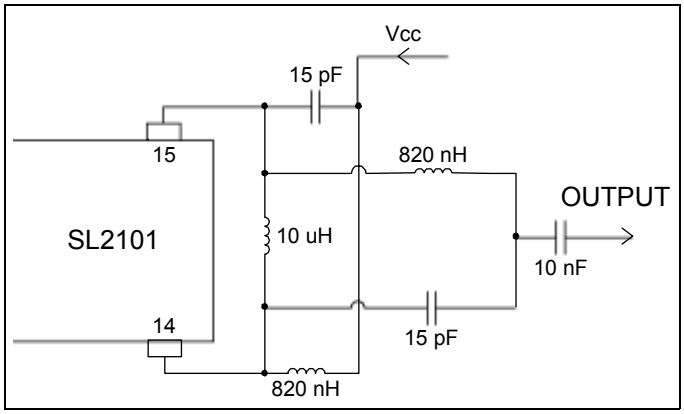


Figure 5 - Nominal Output Load as Downconverter, 44 MHz IF

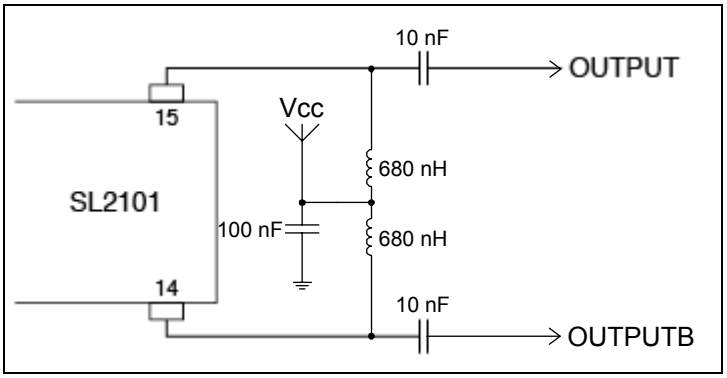


Figure 6 - Output Load as Downconverter to a Differential Amplifier

I2	I1	I0	Supply Current in mA	
			Typ.	Max.
0	0	0	90*	120
0	0	1	67	89
0	1	0	56	75
0	1	1	51	68
1	0	0	82	109
1	0	1	59	78
1	1	0	48	64
1	1	1	43	57

Figure 7 - Supply Current

* default setting on SL2101

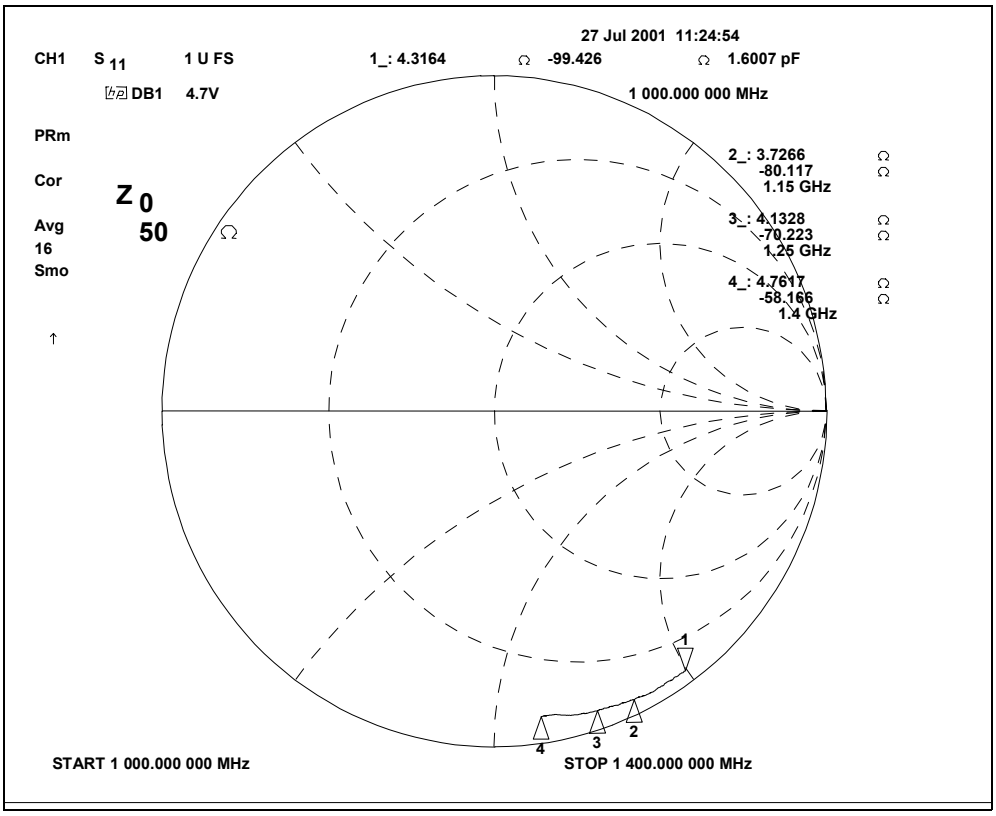


Figure 8 - Typical RF Input Impedance as Broadband Upconverter (Maximum Power Setting)

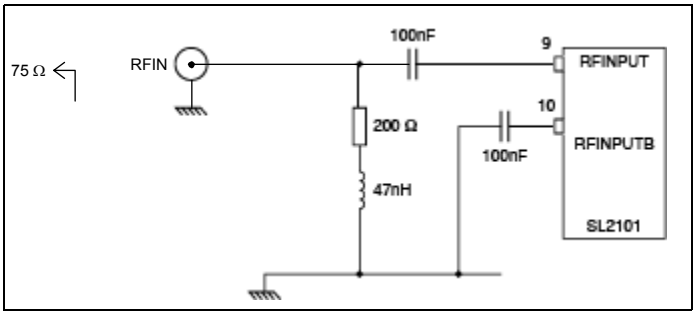


Figure 9 - RF Input Impedance Matching Network as 50 - 860 MHz Upconverter

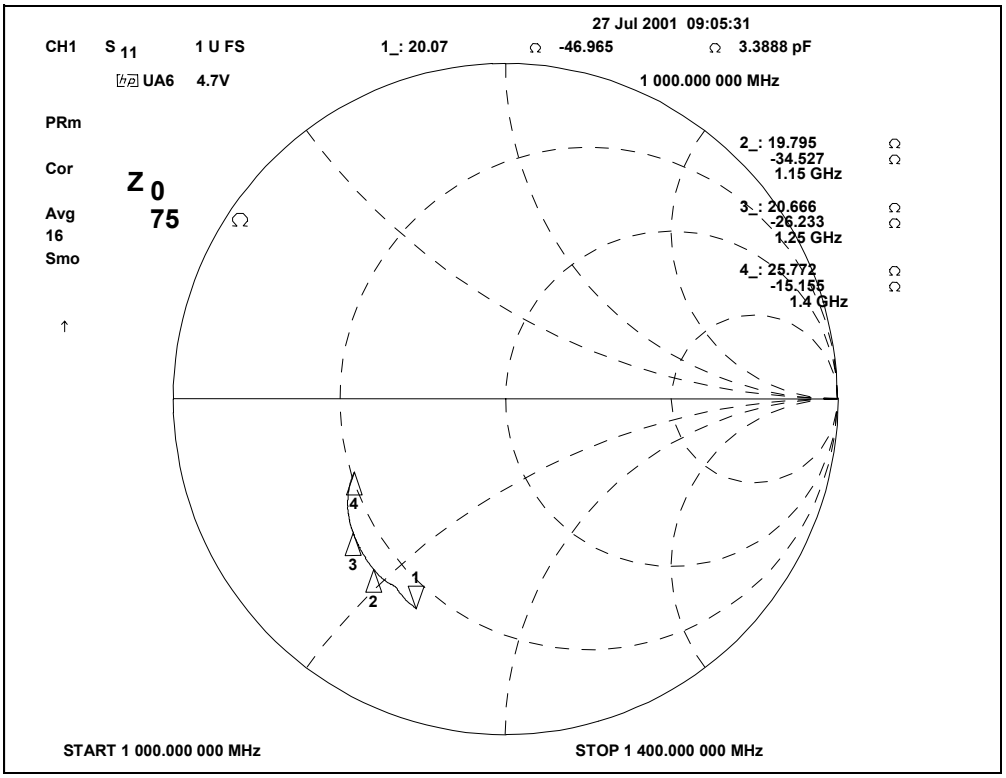


Figure 10 - Typical RF Input Impedance as Narrow Band Downconverter (maximum power setting)

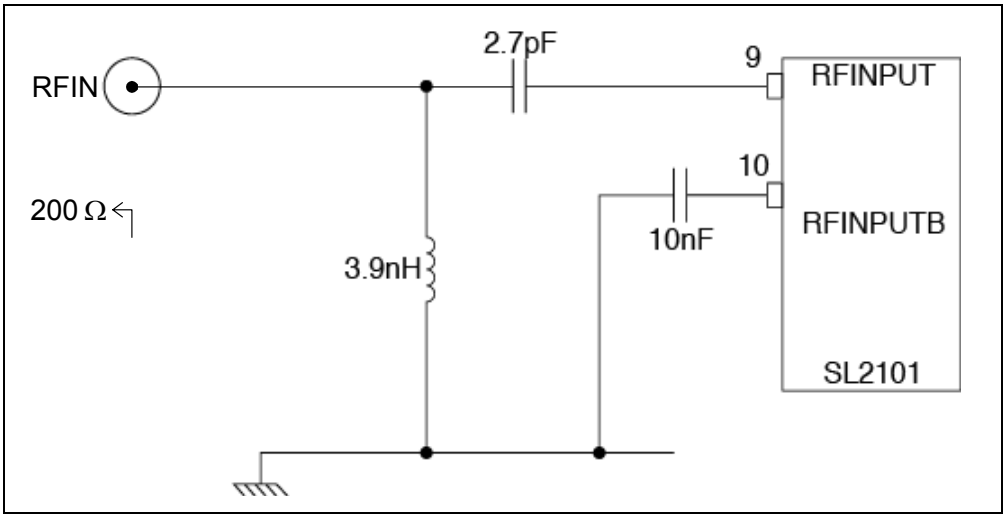


Figure 11 - RF Input Impedance Matching Network as 1.22 GHz Downconverter

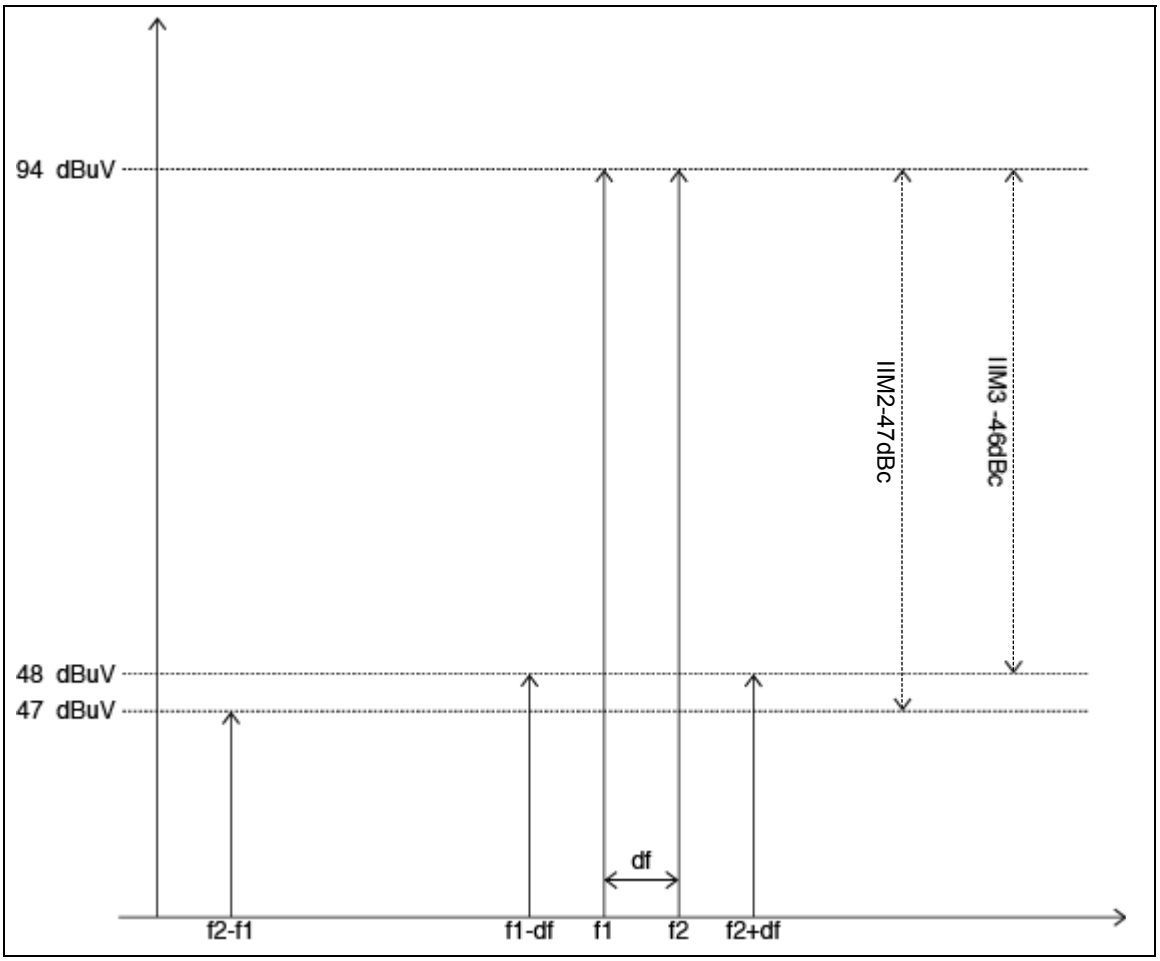


Figure 12 - Two Tone Intermodulation Test Condition Spectrum, Input Referred

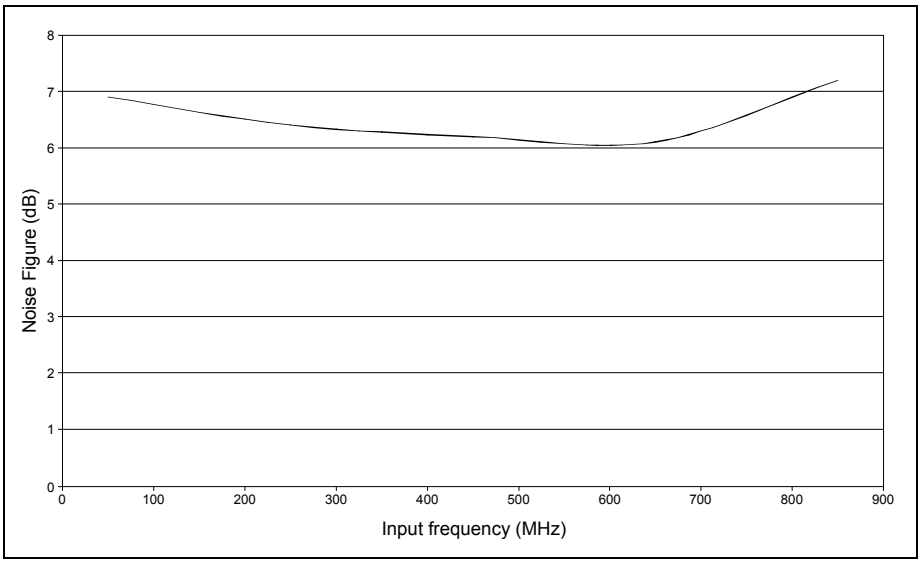


Figure 13 - Input NF, Typical (Maximum Power Setting)

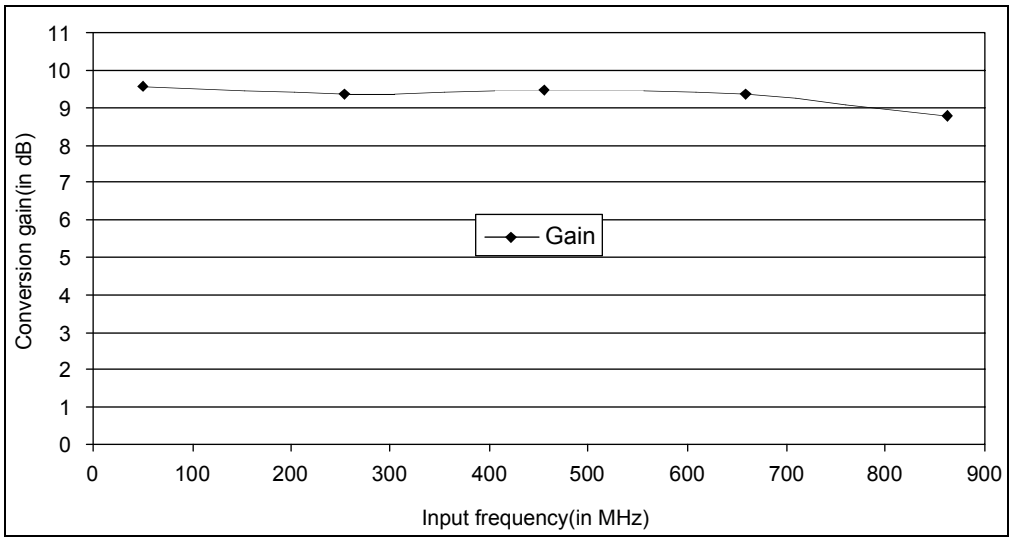


Figure 14 - Conversion Gain as Upconverter (Maximum Power Setting)

I2	I1	I0	Typ NF (dB)	Gain (dB)	typ CSO* (dBc)	typ CTB* (dBc)	typ IPIP2 (dBμV)	typ IPIP3 (dBμV)
0	0	0	6.8	10.1	-65	-65	144	121
0	0	1	6.0	9.1	-60	-54	141	114
0	1	0	5.8	7.6	-56	-42	132	108
0	1	1	6.5	5.4	-49	-35	129	106
1	0	0	8.7	10.4	-63	-60	146	117
1	0	1	6.2	10.0	-64	-56	142	113
1	1	0	5.9	8.3	-58	-42	133	106
1	1	1	6.4	5.8	-50	-34	126	103

Figure 15 - Upconverter Gain, NF and Intermodulation with Recommended Load Versus Power Setting

* Measured with 128 channels at +7 dBmV.

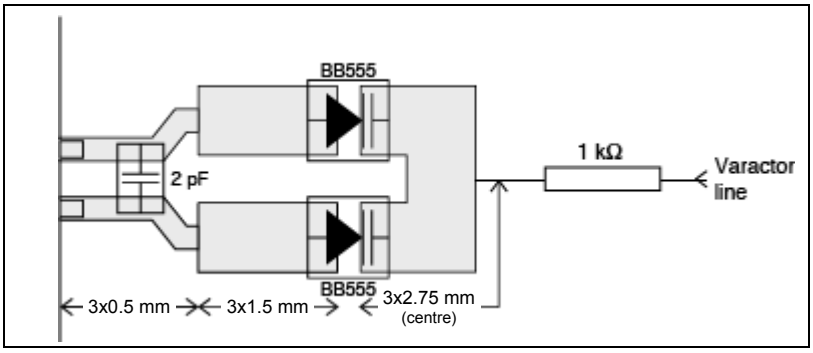


Figure 16 - Upconverter Oscillator Application

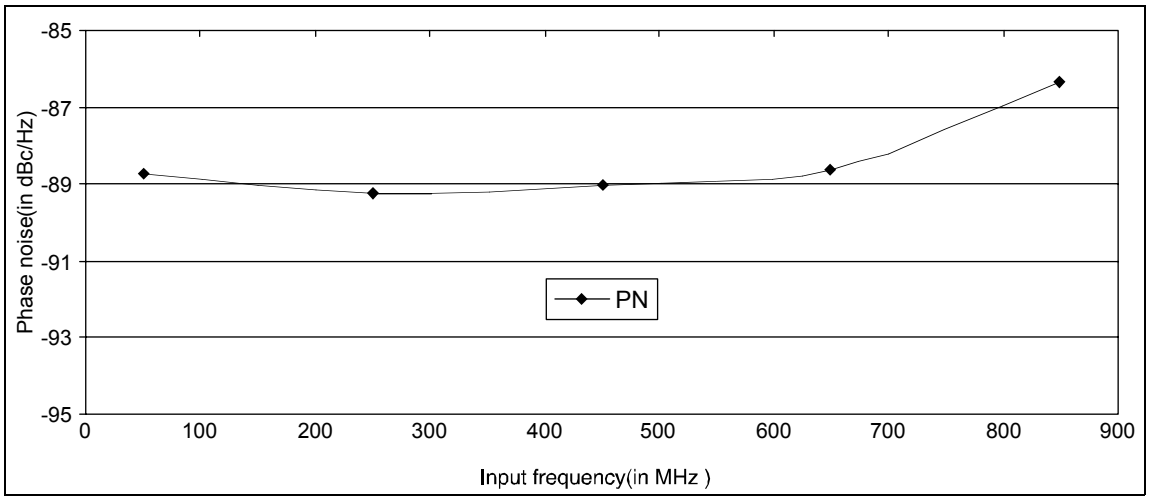


Figure 17 - Oscillator Typical Phase Noise Performance at 10 kHz Offset

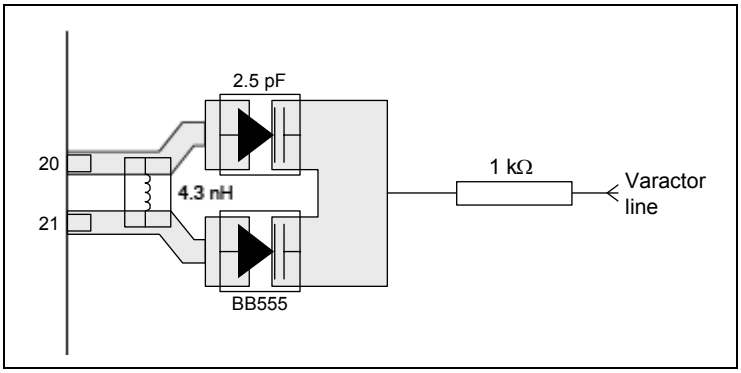


Figure 18 - Downconverter Oscillator Application

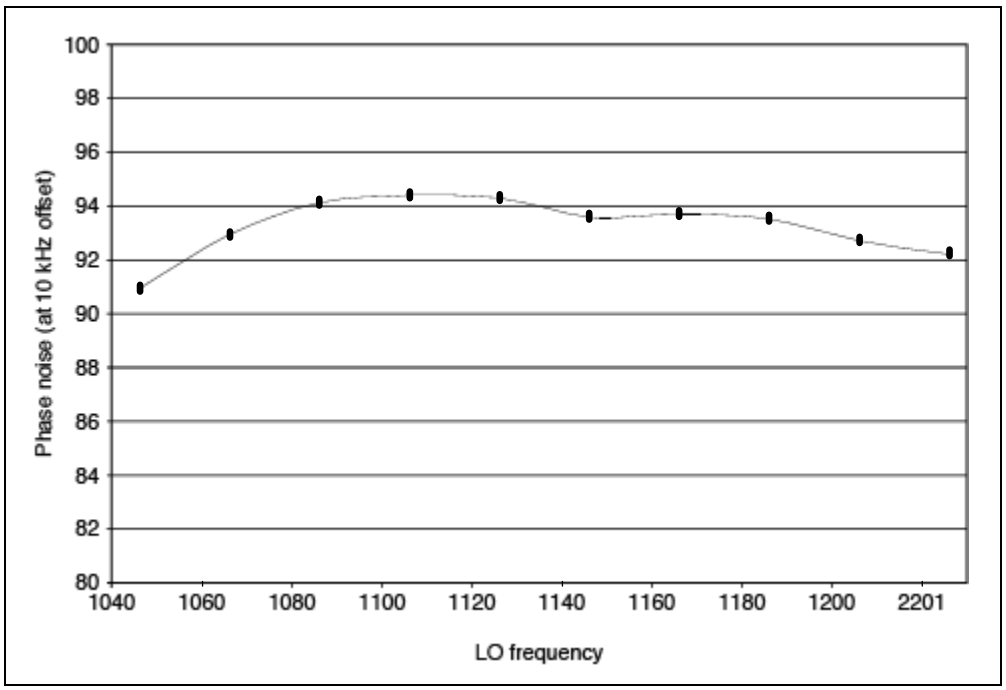


Figure 19 - Typical Phase Noise Performance as Downconverter at 10 kHz Offset

I2	I1	I0	Typ NF (dB)	Gain (dB)	typ IPIP3 (dBμV)
0	0	0	10.3	15.6	124
0	0	1	9.3	15.1	119
0	1	0	8.8	14.0	112
0	1	1	8.7	12.1	106
1	0	0	11.6	15.4	121.3
1	0	1	9.0	15.1	119.7
1	1	0	8.3	13.9	112.6
1	1	1	8.0	11.9	106.3

Figure 20 - Downconverter Gain, NF and IP3 with Recommended (Fig. 4) Load Versus Power Setting

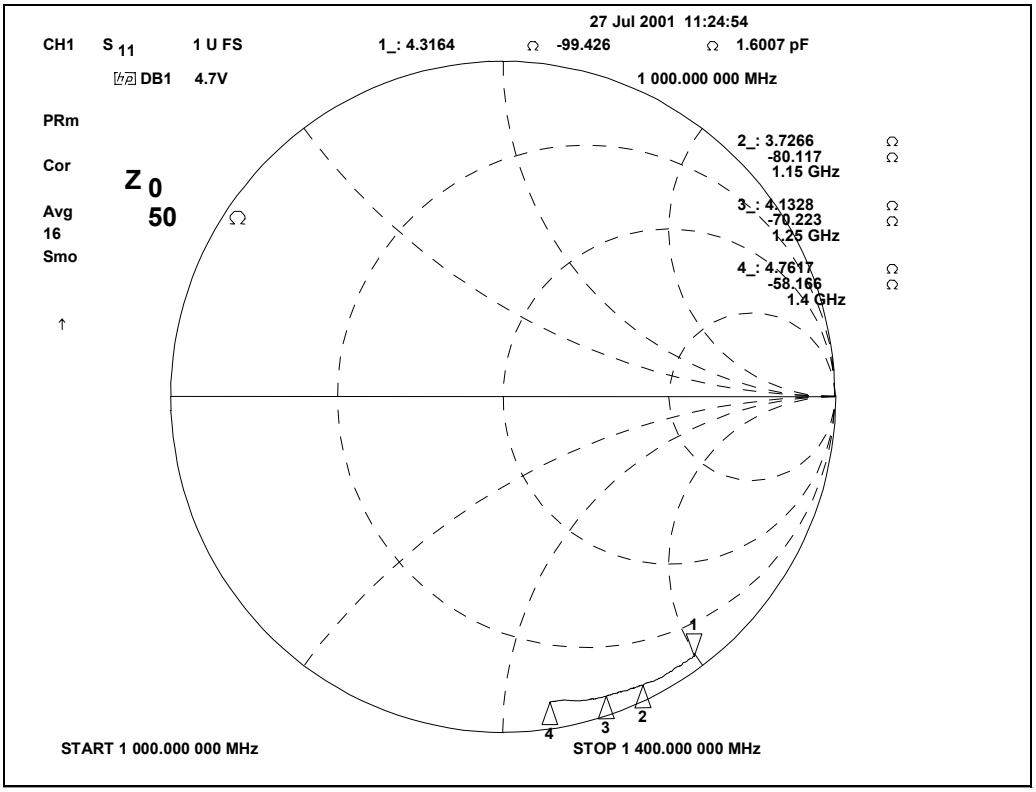


Figure 21 - Typical IF Output Impedance as Upconverter, Single-Ended

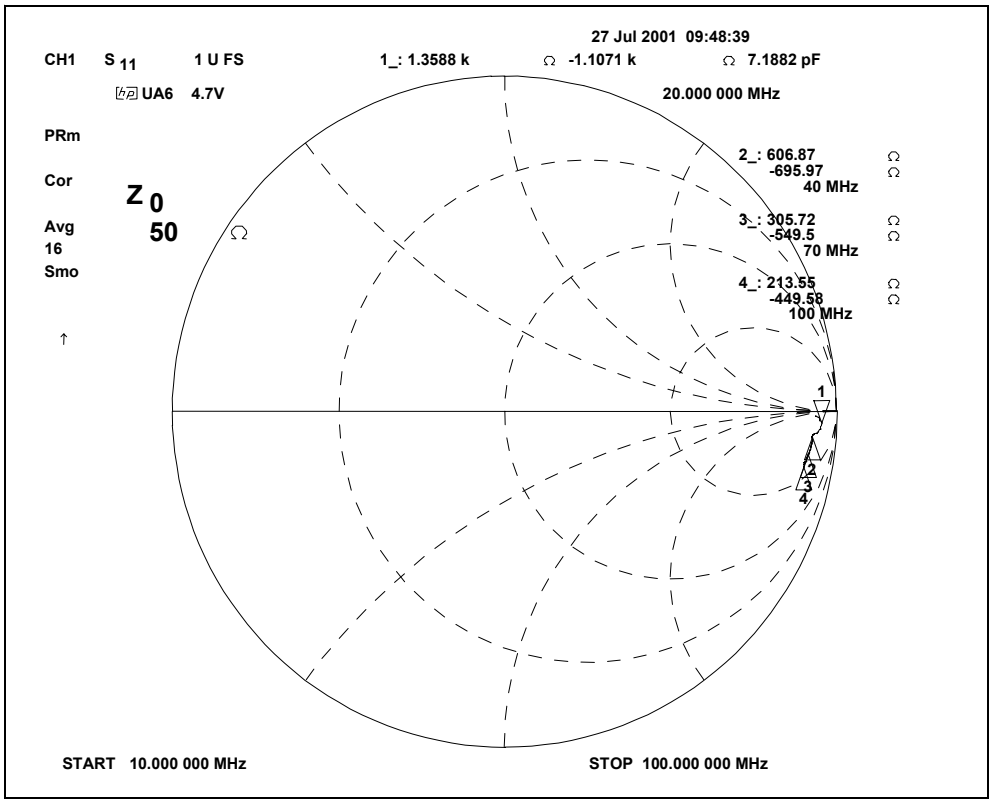


Figure 22 - Typical IF Output Impedance as Downconverter, Single-Ended

R4	R3	R2	R1	R0	Ratio
0	0	0	0	0	2
0	0	0	0	1	4
0	0	0	1	0	8
0	0	0	1	1	16
0	0	1	0	0	32
0	0	1	0	1	64
0	0	1	1	0	128
0	0	1	1	1	256
0	1	0	0	0	Illegal state
0	1	0	0	1	5
0	1	0	1	0	10
0	1	0	1	1	20
0	1	1	0	0	40
0	1	1	0	1	80
0	1	1	1	0	160
0	1	1	1	1	320

R4	R3	R2	R1	R0	Ratio
1	0	0	0	0	Illegal state
1	0	0	0	1	6
1	0	0	1	0	12
1	0	0	1	1	24
1	0	1	0	0	48
1	0	1	0	1	96
1	0	1	1	0	192
1	0	1	1	1	384
1	1	0	0	0	Illegal state
1	1	0	0	1	7
1	1	0	1	0	14
1	1	0	1	1	28
1	1	1	0	0	56
1	1	1	0	1	112
1	1	1	1	0	224
1	1	1	1	1	448

Figure 23 - Reference Division Ratios

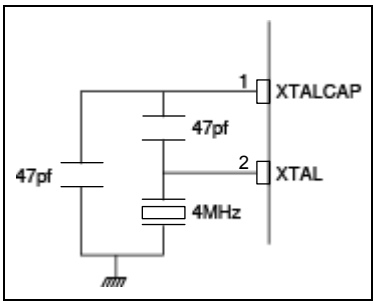


Figure 24 - Standard Application

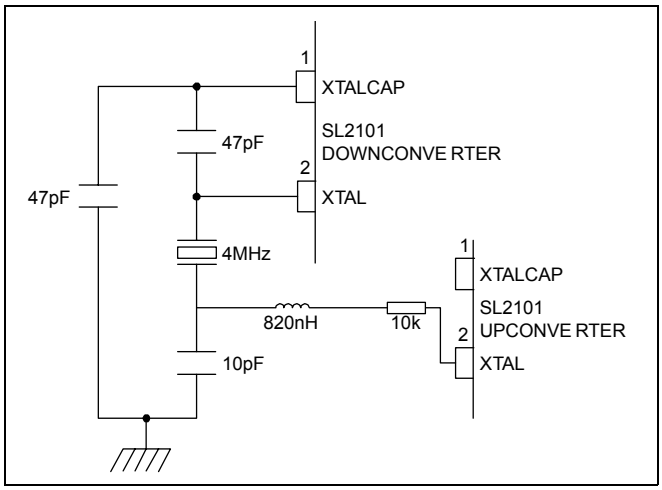


Figure 25 - Application When Driving Two SL2101 from One Crystal

T2	T1	T0	Test Mode Description
0	0	0	Normal operation
0	0	1	Charge pump sink * Status byte FL set to logic '0'
0	1	0	Charge pump source * Status byte FL set to logic '0'
0	1	1	Charge pump disabled * Status byte FL set to logic '1'
1	0	0	Normal operation and Port P0 = Fpd/2
1	0	1	Charge pump sink * Status byte FL set to logic '0' Port P0 = Fcomp
1	1	0	Charge pump source * Status byte FL set to logic '0' Port P0 = F_{comp}
1	1	1	Charge pump disabled * Status byte FL set to logic '1' Port P0 = F_{comp}

Figure 26 - Test Modes

* clocks need to be present on crystal and local oscillator to enable charge pump test modes and to toggle status byte bit FL.

RE	BUFREF output
0	disabled, high impedance
1	enabled

Note:The BUFREF output is only available on the SSOP package

Figure 27 - Buffered Crystal Reference Output Select

	MSB								LSB	
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Control data	1	C1	C0	R4	R3	R2	R1	R0	A	**Byte 4**
Control data	T2	T1	T0	I2	I1	I0	RE	P0	A	**Byte 5**

Table 1 - Write Data Format (MSB is transmitted first)

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Programmable divider	POR	FL	0	0	0	0	0	0	A	**Byte 2**

Table 2 - Read Data Format (MSB is transmitted first)

A : Acknowledge bit
MA1,MA0 : Variable address bits (see Table 3)
2^{14}-2^{0} : Programmable division ratio control bits
I2-I0 : Ina/mixer power select (see Figure 7)
C1-C0 : Charge pump current select (see Figure 29)
R4-R0 : Reference division ratio select (see Figure 23)
T2-T0 : Test mode control bits (see Figure 26)
RE : Buffered crystal reference output enable (see Figure 27
P0 : P0 port output state
POR : Power on reset indicator
FL : Phase lock flag

MA1	MA0	Address input voltage level
0	0	0-0.1Vcc
0	1	Open circuit
1	0	0.4Vcc – 0.6 Vcc #
1	1	0.9 Vcc - Vcc

Table 3 - Address Selection

Figure 28 - Read/Write Data Formats

C1	C0	Current in mA		
		Min.	Typ.	Max.
0	0	+-98	+-130	+-162
0	1	+-210	+-280	+-350
1	0	+-450	+-600	+-750
1	1	+-975	+-1300	+-1625

Figure 29 - Charge Pump Current

Electrical Characteristics - Test conditions (unless otherwise stated). T_{amb} = -40° to 85°C, Vee= 0V, Vcc=5 V+-5%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage at maximum power setting unless otherwise stated.

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Supply current	6, 12,17, 19, 22		90	120	mA	IF outputs will be connected to Vcc through the differential load as in Figures 4, 5 & 6. See Figure 7 for programmable settings.
Input frequency range	9, 10	50		1400	MHz	Operating condition only.
Output frequency range	14, 15	30		1400	MHz	Operating condition only.
Composite peak input signal	9, 10		97		dBμV	Operating condition only.
All synthesizer related spurs on IF Output	14, 15			-60	dBc	Within channel bandwidth of 8 MHz and with input power of 60 dBμV.
Upconverter application						
Input frequency range	9, 10	50		860	MHz	
Input impedance			75		Ω	See Figure 8.
Input return loss		6			dB	With input matching network as in Figure 9.
Input Noise Figure				9.5	dB	Tamb=27°C, see Figure 13, with input matching network as in Figure 9. See Figure 15 for programmable settings.
Conversion gain			9		dB	Differential voltage gain to 200 Ω load on output of SAWF as in Figure 4, see Figure 14. See Figure 15 for programmable settings.

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Gain variation across operation range		-1		+1	dB	50-860 MHz
Gain variation within channel				0.5	dB	Channel bandwidth 8 MHz within operating frequency range.
Through gain				-20	dB	45-1400 MHz
CSO			-65		dBc	Measured with 128 channels at 62 dBμV. See Figure 15 for programmable settings.
CTB			-68		dBc	Measured with 128 channels at 62 dBμV. See Figure 15 for programmable settings.
$IPIP2_{2T}$		141			dBuV	See Note 2. See Figure 15 for programmable settings.
$IPIP3_{2T}$		117			dBuV	See Note 2. See Figure 15 for programmable settings.
$IPIM2_{2T}$				-47	dBc	See Note 2. See Figure 12.
$IPIM3_{2T}$				-46	dBc	See Note 2. See Figure 12.
LO operating range		1		2.3	GHz	Maximum tuning range 0.9 GHz determined by application.
LO phase noise, SSB @ 10 kHz offset @ 100 kHz offset			 -86 -106		 dBc/Hz dBc/Hz	Application as in Figure 16. See Figure 17.
LO phase noise floor				-136	dBc/Hz	Application as in Figure 16.
IF output frequency range	14, 15	1		1.4	GHz	
IF output impedance						See Figure 21.
Downconverter application						
Input frequency range	9, 10	1000		1400	MHz	
Input impedance			75		Ω	See Figure 10.
Input return loss		12			dB	With input matching network as in Figure 11.
Input Noise Figure				14	dB	Tamb=27°C, with input matching network as in Figure 11. See Figure 20 for programmable settings.

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Conversion gain			12		dB	Differential voltage gain to 50 Ω load on output of impedance transformer as in Figure 6. See Figure 20 for programmable settings.
Gain variation within channel				0.5	dB	Channel bandwidth 8 MHz within operating frequency range.
Through gain				-20	dB	45-1400 MHz
$IPIP3_{2T}$		117			dBμV	See Note 2.
$IPIM3_{2T}$				-46	dBc	See Note 2. See Figure 12.
LO operating range		1		2.3	GHz	Maximum tuning range determined by application, see Note 4.
LO phase noise, SSB @ 10 kHz offset @ 100 kHz offset			 -92 -112		 dBc/Hz dBc/Hz	Application as in Figure 18. See Figure 19.
LO phase noise floor				-136	dBc/Hz	Application as in Figure 18.
IF output frequency range	14, 15			100	MHz	
IF output impedance						See Figure 22.
Synthesizer						
SDA, SCL	3, 4					
Input high voltage		3		5.5	V	I^2C 'Fast mode' compliant
Input low voltage		0		1.5	V	
Input high current				10	μA	Input voltage = Vcc
Input low current		-10			μA	Input voltage = Vee
Leakage current				10	μA	Vcc=Vee
Hysterysis			0.4			
SDA output voltage	3			0.4 0.6	V V	Isink = 3 mA Isink = 6 mA
SCL clock rate	4			400	kHz	
Charge pump output current	28					See Figure 29. Vpin = 2 V
Charge pump output leakage	28		+-3	+-10	nA	Vpin = 2 V

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Charge pump drive output current	27	0.5			mA	Vpin = 0.7 V
Crystal frequency	1,2	2		20	MHz	See Figure24 and Figure 25 for application.
Recommended crystal series resistance		10		200	Ω	4 MHz parallel resonant crystal
External reference input frequency	2	2		20	MHz	Sinewave coupled through 10 nF blocking capacitor
External reference drive level	2	0.2		0.5	Vpp	Compatible with BUFREF output. (SSOP package only)
Phase detector comparison frequency				4	MHz	
Equivalent phase noise at phase detector						SSB, within loop bandwidth
			-148		dBc/Hz	F_{comp} = 1 MHz
			-152		dBc/Hz	F_{comp} = 250 kHz
			-158		dBc/Hz	F_{comp} = 62.5 kHz
Local oscillator programmable divider division ratio		240		32767		
Reference division ratio						See Figure 23.
Output port sink current leakage current	26	 2		 10	 mA μA	See Note 3. Vport = 0.7 V Vport =Vcc
BUFREF output output amplitude output impedance	5		 0.35 250		 Vpp Ω	AC coupled. Note 5. Enabled by bit RE=1 and default state on power-up. BUFREF output only available on SSOP package
Address select Input high current Input low current				 1 -0.5	 mA mA	See Figure 28, Table 3 Vin=Vcc Vin=Vee

Note 1: All power levels are referred to 75 Ω and 0 dBm = 109 dBμV

Note 2: Any two tones within RF operating range at 94 dBμV beating within band, with output load as in Figure 4

Note 3: Port powers up in high impedance state

Note 4: To maximise phase noise the tuning range should be minimised and Q of resonator maximised. The application as in Figure 18 has a tuning range of 200 MHz.

Note 5: If the BUFREF output is not used it should be left open circuit or connected to Vccd and disabled by setting RE = '0'.

Absolute Maximum Ratings - All voltages are referred to Vee at 0 V (pins 7, 8, 11, 13, 16, 18, 23, 25).

Characteristic	Pin	Min.	Max.	Units	Conditions
Supply voltage, V_{cc}	6, 12, 17, 19, 22	-0.3	6	V	
RF input voltage	9, 10		117	dBuV	Differential, AC coupled inputs
All I/O port DC offsets		-0.3	Vcc+0.3	V	
SDA, SCL DC offsets	3, 4	-0.3	6	V	Vcc = Vee to 5.25 V
Storage temperature		-55	150	°C	
Junction temperature			125	°C	Power applied.
Package thermal resistance, chip to case (SSOP)			20	°C/W	
Package thermal resistance, chip to ambient (SSOP)			85	°C/W	
Power consumption at 5.25 V			630	mW	Maximum power setting.
ESD protection (pins 3-28)		1		kV	Mil-std 883B method 3015 cat1
ESD protections (pins 1, 2)		0.75		kV	

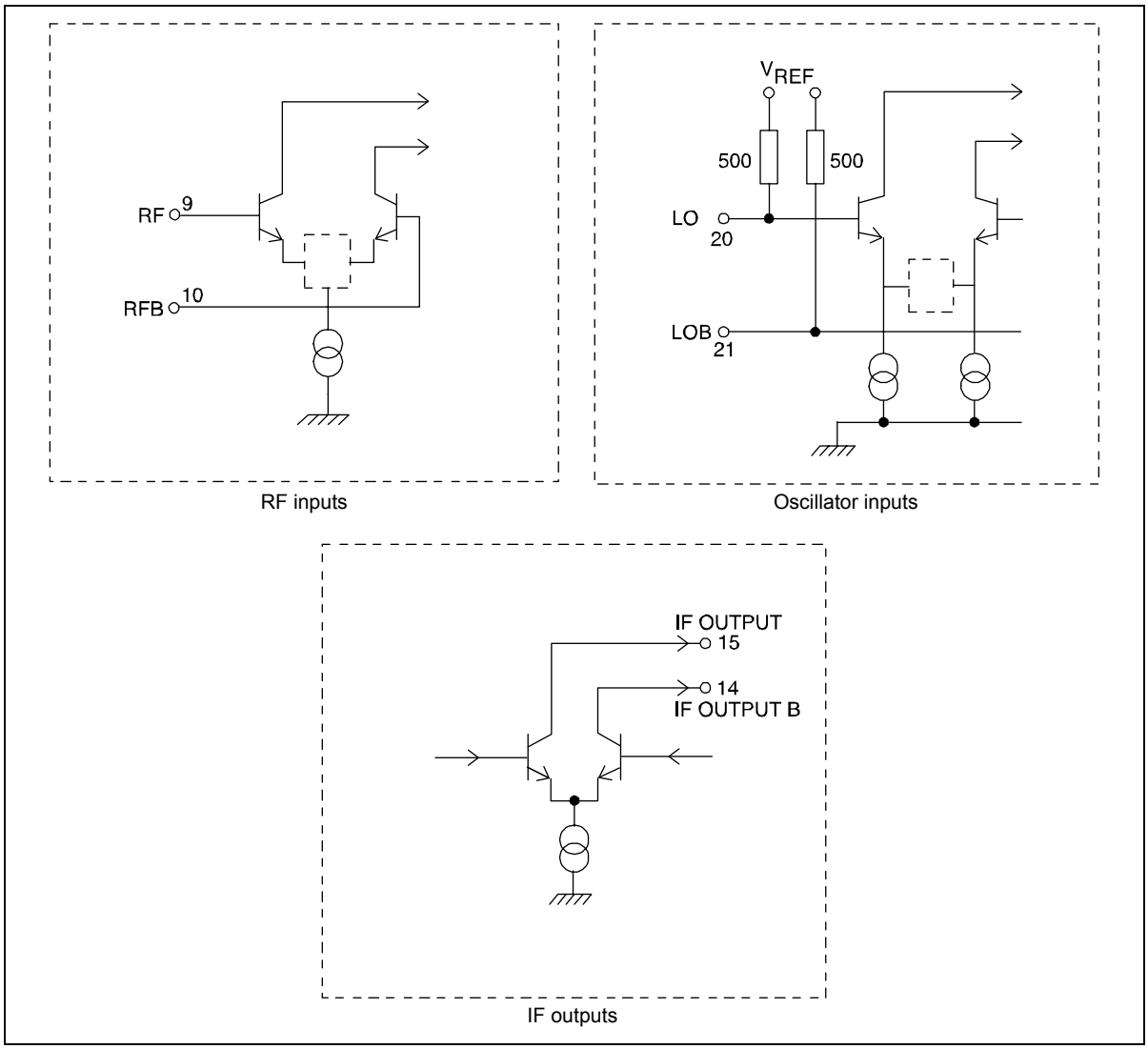


Figure 30 - Input and Output Interface Circuits (RF section)

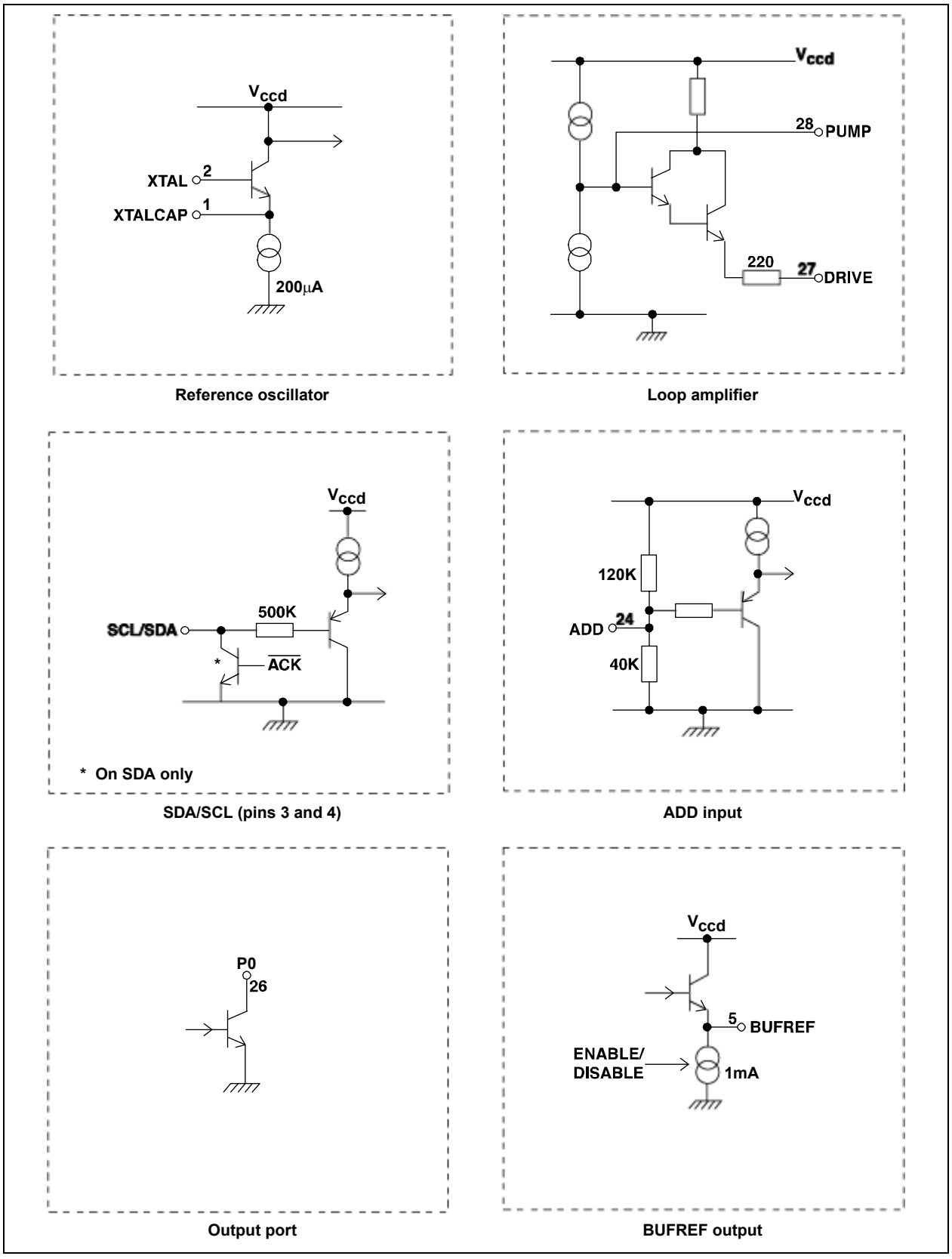
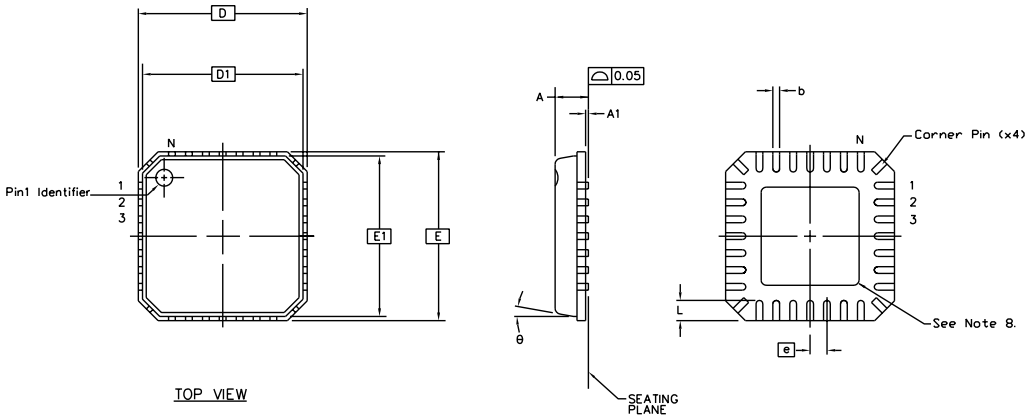


Figure 31 - Input and Output Interface Circuits (PLL section)



SYMBOL	COMMON DIMENSIONS	
	MIN.	MAX.
A	–	1.00
A1	0.00	0.05
b	0.18	0.30
D	5.00 BSC	
D1	4.75 BSC	
E	5.00 BSC	
E1	4.75 BSC	
N	28	
Nd	7	
Ne	7	
e	0.50 BSC	
L	0.50	0.75
θ	0°	12°

Conforms to JEDEC MO-220 WHHD-1 iss A

NOTES:
1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd & Ne ARE THE NUMBER OF TERMINALS IN X & Y DIRECTION RESPECTIVELY.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.25mm FROM TERMINAL.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. LEAD COUNT IS 28 PLUS 4 CORNER LEADS.
6. PACKAGE WARPAGE MAX 0.05mm.
7. NOT TO SCALE.
8. DIMENSION OF THE EXPOSED METAL PAD MAY BE UPTO 0.20MM SMALLER THAN THE NOMINAL DIE PAD DIMENSION – SEE LEADFRAME DRAWING FOR SPECIFIC PADDLE DIMENSION.

ISSUE	2	3	4	5
ACN	208382	208538	212490	CDCA
DATE	17Feb00	16Mar00	8Apr02	17Dec03
APPRD.				

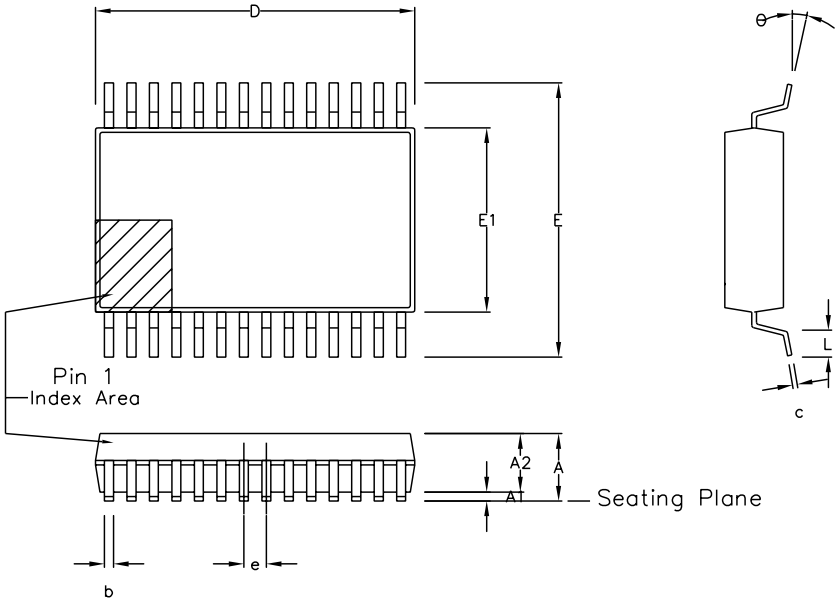
ZARLINK SEMICONDUCTOR

Package Code LD

Previous package codes
LH

Package Outline for Stamped 28 (+4) Lead QFN (5x5mm)

GPD00632



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	9.90		10.50		0.390		0.413
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	28						
Conforms to JEDEC MO-150 AH Iss. B							

This drawing supersedes:-
418/ED/51481/004 (Swindon/Plymouth)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protusion. Mould flash or protusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

ISSUE	1	2	3	
ACN	201935	205232	212478	
DATE	27Feb97	25Sep98	3Apr02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
NP / N

Package Code DD

Package Outline for 28 lead SSOP (5.3mm Body Width)

GPD00296

For more information about all Zarlink products visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE