Ordering number : EN5913

CMOS IC

LC75281E

Parametric Equalizer System

Overview

The LC75281E is a four-band stereo parametric equalizer. A parametric equalizer is a fully general equalizer that allows all three parameters that define an equalizer's characteristics, i.e., the center frequency, gain, and Q, to be set independently.

Functions

- Four-band (low, low mid, high mid, and high) left and right channels parametric equalizer
- For each band:
  Center frequency: 11 positions
  Gain: 13 positions in ±2dB steps
  Q: Variable over 8 positions
- The center frequency, gain, and Q control settings are set using serial data input in the CCB format.

Features

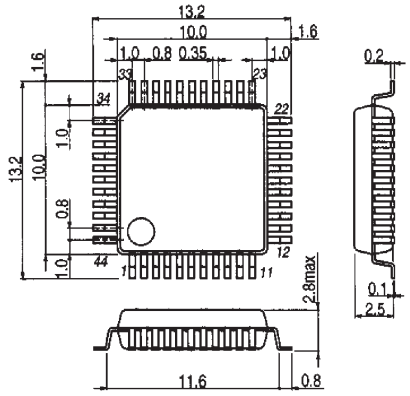
- A parametric equalizer with the following features can be implemented with just two ICs: this IC and a microcontroller.
- The center frequency, gain, and Q can be controlled by a single operation.
- Memory recall by a single operation can be implemented using preset values.
- Either shelving or peaking characteristics can be selected for the low band.

Package Dimensions

unit: mm

3159-QFP64E

[LC75281E]

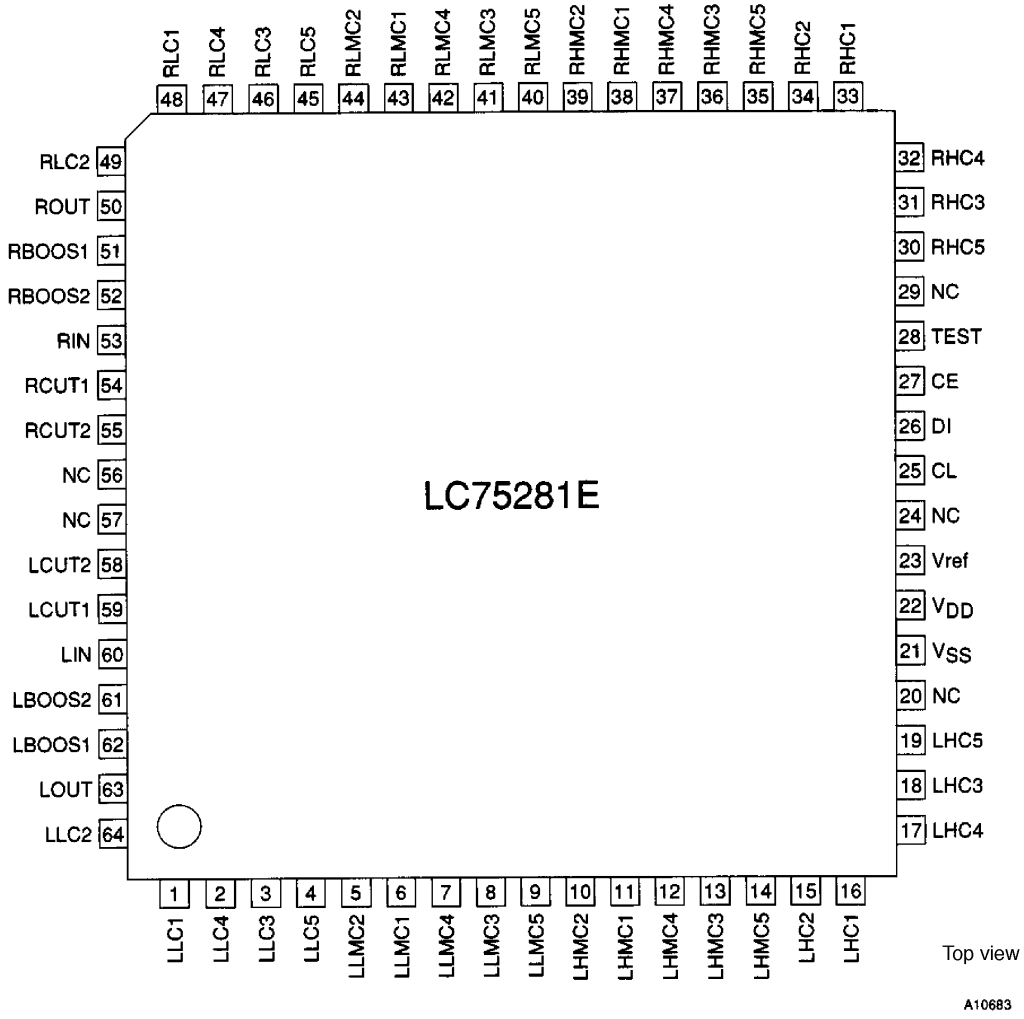


SANYO: QFP64E (QIP64E)

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Pin Assignment



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		10.5	V
Maximum input voltage	V_{IN}1 max	LIN, RIN	0 to V_{DD}	V
	V_{IN}2 max	CL, CE, DI	0 to V_{DD}	V
Allowable power dissipation	Pd max	Ta ≤ 85°C	300	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		6.0		9.0	V
High-level input voltage	V_{IH}	CL, CE, DI	4.0		V_{DD}	V
Low-level input voltage	V_{IL}	CL, CE, DI	V_{SS}		1.0	V
Input voltage range	V_{IN}	LIN, RIN	0		V_{DD}	V
Load resistance	R_L	LOUT, ROUT, MIXOUT	1			kΩ
Input pulse width	tøw	CL	1			µs
Setup time	tsetup	CL, CE, DI	1			µs
Hold time	thold	CL, CE, DI	1			µs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, f = 1 kHz, V_{DD} = 8 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{DD}	V_{DD}		36	50	mA
Output voltage	V_O	LOUT, ROUT: THD = 1%		2.2		Vrms
Total harmonic distortion	THD1	LOUT, ROUT: Vo = Flat, V_{IN} = 0 dBV		0.005	0.01	%
	THD2	LOUT, ROUT: Vo = Boost, All bands +2 dB, V_{IN} = –15 dBV		0.1	1	%
Output noise voltage	V_N1	LOUT, ROUT: Vo = Flat, Rg = 1 kΩ, IHF-A filters		7	15	µs
	V_N2	LOUT, ROUT: Vo = Flat, Rg = 1 kΩ, DIN filters		13		µs
	V_N3	LOUT, ROUT, Rg = 1 kΩ, f0 = f1, Q = Q1 IHF-A filter, all bands at full boost, with the external constants the same as those for the center frequency (example 1)		58		µs
	V_N4	LOUT, ROUT, Rg = 1 kΩ, f0 = f1, Q = Q1 IHF-A filters, all bands at full cut, with the external constants the same as those for the center frequency (example 1)		23		µs
Crosstalk between inputs	CT	V_{IN} = 1 Vrms, f = 1 kHz	60	80		dB
High-level input current	I_{IH}	CL, DI, CE, V_{IN} = 9 V			1	µA
Low-level input current	I_{IL}	CL, DI, CE, V_{IN} = 0 V	–1			µA
DC variation	V_{DC}	All bands G = +12 dB, Q: Setting switched from Q1 to Q2 With the external constants the same as those for the center frequency (example 1) shown on page 7.	–10		+10	mV

Pin Functions

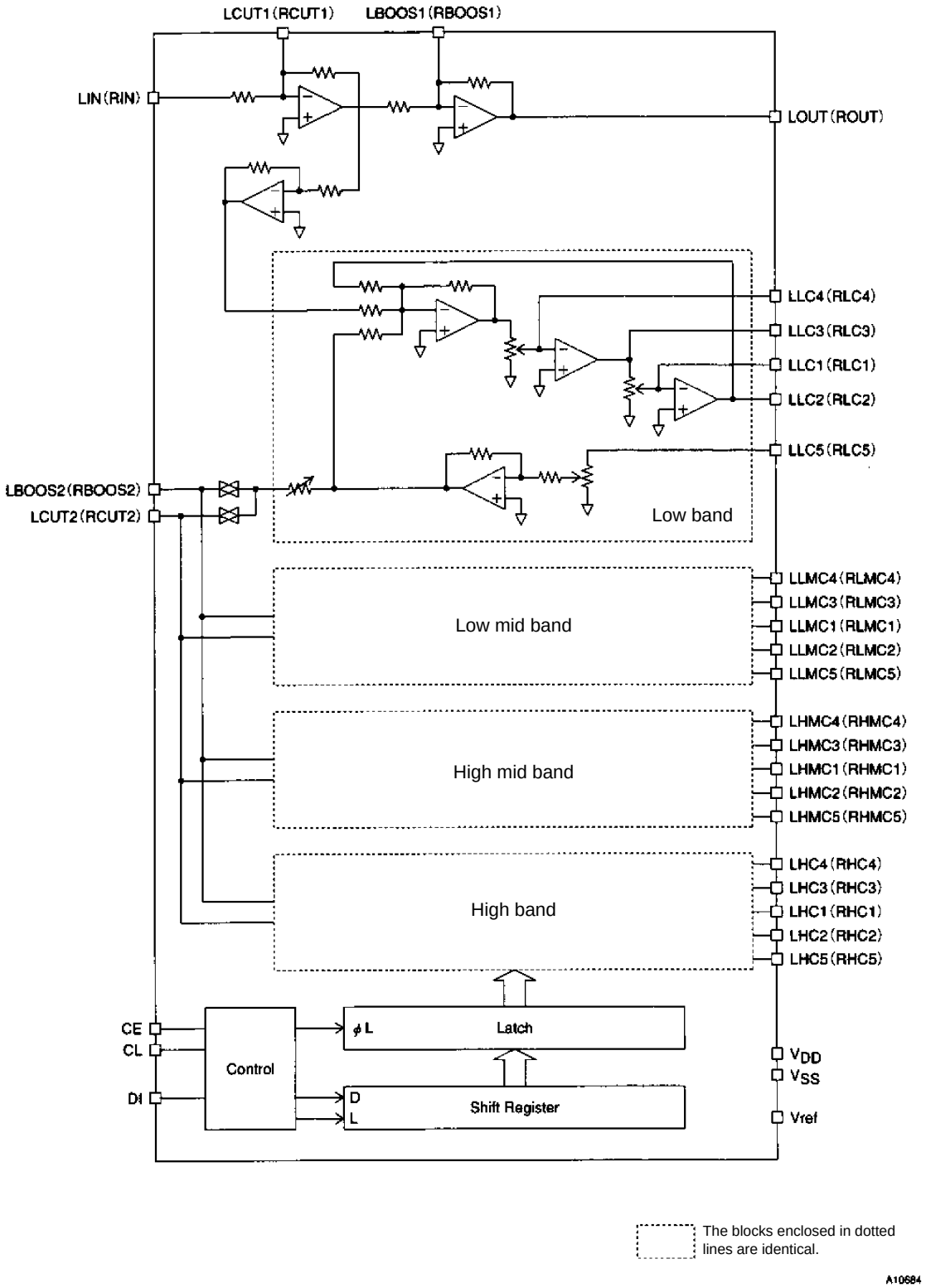
Pin No.	Pin	Function
64 1 2 3 4	LLC2 LLC1 LLC4 LLC3 LLC5	Left channel low band control block. External capacitor connections.
5 6 7 8	LLMC2 LLMC1 LLMC4 LLMC3	Left channel low mid band control block. External capacitor connections.

Continued on next page.

Continued from preceding page.

Pin No.	Pin	Function
10 11 12 13 14	LHMC2 LHMC1 LHMC4 LHMC3 LHMC5	Left channel high mid band control block. External capacitor connections.
15 16 17 18 19	LHC2 LHC1 LHC4 LHC3 LHC5	Left channel high band control block. External capacitor connections.
20, 24, 29 56, 57	NC	Unused pins. These pins must be either left open or connected to V_{SS}.
23	Vref	Internal operational amplifier reference voltage generator outputs. Several capacitors with values of about 10 µF must be connected with this pin to reduce ripple.
21 22	V_{SS} V_{DD}	Power supply. These pins must be connected to the stipulated power supply.
27	CE	Chip enable input. Data is written to the internal latch and the analog switches operate when this pin changes from high to low. Data transfer is enabled when this pin is high.
26 25	DI CL	Serial data and clock inputs for IC control
49 48 47 46 45	RLC2 RLC1 RLC4 RLC3 RLC5	Right channel low band control block. External capacitor connections.
44 43 42 41 40	RLMC2 RLMC1 RLMC4 RLMC3 RLMC5	Right channel low mid band control block. External capacitor connections.
39 38 37 36 35	RHMC2 RHMC1 RHMC4 RHMC3 RHMC5	Right channel high mid band control block. External capacitor connections.
34 33 32 31 30	RHC2 RHC1 RHC4 RHC3 RHC5	Right channel high band control block. External capacitor connections.
58 59 61 62	LCUT2 LCUT1 LBOOS2 LBOOS1	Internal filter DC offset voltage exclusion capacitor connections. Capacitors of about 10 µF must be connected between pins 61 and 62, and between pins 63 and 64. (These are for the left channel block.)
55 54 52 51	RCUT2 RCUT1 RBOOS2 RBOOS1	Internal filter DC offset voltage exclusion capacitor connections. Capacitors of about 10 µF must be connected between pins 51 and 52, and between pins 49 and 50. (These are for the right channel block.)
60	LIN	Left channel audio signal input (Must be driven with a low load capacitance.)
53	RIN	Right channel audio signal input (Must be driven with a low load capacitance.)
63	LOUT	Left channel audio signal output (Must be received with a low load capacitance.)
50	ROUT	Right channel audio signal output (Must be received with a low load capacitance.)
28	TEST	IC test pin. This pin must be left open when not used for IC test.

Block Diagram



• Center frequency (fo)

Band	f1	f2	f3	f4	f5	f6	f7	f8	f9	f10	f11	External capacitor (μF)
Low	31.5	40	50	63	80	100	125	160	200	250	315	0.047
Low mid	160	200	250	315	400	500	630	800	1 k	1.25 k	1.6 k	0.0094
High mid	630	800	1 k	1.25 k	1.6 k	2 k	2.5 k	3.15 k	4 k	5 k	6.3 k	0.00235
High	1.6 k	2 k	2.5 k	3.15 k	4 k	5 k	6.3 k	8 k	10 k	12.5 k	16 k	0.0094

External capacitor calculations

Figure a shows the LC75281E internal f0 control circuit. The center frequency f0 can be set to one of 11 frequencies in 1/3 octave steps by switching the resistors in the figure.

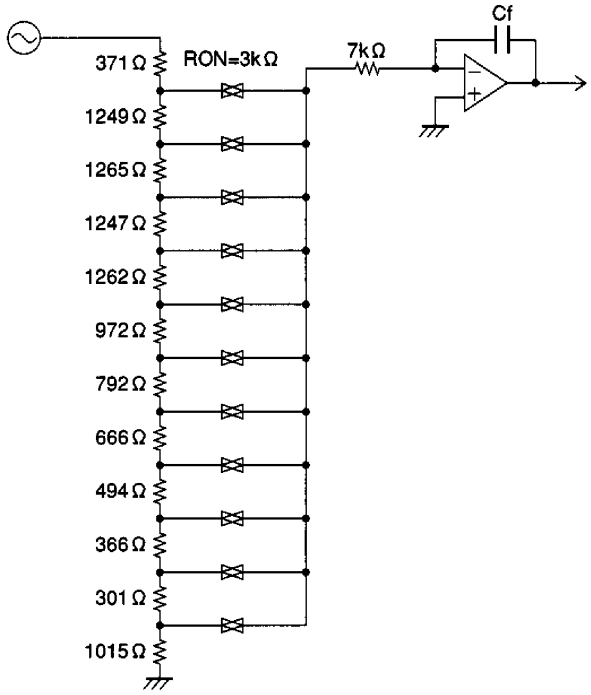
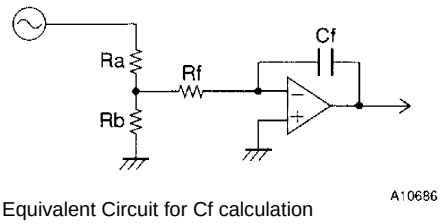


Figure a

The value of the external capacitor C is determined by substituting the desired center frequency in the following formula.

$$Cf = \frac{1}{2\pi\ Rf\ fo\ max} \cdot \frac{Rb//Rf}{Ra + (Rb//Rf)}$$

fo max: Corresponds to 315 Hz in the low band row in the preceding table.



Equivalent Circuit for Cf calculation

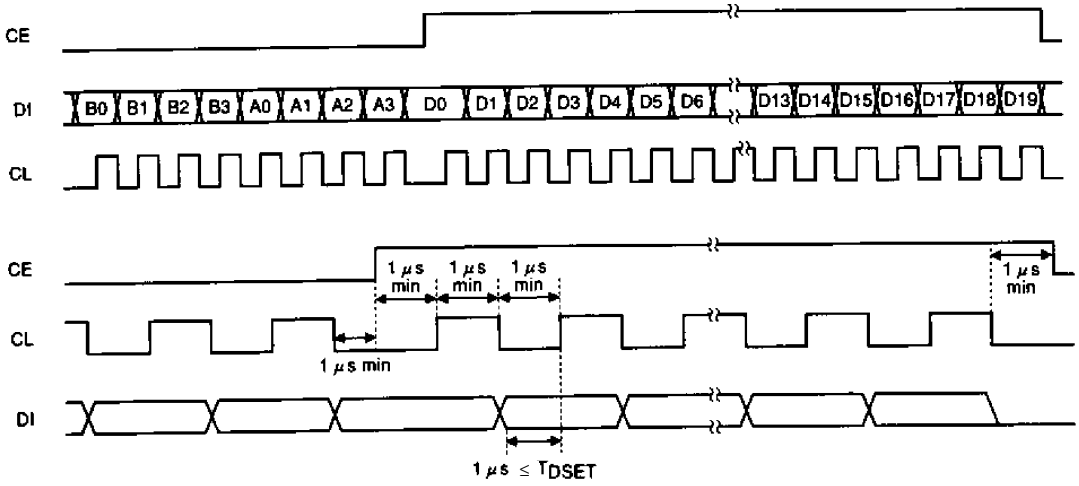
• Gain: 13 positions in 2-dB steps

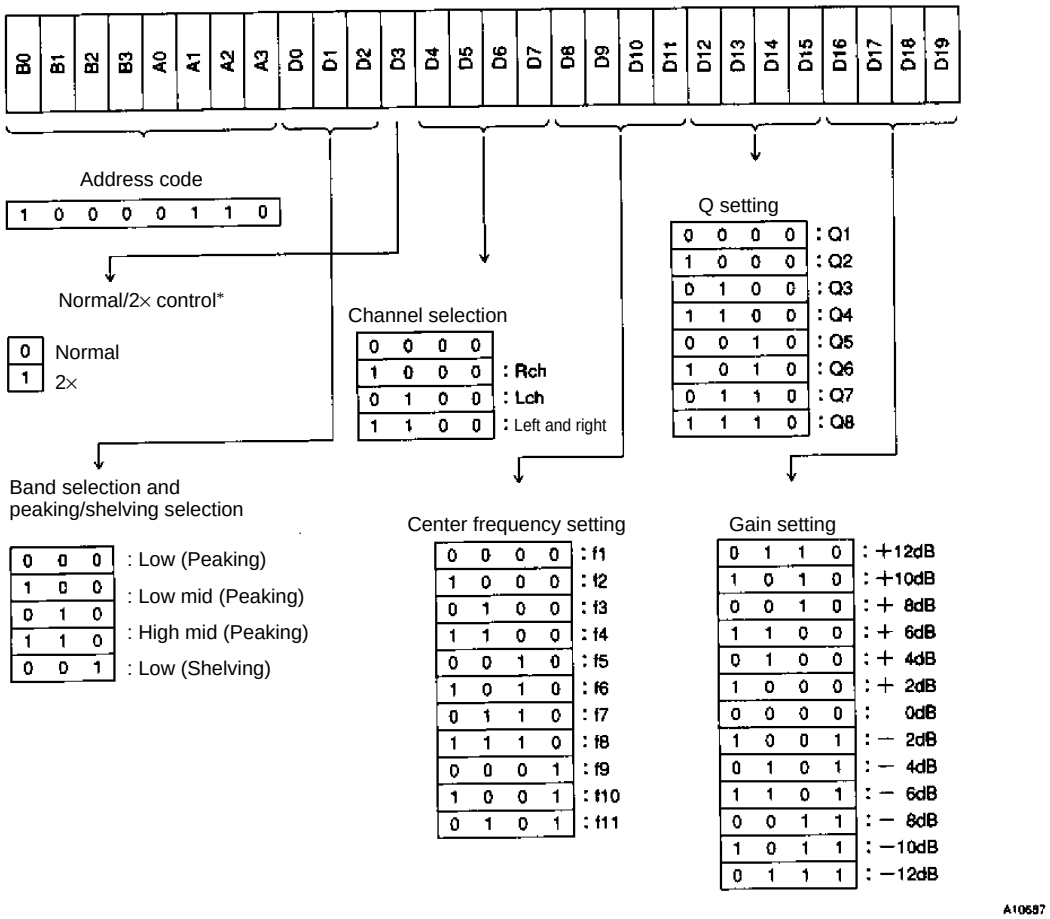
• Q

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
Q	0.404	0.667	1.41	2.15	2.87	4.32	5.76	8.65
OCT	3	2	1	2/3	1/2	1/3	1/4	1/6

Data Input Procedure

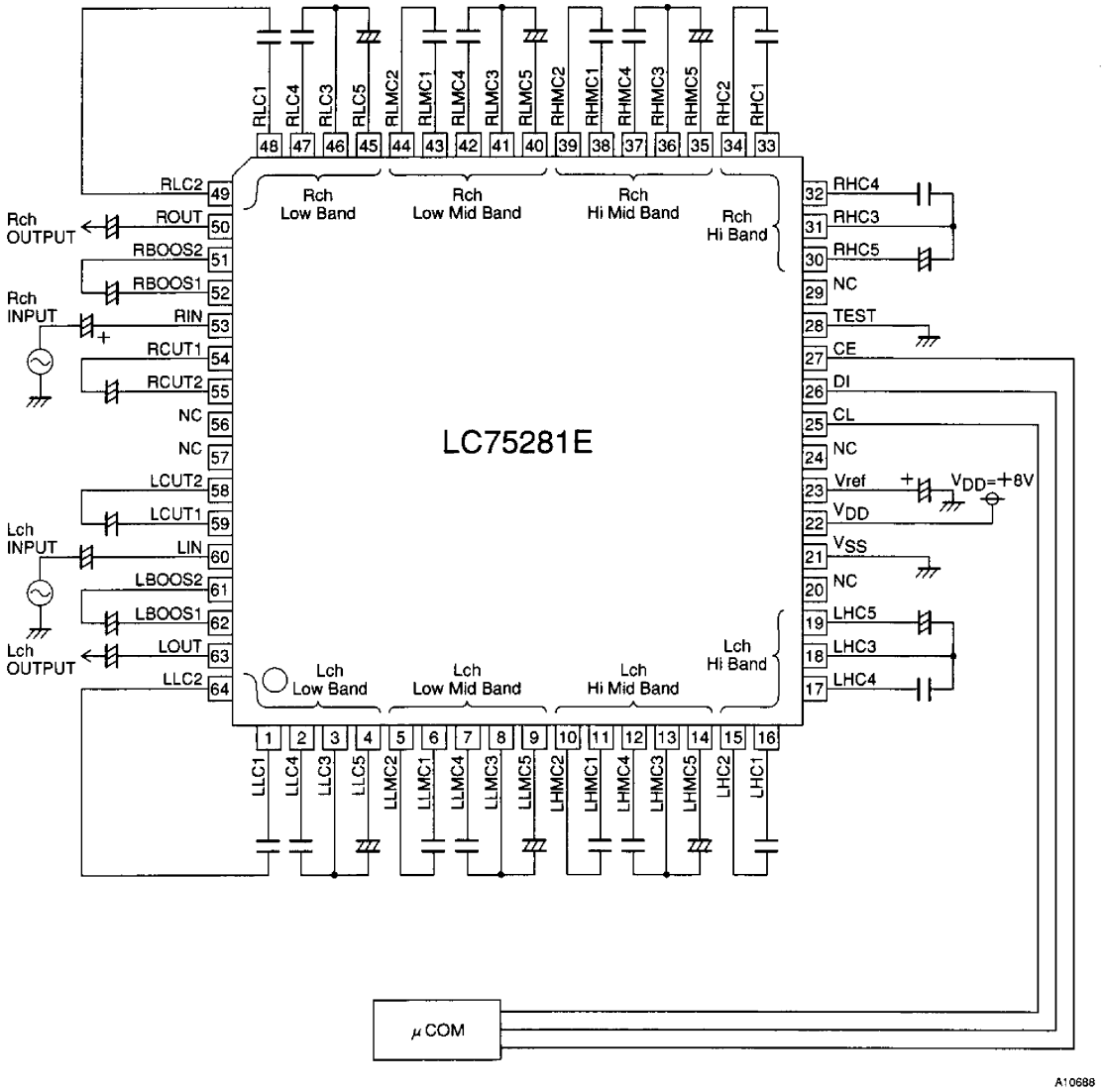
The LC75281E is controlled by inputting the stipulated serial data to the CE, CL, and DI pins. The data consists of 28 bits, of which 8 bits are the address and 20 bits are the data.



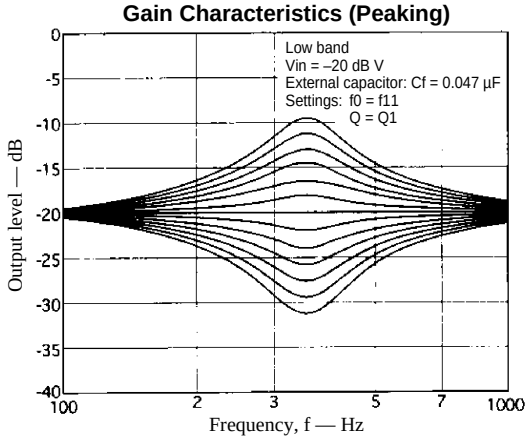


Note *: The 2× command doubles the center frequency of all bands. When setting this bit to 1, applications must either enter the band data for one of the bands in bits D1 to D19, or must set both bits D4 and D5 to 0, in which case all other bits are ignored.

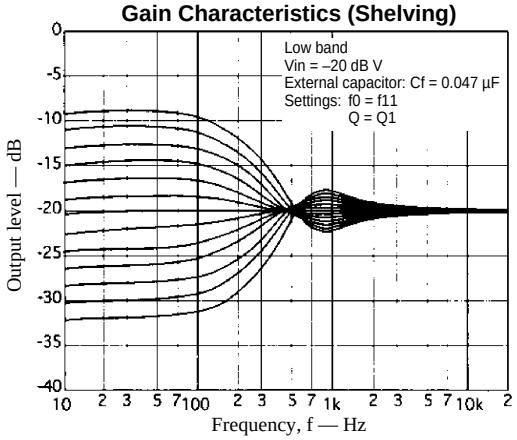
Sample Application Circuit



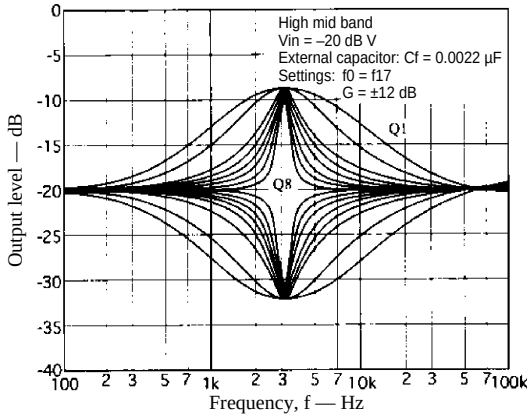
Gain Characteristics (Peaking)



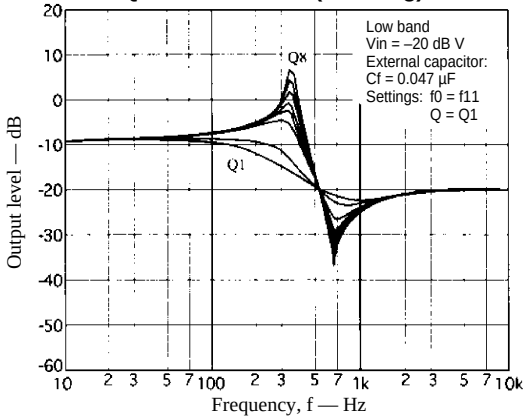
Gain Characteristics (Shelving)



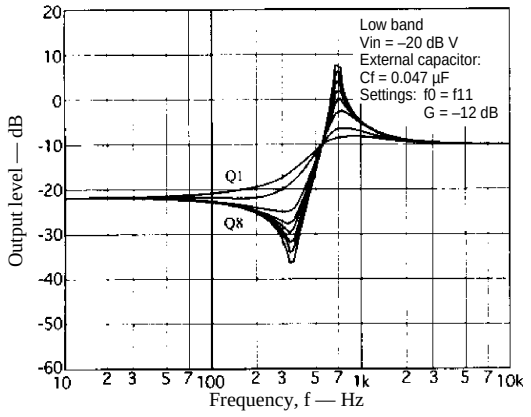
Q Characteristics (Peaking)



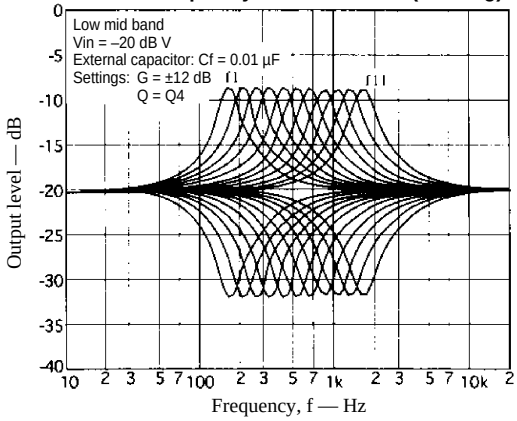
Q Characteristics (Shelving) - 1



Q Characteristics (Shelving) - 2



Center Frequency Characteristics (Peaking)



Center Frequency Characteristics (Shelving)