



# LC75366, 75366M

## Two-Channel Electronic Volume Control



### Overview

The LC75366 (DIP20) and the LC75366M (MFP20) are electronic volume controls that can be controlled by serial input data and provide volume, balance and loudness functions.

### Features

- Silicon gate CMOS process for low switching noise

### Functions

- Volume: 0 dB to -68 dB (in 2 dB steps) and  $-\infty$ ; 36 positions.

A balance function can be implemented by controlling the left and right channel volume settings independently.

- Loudness: Taps are provided at the -20 dB positions in the 10 dB step resistor ladder used by the volume control function. A loudness function can be implemented by attaching external RC circuits at these tap points.
- An address selection pin (the S pin) allows two LC75366 chips to be used on the same bus.
- Serial data input: Supports CCB\* format communication with the system controller.

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

### Specifications

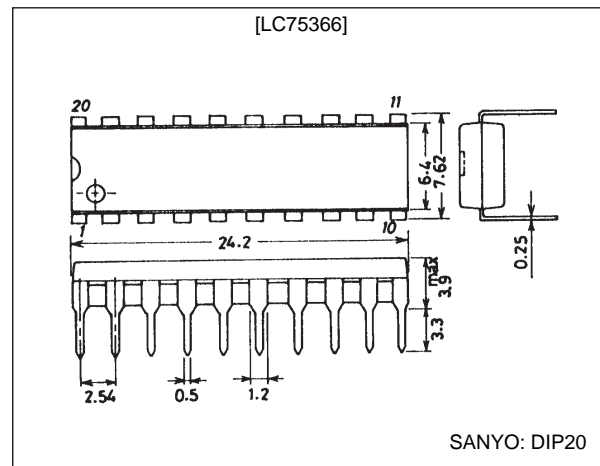
**Absolute Maximum Ratings at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\ max}$	$V_{DD}$	12	V
Maximum input voltage	$V_{IN\ max1}$	CL, DI, CE, S	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
	$V_{IN\ max2}$	L10dBIN, L2dBIN, R10dBIN, R2dBIN	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_d\ max$	$T_a \leq 85^\circ\text{C}$	140	mW
Operating temperature	$T_{opr}$		-40 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-50 to +125	$^\circ\text{C}$

### Package Dimensions

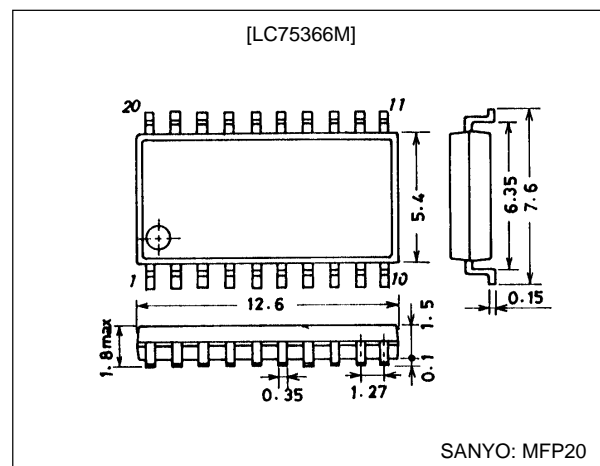
unit: mm

#### 3021B-DIP20



unit: mm

#### 3036B-MFP20



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## LC75366, 75366M

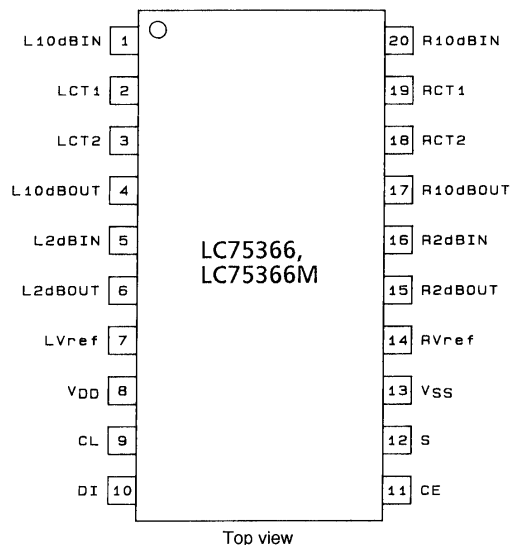
### Allowable Operating Ranges at $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}$	$V_{DD}$	4.0 to 11.0	V
Input high level voltage	$V_{IH}(1)$	CL, DI, CE	$0.3 V_{DD} + 1$ to $V_{DD}$	V
	$V_{IH}(2)$	S	$0.8 V_{DD}$ to $V_{DD}$	V
Input low level voltage	$V_{IL}(1)$	CL, DI, CE	$V_{SS}$ to $0.2 V_{DD}$	V
	$V_{IL}(2)$	S	$V_{SS}$ to $0.2 V_{DD}$	V
Input voltage amplitude	$V_{IN}$	L10dBIN, L2dBIN, R10dBIN, R2dBIN	$V_{SS}$ to $V_{DD}$	Vp-p
Input pulse width	$t_{\text{pw}}$	CL	1 or longer	$\mu\text{s}$
Setup time	$t_{\text{set up}}$	CL, DI, CE	1 or longer	$\mu\text{s}$
Hold time	$t_{\text{hold}}$	CL, DI, CE	1 or longer	$\mu\text{s}$
Operating frequency	fop	CL	Up to 500	kHz

### Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

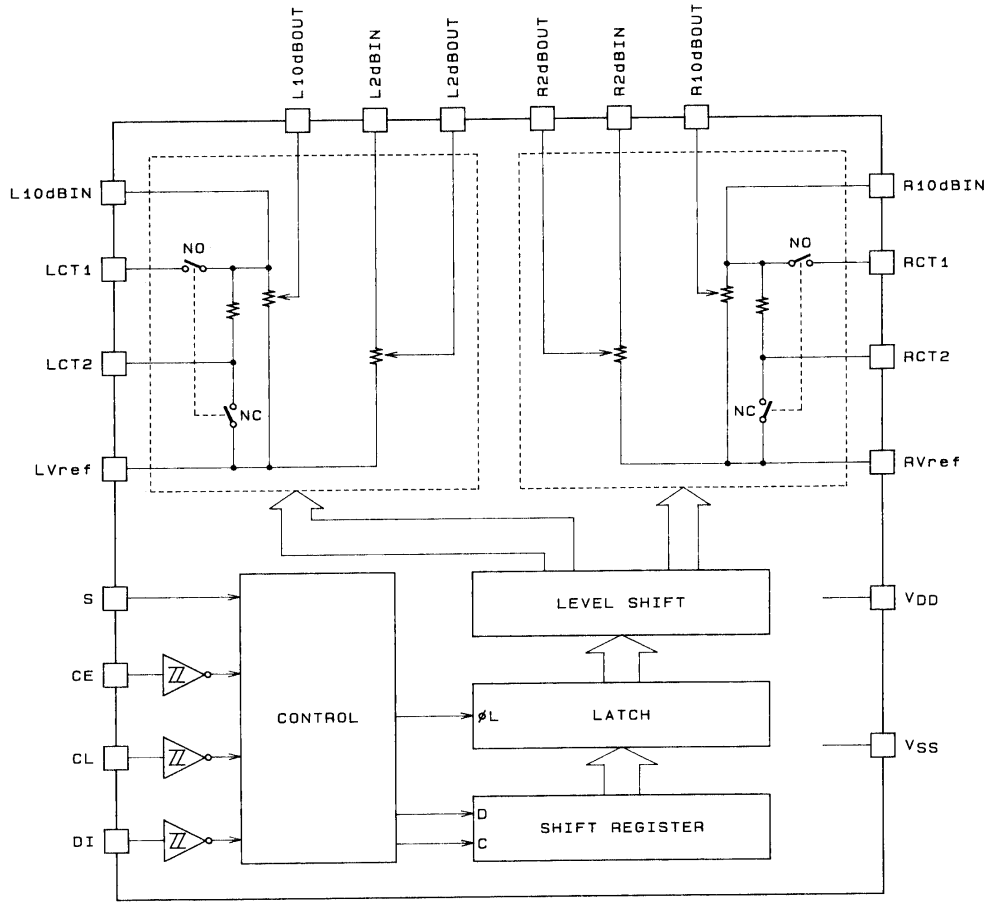
Parameter	Symbol	Conditions	min	typ	max	Unit
Total harmonic distortion	THD (1)	$V_{IN} = 1\text{ Vrms}$ , $f = 1\text{ kHz}$ , all settings flat overall, $V_{DD} = 9\text{ V}$		0.006		%
	THD (2)	$V_{IN} = 1\text{ Vrms}$ , $f = 20\text{ kHz}$ , all settings flat overall, $V_{DD} = 9\text{ V}$		0.015		%
Crosstalk	CT	$V_{IN} = 1\text{ Vrms}$ , $f = 20\text{ kHz}$ , all settings flat overall, $R_g = 1\text{ k}\Omega$		85		dB
Output at maximum attenuation	$V_{O\text{ min}}$	$V_{IN} = 1\text{ Vrms}$ , $f = 20\text{ kHz}$ , volume setting: $-\infty$ , with a $470\text{ }\mu\text{F}$ capacitor between L/R Vref and $V_{SS}$		-80		dB
Total resistance	$R_{VOL}(1)$	10 dB steps	28.2	47	65.8	$\text{k}\Omega$
	$R_{VOL}(2)$	2 dB steps	12	20	28	$\text{k}\Omega$
Output off leakage current	$I_{\text{off}}$	L10dBIN, R10dBIN, LCT1, L2dBIN, R2dBIN, RCT1, L10dBOUT, R10dBOUT, LCT2, L2dBOUT, R2dBOUT, RCT2, LVref, RVref	-10		+10	$\mu\text{A}$
Input high level current	$I_{IH}$	$V_I = V_{DD}$ (CL, CE and DI pins)			10	$\mu\text{A}$
Input low level current	$I_{IL}$	$V_I = V_{SS}$ (CL, CE and DI pins)	-10			$\mu\text{A}$
Output noise voltage	$V_N$	All settings flat overall (IHF-A), $V_{DD} = 9\text{ V}$ , $R_g = 1\text{ k}\Omega$		2	10	$\mu\text{V}$
Current drain	$I_{DD}$	$V_{DD} - V_{SS} = 11\text{ V}$			1	mA
Analog switch on resistance (Design target value)	$R_{ON}$	CT1	180	300	420	$\Omega$
		For use between CT2 and Vref	90	150	210	$\Omega$
		0 dB, $-\infty$	0.6	1.0	1.4	$\text{k}\Omega$
		Other than the above	6.0	10.0	14.0	$\text{k}\Omega$

### Pin Assignment



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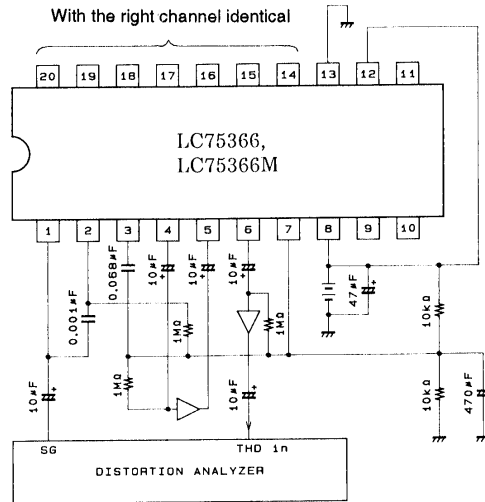
Equivalent Circuit Block Diagram



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Test Circuits

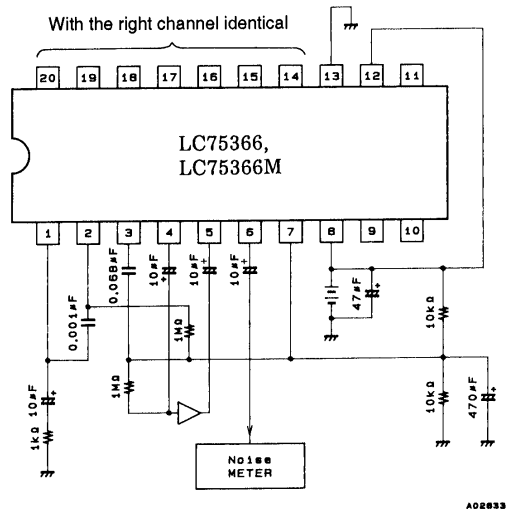
1. Total harmonic distortion



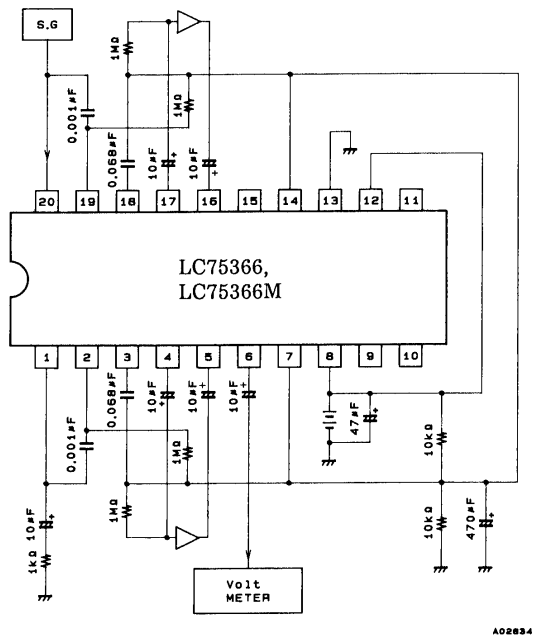
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## LC75366, 75366M

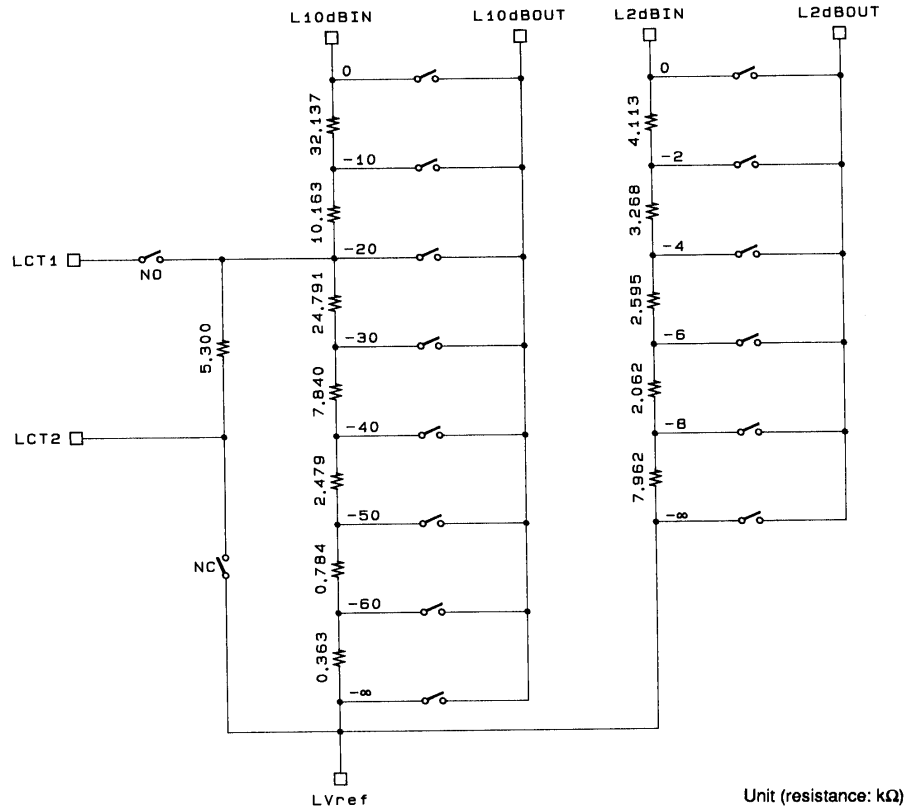
### 2. Output noise voltage



### 3. Crosstalk



Volume Block Equivalent Circuit



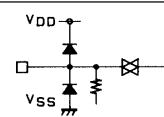
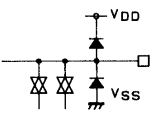
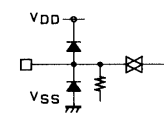
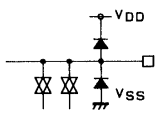
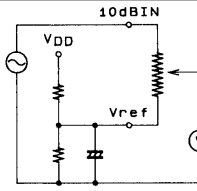
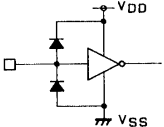
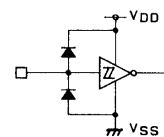
Unit (resistance: kΩ)

The right channel is identical.

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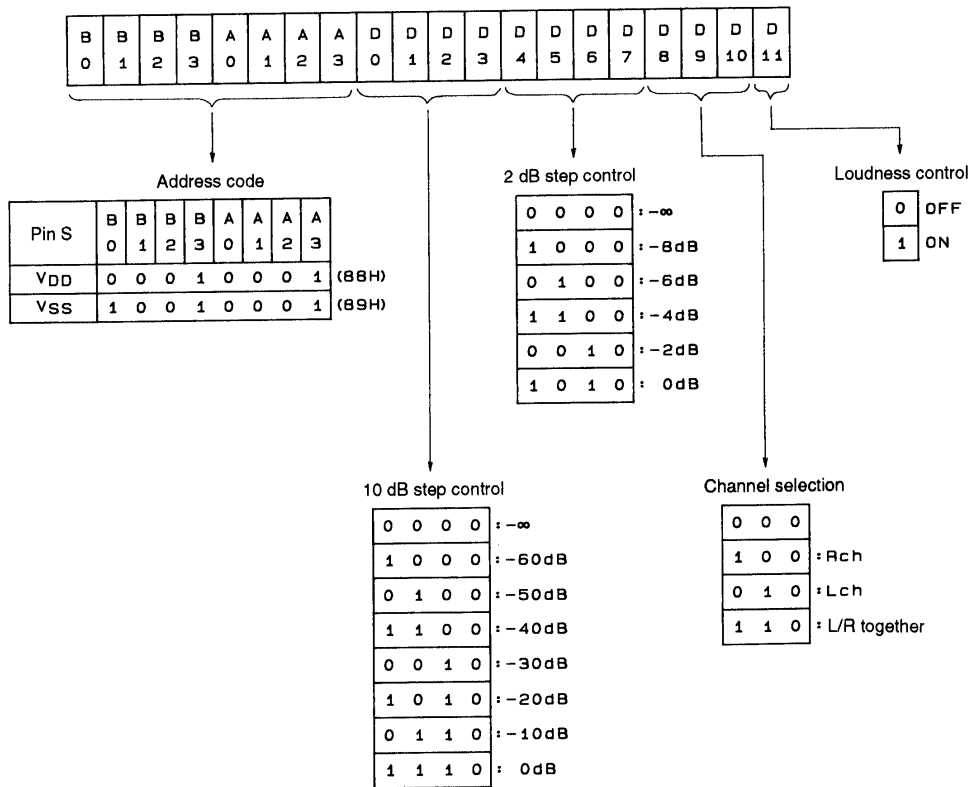
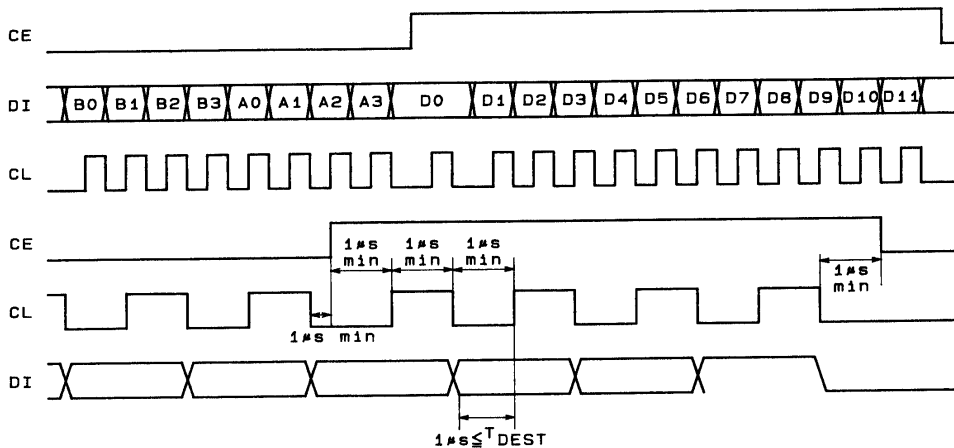
## LC75366, 75366M

### Pin Functions

Pin No.	Symbol	Function	Note
1	L10dBIN	Input pins for the 10 dB step attenuator. Must be driven from a low impedance.	 A02836
20	R10dBIN		
2	LCT1	Loudness connections. Connect a high band compensation capacitor between CT1 and 10dBIN and connect a low band compensation capacitor between CT2 and Vref.	
3	LCT2		
19	RCT1		
18	RCT2		
4	L10dBOUT	Output pins for the 10 dB step attenuator. These outputs must be received by a load of about 1 MΩ.	 A02837
17	R10dBOUT		
5	L2dBIN	Input pins for the 2 dB step attenuator. Must be driven from a low impedance.	 A02836
16	R2dBIN		
6	L2dBOUT	Output pins for the 2 dB step attenuator. These outputs must be received by a load of about 1 MΩ.	 A02837
15	R2dBOUT		
7	LVref	Volume circuit common pins. The impedance of the pattern connected to these pins should be kept as low as possible. Since the capacitors between Vref and VSS form the residual resistance components when the volume is cut, adequate care must be taken in determining the value of these capacitors.	 A02838
14	RVref		
12	S	Pin that selects the address code in the data format. Data will be accepted for an address code of 88 when this pin is tied to VDD, and for an address code of 89 when tied to VSS.	 A02839
9	CL	Serial data and clock inputs for control	 A02840
10	DI		
11	CE	Chip enable. The internally latched data is written and the analog switches operate when this pin goes from high to low. Data transfer is enabled when this pin is at the high level.	
8	VDD	These pins must be connected to the power supply.	
13	VSS		

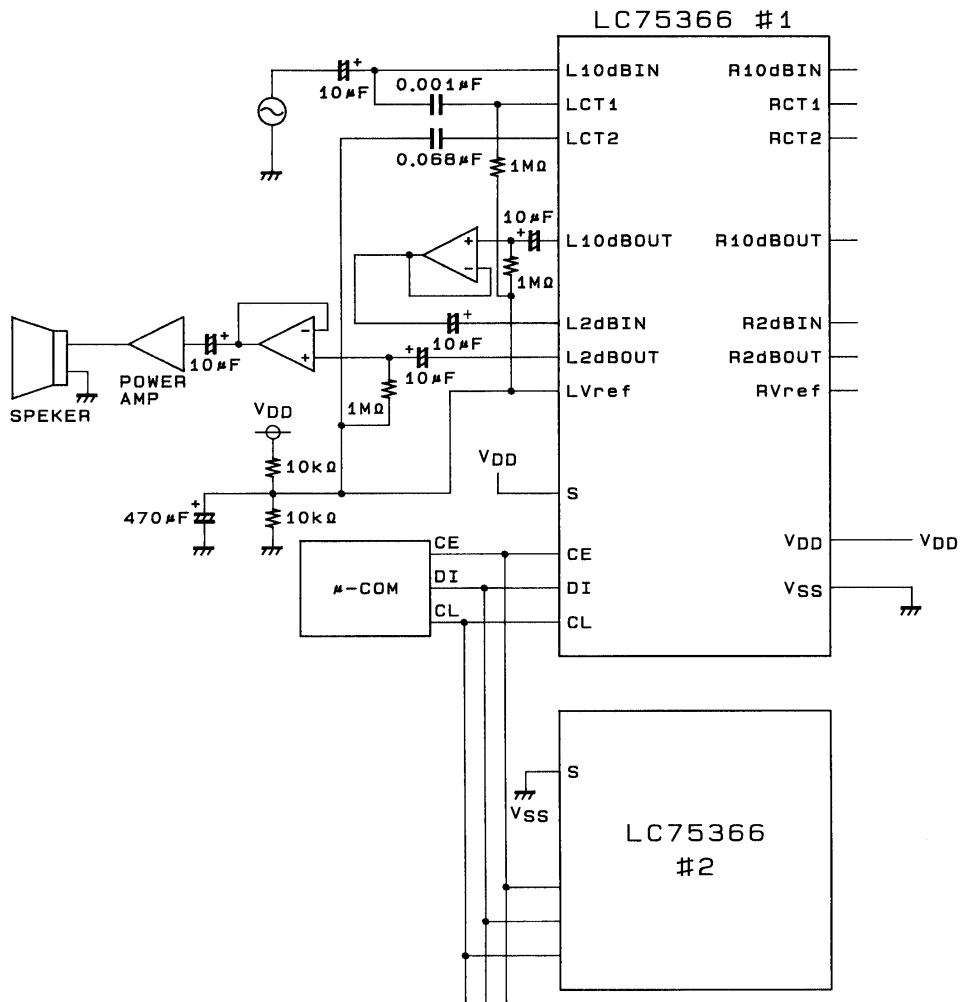
**Control System Timing and Data Format**

Apply the stipulated serial data to the CE, CL and DI pins to control the LC75366 and LC75366M. The data consists of 20 bits, of which 8 bits are the address and 12 bits are control data.



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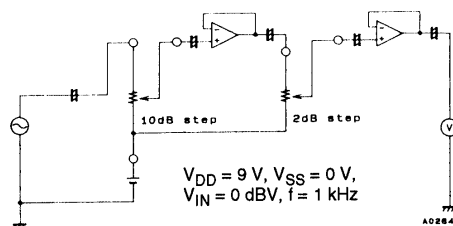
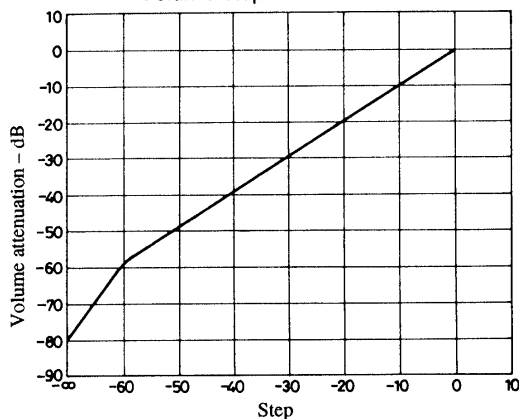
Sample Application Circuit



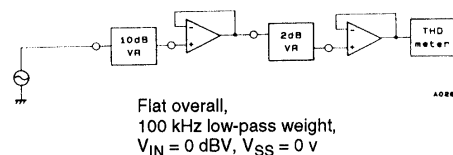
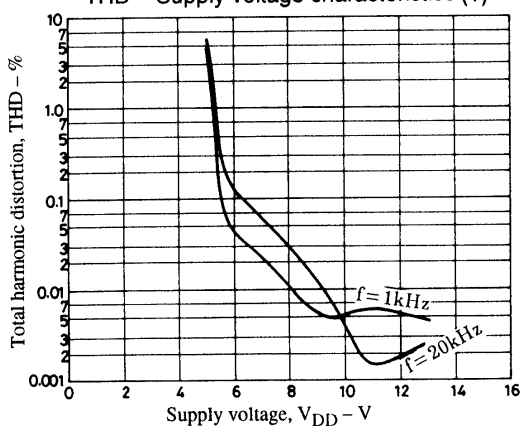
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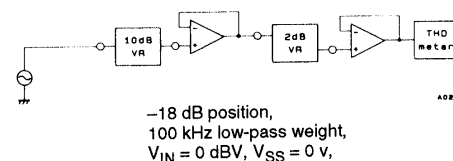
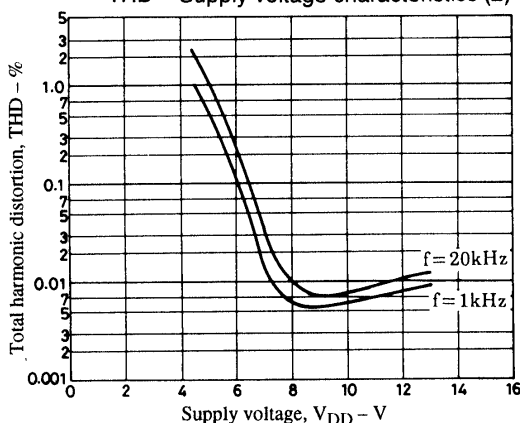
Volume step characteristics



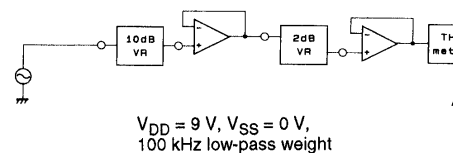
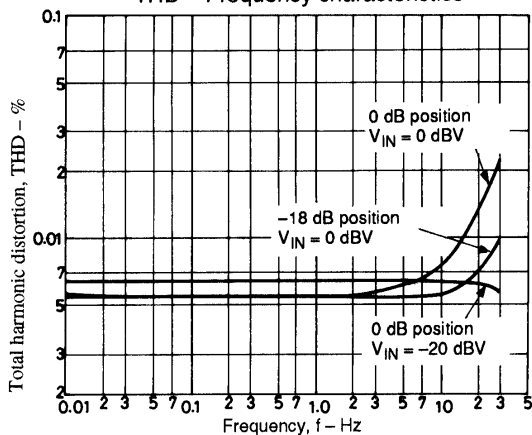
THD – Supply voltage characteristics (1)

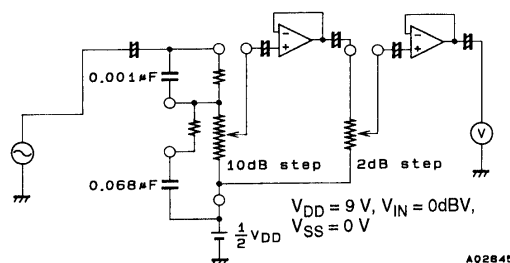
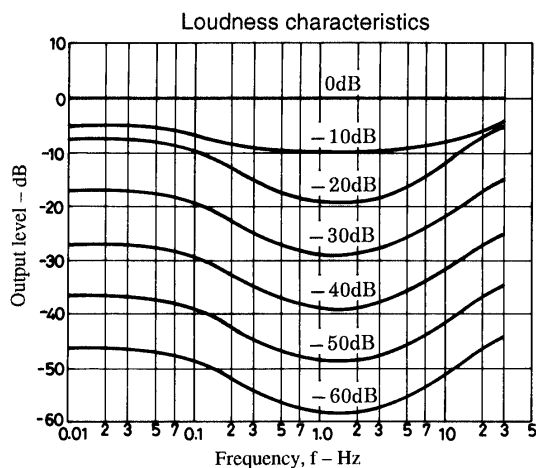
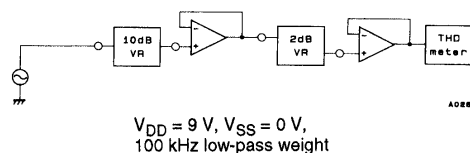
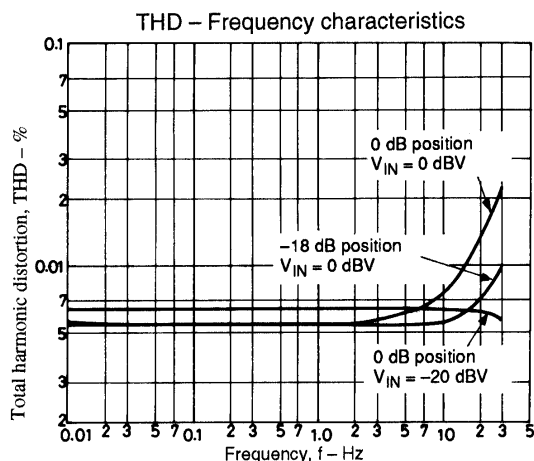


THD – Supply voltage characteristics (2)



THD – Frequency characteristics





**Loudness Function External Circuit Constant Calculation Example**

First, refer to the LC75366 and LC75366M 10 dB step internal equivalent circuit shown on page 5. Figure 1 below shows this circuit simplified with the external components used for the loudness function connected for this calculation. The sample calculation below uses this diagram to acquire a 5 dB boost at f = 100 Hz.

(f = 100 Hz, 5 dB boost)

Let R and C in Figure 1 be:

R1 = R2 = 10 kΩ

R3 = 1 kΩ

C1 = Z1, C2 = Z2

Then:

$$V_{OUT} = \frac{\frac{R2 (R3 + Z2)}{R2 + R3 + Z2}}{\frac{R1 \cdot Z1}{R1 + Z1} + \frac{R2 (R3 + Z2)}{R2 + R3 + Z2}} = -20 \text{ dB}$$

(at = 1 kHz)

$$V_{OUT} = \frac{\frac{R2 (R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}}{\frac{R1 \cdot 10 \cdot Z1}{R1 + 10 \cdot Z1} + \frac{R2 (R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}} = -15 \text{ dB}$$

(at = 100 Hz)

Solving the above equations gives:

Z1 ≠ 178.3 kΩ and Z2 = 176 Ω

Therefore, under such conditions where  $f = 1 \text{ kHz}$ , specifications may be satisfied if C (capacitor) having these impedances is supplied externally.

The result is that  $C1 = 893 \text{ pF}$  and  $C2 = 0.9 \text{ }\mu\text{F}$ .

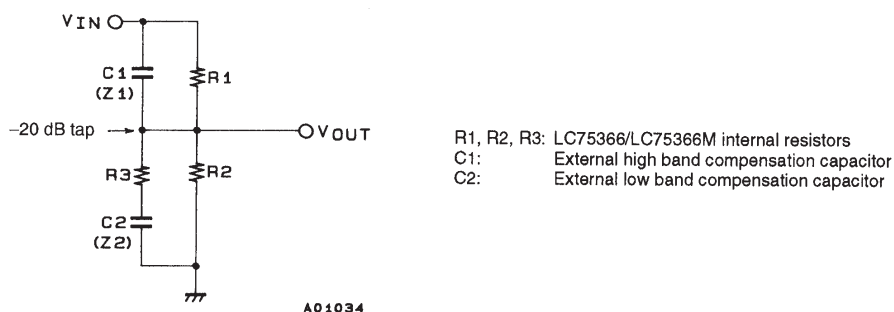


Figure 1

### Usage Notes

1. The states of the internal analog switches will be indeterminate when power is first applied. Muting should be applied externally until control data has been transferred and stored.
2. The signal lines for the CL, DI and CE pins should either be covered by the pattern ground or be formed from shielded cable to prevent the high-frequency digital signals transmitted over these lines from entering the analog system.

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