



LC75372E

Electronic Volume Control for Car Stereo Systems



Overview

The LC75372E is an electronic volume control that can implement volume, balance, fader, bass/treble, loudness, input switching, and input level control functions with a minimal number of external components.

Features

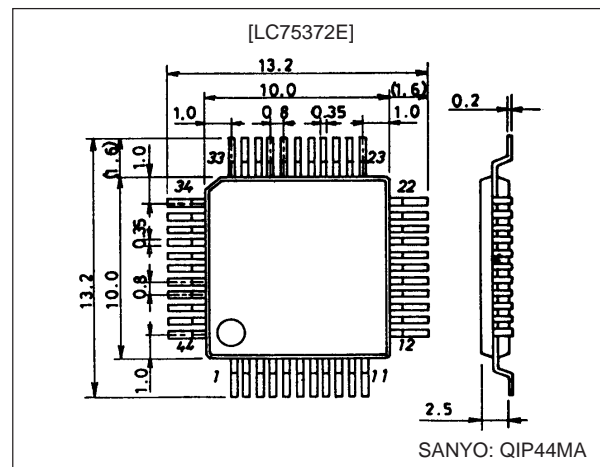
- Volume: Provides 81 positions, from 0 dB to -79 dB (in 1-dB steps) and $-\infty$. A balance function can be implemented by controlling the left and right channels independently.
- Fader: This function can attenuate either the rear or the front outputs over 16 positions. (From 0 to -20 dB in 2-dB steps, from -20 to -25 dB in one 5-dB step, from -25 to -45 dB in 10-dB steps, -60 dB, and $-\infty$.)
- Bass/treble: Forms an NF-type tone control circuit (LUX type) with the addition of external capacitors. The base and treble controls each have 15 positions.
- Loudness: The volume resistor ladders are tapped starting at the -20 -dB position. A loudness function can be implemented by adding external RC circuits at these taps.
- The signal can be selected from one of three inputs for each of the left and right channels. The input signals can be amplified from 0 to $+18$ dB in 6-dB steps.
- On-chip buffer amplifiers for a minimum of external components.
- Minimal switching noise due to fabrication in a silicon-gate CMOS process.

- Built-in reference voltage generation circuit
- Serial data input: Supports CCB format communication with the system controller.

Package Dimensions

unit: mm

3148-QFP44MA



- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0$ V

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|--------------|--|----------------------------------|------------------|
| Maximum supply voltage | V_{DD} max | V_{DD} | 11 | V |
| Maximum input voltage | V_{IN} max | CL, DI, CE, LIN, RIN, LFIN, RFIN, L1 to L3, R1 to R3 | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| Allowable power dissipation | P_d max | $T_a \leq 85^\circ\text{C}$ | 260 | mW |
| Operating temperature | T_{opr} | | -40 to $+85$ | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -50 to $+125$ | $^\circ\text{C}$ |

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41596HA (OT) No. 5330-1/18

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Allowable Operating Ranges at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

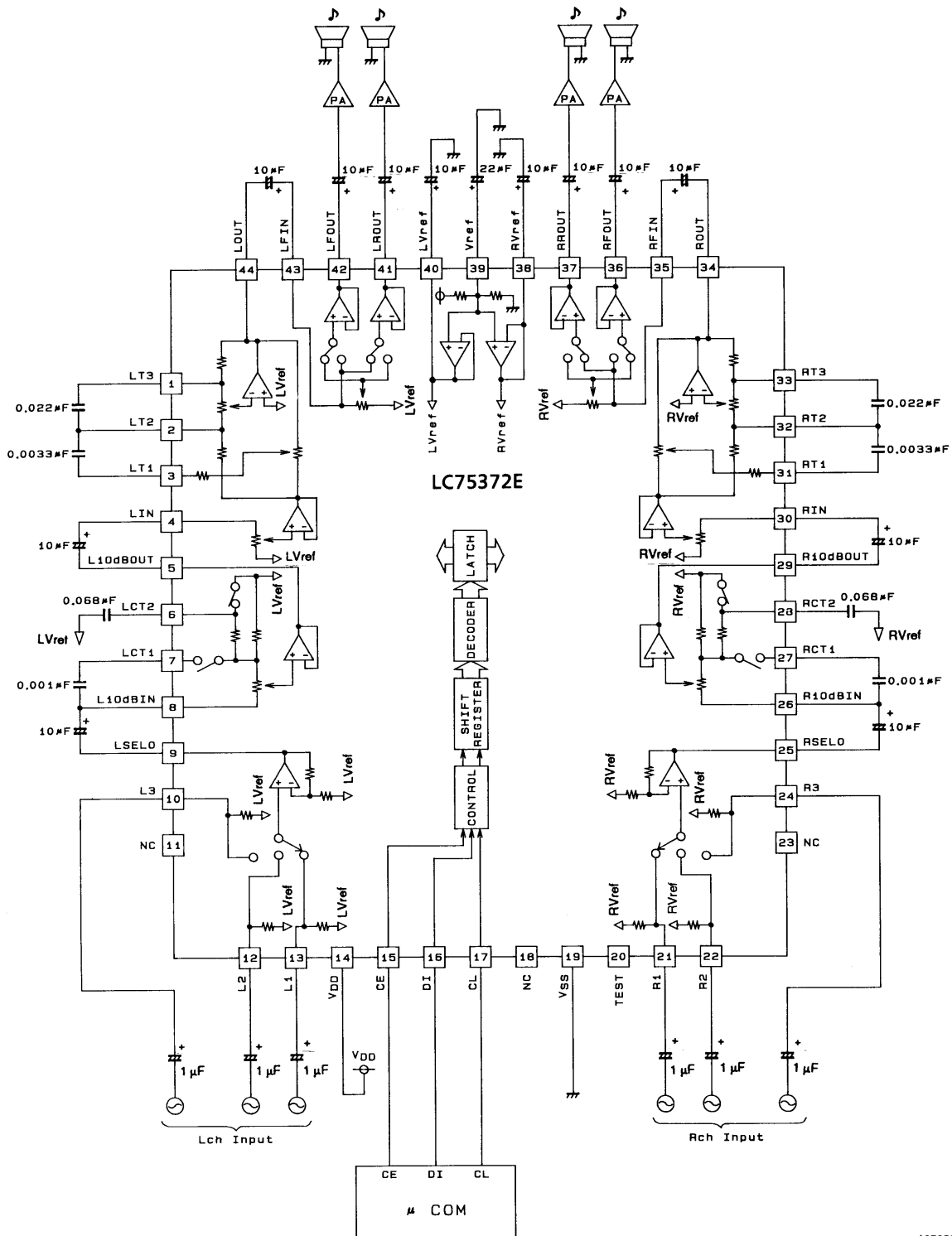
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|--------------------------|--------------------|--|----------|-----|----------|---------------|
| Supply voltage | V_{DD} | V_{DD} | 6.0 | | 10.0 | V |
| Input high-level voltage | V_{IH} | CL, DI, CE | 4.0 | | V_{DD} | V |
| Input low-level voltage | V_{IL} | CL, DI, CE | V_{SS} | | 1.0 | V |
| Input voltage amplitude | V_{IN} | CL, DI, CE, LIN, RIN, LFIN, RFIN, L1 to L3, R1 to R3 | V_{SS} | | V_{DD} | Vp-p |
| Input pulse width | $t_{\phi W}$ | CL | 1 | | | μs |
| Setup time | t_{setup} | CL, DI, CE | 1 | | | μs |
| Hold time | t_{hold} | CL, DI, CE | 1 | | | μs |
| Operating frequency | fopg | CL | | | 500 | kHz |

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} = 9\text{ V}$, $V_{SS} = 0\text{ V}$

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|-------------------------------|---------------------|---|---------|------------|----------|-------------------------|
| [Input Block] | | | | | | |
| Input resistance | R_{in} | L1 to L3, R1 to R3 | 30 | 50 | 70 | $\text{k}\Omega$ |
| Minimum input gain | $G_{in\text{ min}}$ | | -2 | 0 | +2 | dB |
| Maximum input gain | $G_{in\text{ max}}$ | | +16.0 | +18.0 | +20.0 | dB |
| Step resolution | G_{step} | | | +6.0 | | dB |
| [Volume Control Block] | | | | | | |
| Input resistance | R_{v10} | L10dBIN, R10dBIN: 10-dB steps, loudness off | 30 | 50 | 70 | $\text{k}\Omega$ |
| | R_{v1} | LIN, RIN: 1-dB steps | 12 | 20 | 28 | $\text{k}\Omega$ |
| Step resolution | AT_{step} | | | 1 | | dB |
| Step error | AT_{err} | step = 0 to -20 dB | -1 | 0 | +1 | dB |
| | | step = -20 to -50 dB | -3 | 0 | +3 | dB |
| [Fader Volume Block] | | | | | | |
| Input resistance | R_{fd} | LFIN, RFIN | 12 | 20 | 28 | $\text{k}\Omega$ |
| Step resolution | AT_{step} | step = 0 to -20 dB | | 2 | | dB |
| | | step = -20 to -25 dB | | 5 | | dB |
| | | step = -25 to -45 dB | | 10 | | dB |
| Step error | AT_{err} | step = 0 to -45 dB | -2 | 0 | +2 | dB |
| | | step = -45 to -60 dB | -3 | 0 | +3 | dB |
| Output load resistance | R_L | LFOUT, LROUT, RFOUT, RROUT | 10 | | | $\text{k}\Omega$ |
| [Bass/Treble Control Block] | | | | | | |
| Bass control range | G_{bass} | Max. boost/cut | ± 9 | ± 10.5 | ± 12 | dB |
| Treble control range | G_{tre} | Max. boost/cut | ± 8 | ± 10.5 | ± 13 | dB |
| [Overall Characteristics] | | | | | | |
| Total harmonic distortion | THD (1) | $V_{IN} = 1\text{ V}_{\text{rms}}$, $f = 1\text{ kHz}$, all settings flat overall | | 0.045 | | % |
| | THD (2) | $V_{IN} = 1\text{ V}_{\text{rms}}$, $f = 20\text{ kHz}$, all settings flat overall | | 0.040 | | % |
| Crosstalk | CT | $V_{IN} = 1\text{ V}_{\text{rms}}$, $f = 1\text{ kHz}$, all settings flat overall, $R_g = 1\text{ k}\Omega$ | | 80 | | dB |
| Output at maximum attenuation | $V_{O\text{ min}}$ | $V_{IN} = 1\text{ V}_{\text{rms}}$, $f = 1\text{ kHz}$, main volume at $-\infty$ | | -78 | | dB |
| | | $V_{IN} = 1\text{ V}_{\text{rms}}$, $f = 1\text{ kHz}$, main volume at $-\infty$, INMUTE | | -81 | | dB |
| Output noise voltage | V_N (1) | All settings flat overall (IHF-A), $R_g = 1\text{ k}\Omega$ | | 15 | 30 | μV |
| | V_N (2) | All settings flat overall (DIN-AUDIO), $R_g = 1\text{ k}\Omega$ | | 20 | 40 | μV |
| Current drain | I_{DD} | $V_{DD} - V_{SS} = 10\text{ V}$ | | 25 | 30 | mA |
| Input high-level current | I_{IH} | CL, DI, CE: $V_{IN} = 9\text{ V}$ | | | 10 | μA |
| Input low-level current | I_{IL} | CL, DI, CE: $V_{IN} = 0\text{ V}$ | -10 | | | μA |
| Maximum input level | V_{CL} | All settings flat overall, measurement point; fader output THD = 1%, $R_L = 10\text{ k}\Omega$ | | 2 | | V_{rms} |

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Equivalent Circuit Block Diagram and Sample Application Circuit

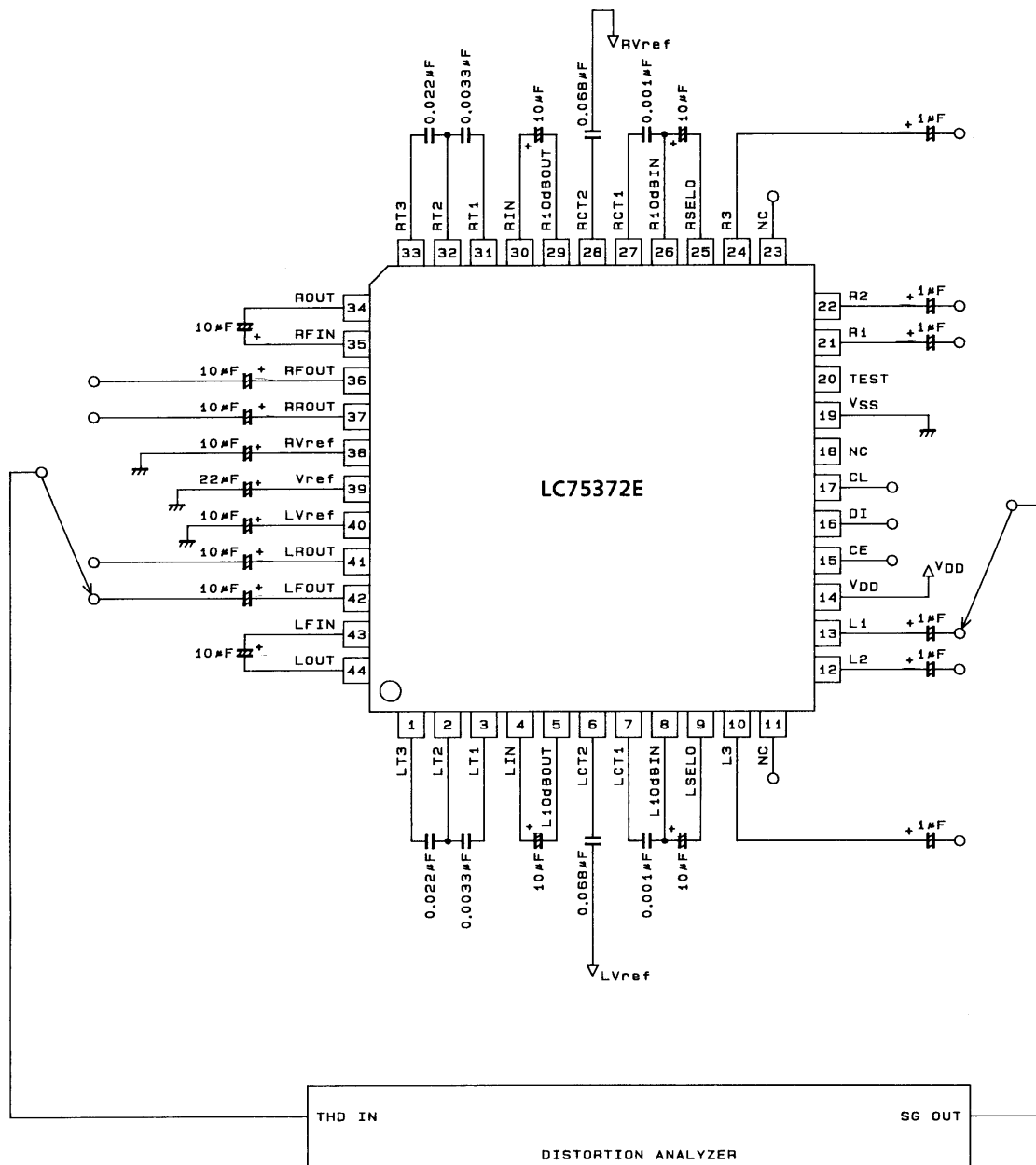


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Electrical Characteristics Test Circuits

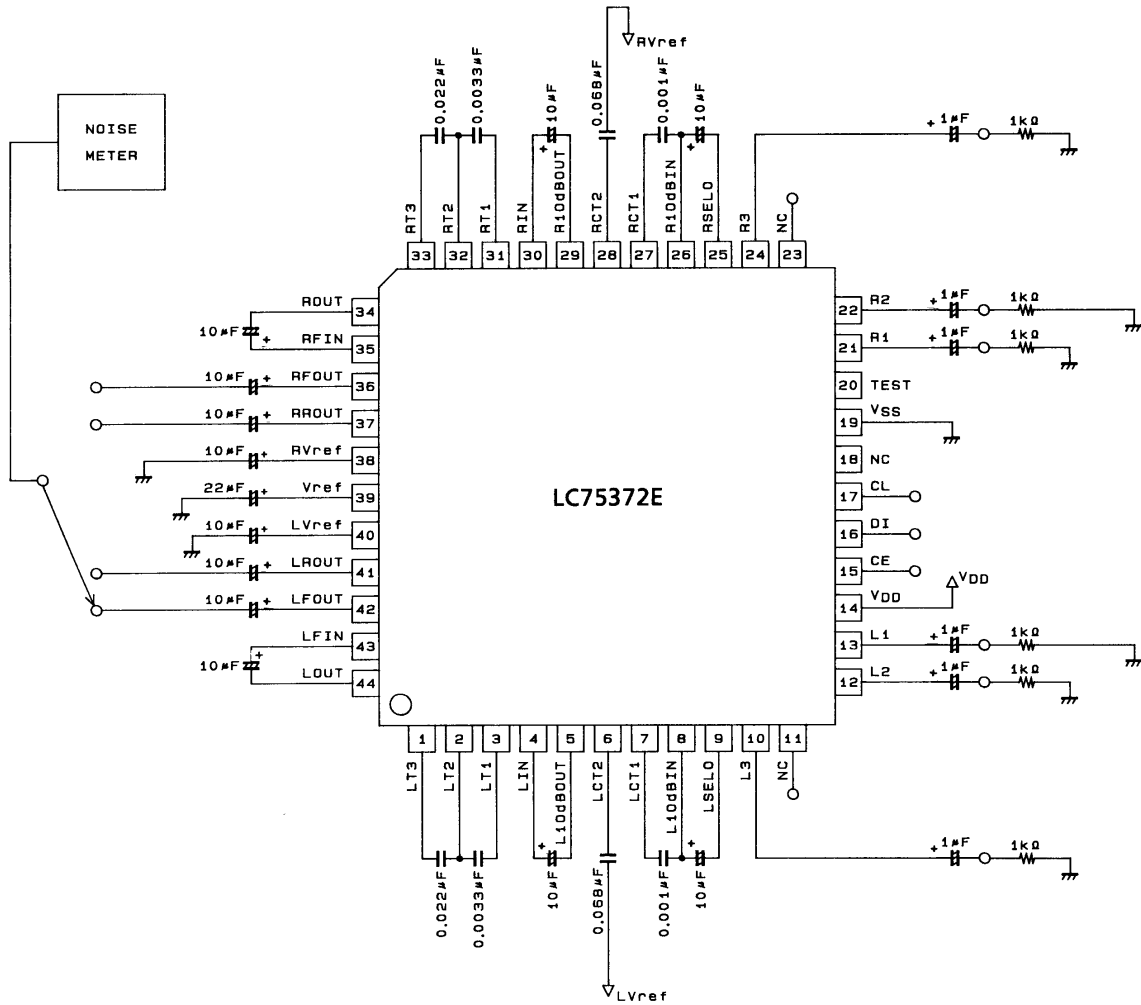
1. Total harmonic distortion



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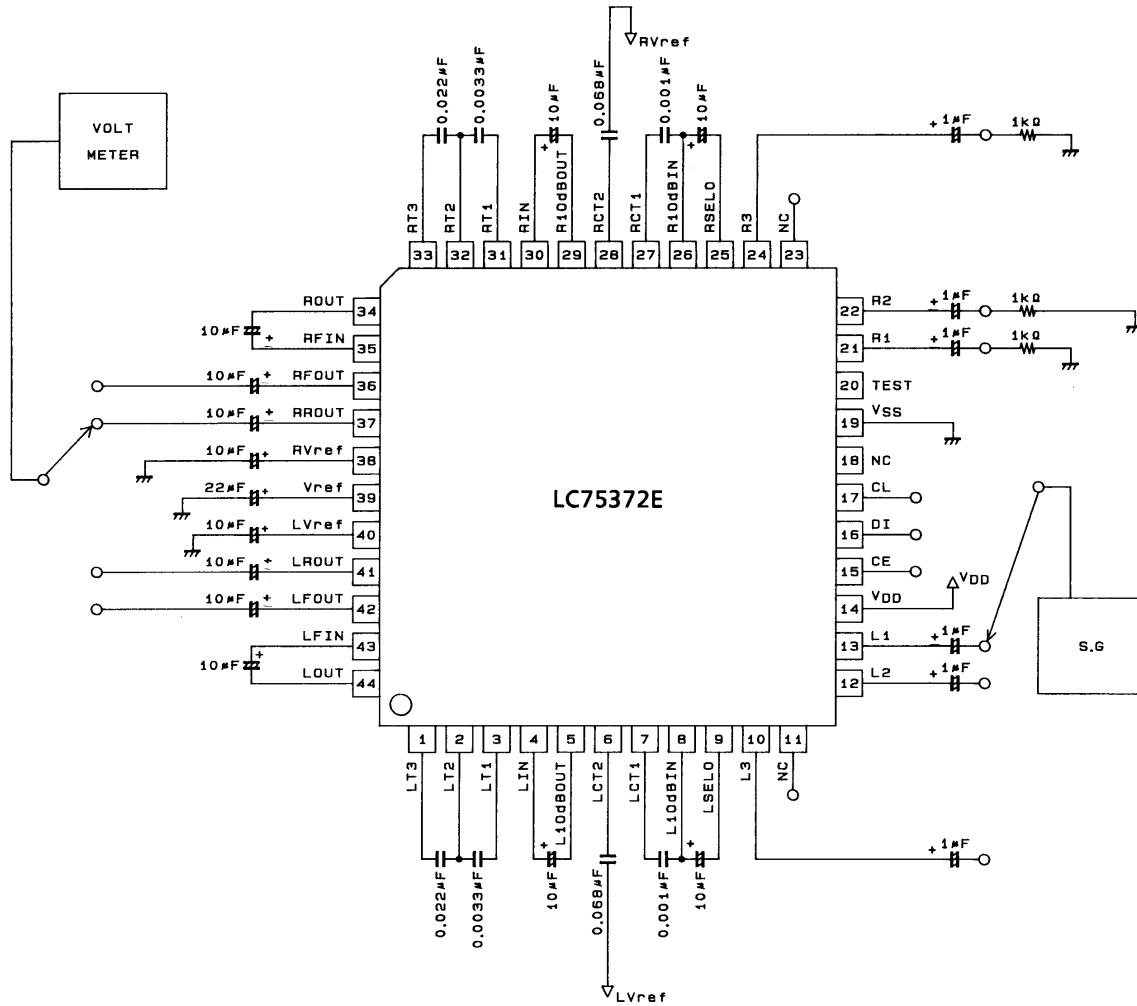
2. Output noise voltage



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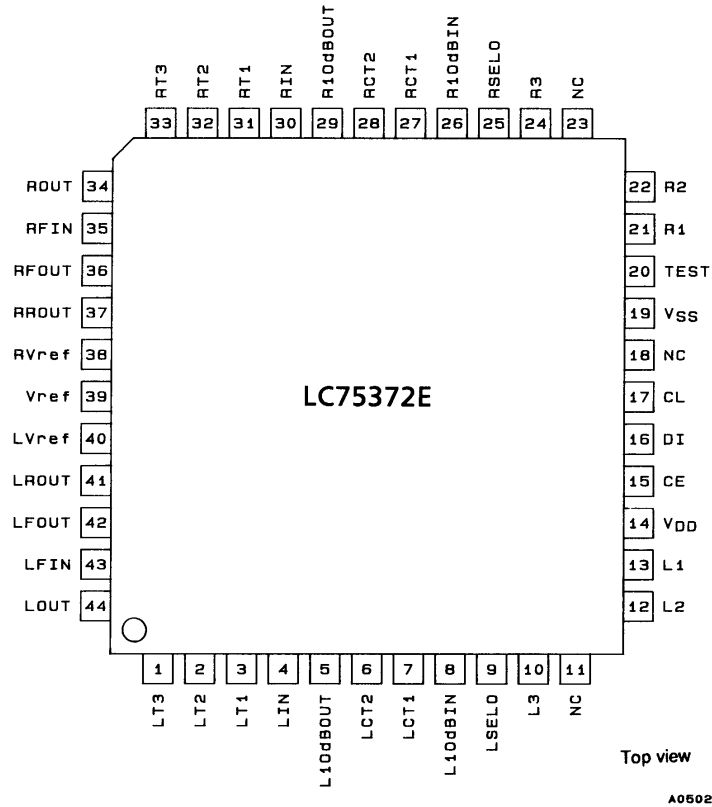
3. Crosstalk



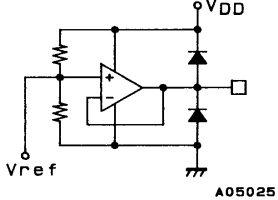
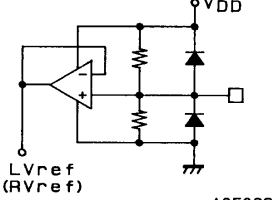
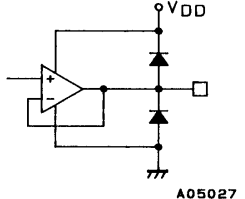
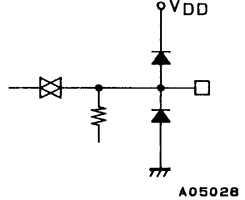
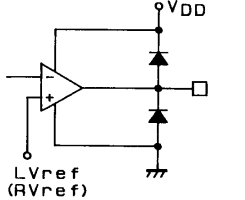
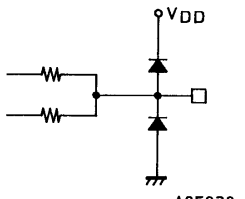
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Pin Assignment



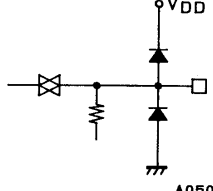
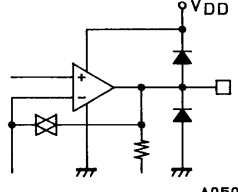
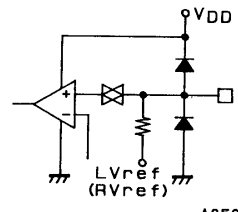
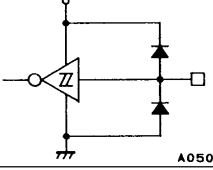
Pin Functions

| Pin No. | Symbol | Equivalent I/O circuit | Function |
|-------------------------------|--|--|---|
| 40 38 | LVref RVref | <ul style="list-style-type: none"> Common pins for the main volume block, fader volume block, tone block, gain control block, and input switching block. Since the capacitors connected between LVref/RVref and V_{SS} become the residual resistance when the volume control is at maximum attenuation, the values of these capacitors must be chosen carefully. The applied voltage must never exceed V_{DD}. |  <p>A05025</p> |
| 39 | Vref | 0.488 V_{DD} voltage generation block. A capacitor must be connected between Vref and V_{SS} to suppress power supply ripple. |  <p>A05026</p> |
| 41 42 37 36 | LROUT LFOUT RROUT RFOUT | <ul style="list-style-type: none"> Fader outputs. The front and rear systems can be attenuated independently. The amount of attenuation is the same in the left and right channels. Low impedance operational amplifier outputs |  <p>A05027</p> |
| 43 35 | LFIN RFIN | <ul style="list-style-type: none"> Fader inputs Must be driven from low-impedance circuits. |  <p>A05028</p> |
| 44 34 | LOUT ROUT | Tone control outputs |  <p>A05029</p> |
| 3 2 1 31 32 33 | LT1 LT2 LT3 RT1 RT2 RT3 | Connections for the bass and treble compensation capacitors for the tone control circuit Connect high-band compensation capacitors between T1 and T2. Connect low-band compensation capacitors between T2 and T3. |  <p>A05030</p> |
| 7 6 27 28 | LCT1 LCT2 RCT1 RCT2 | Loudness pins. Connect high-band compensation capacitors between LCT1/RCT1 and L10dBIN/R10dBIN, and connect low-band compensation capacitors between LCT2/RCT2 and LVref/RVref. | |

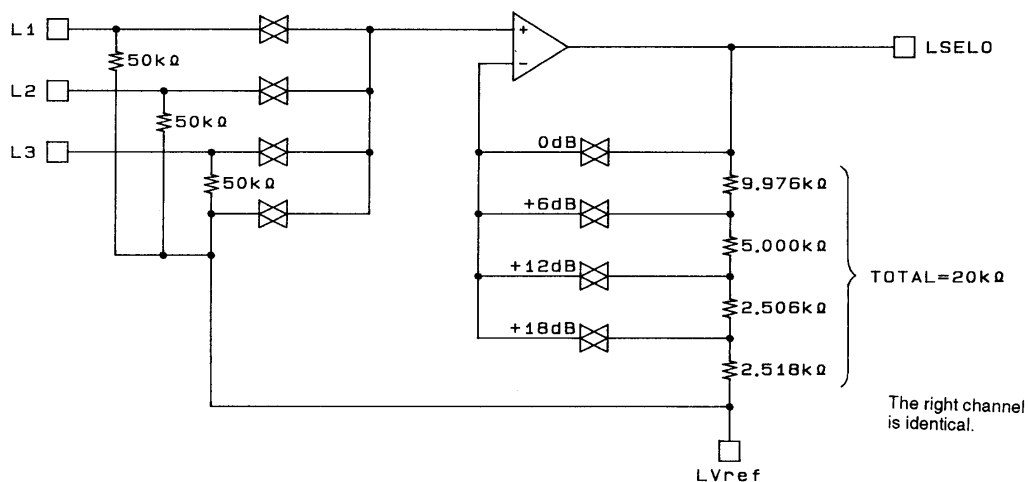
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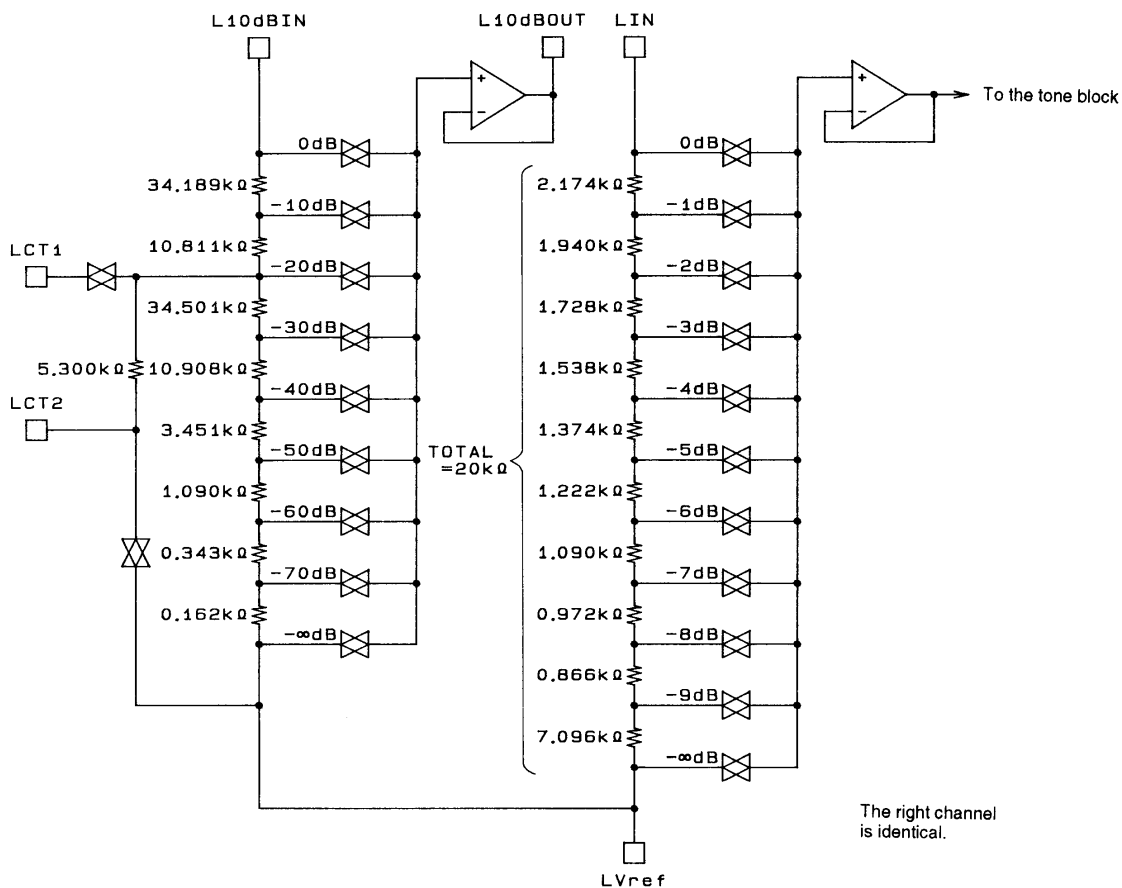
| Pin No. | Symbol | Equivalent I/O circuit | Function |
|----------------------------------|----------------------------------|---|--|
| 8 26 | L10dBIN R10dBIN | <ul style="list-style-type: none"> • 10-dB volume control inputs • These inputs must be driven from low-impedance circuits. |  <p style="text-align: right;">A05031</p> |
| 9 25 | LSELO RSELO | Outputs from the input selector |  <p style="text-align: right;">A05032</p> |
| 13 12 10 21 22 24 | L1 L2 L3 R1 R2 R3 | Signal inputs |  <p style="text-align: right;">A05033</p> |
| 14 | V _{DD} | Power supply connection | |
| 19 | V _{SS} | Ground | |
| 15 | CE | Chip enable. Data is latched internally at the point this pin goes from high to low. The analog switches operate at that point. Data transfer is enabled when this pin is high. |  <p style="text-align: right;">A05034</p> |
| 16 17 | DI CL | Inputs for the serial data and clock used for LSI control. | |
| 20 | TEST | Test input (Must be left open during normal operation.) | |
| 5 29 | L10dBOUT R10dBOUT | 10-dB block outputs | |
| 4 30 | LIN RIN | <ul style="list-style-type: none"> • 1-dB block inputs • These inputs must be driven by low-impedance circuits. | |
| 11 18 23 | NC | No-connection pins. | |

Input Block Equivalent Circuit



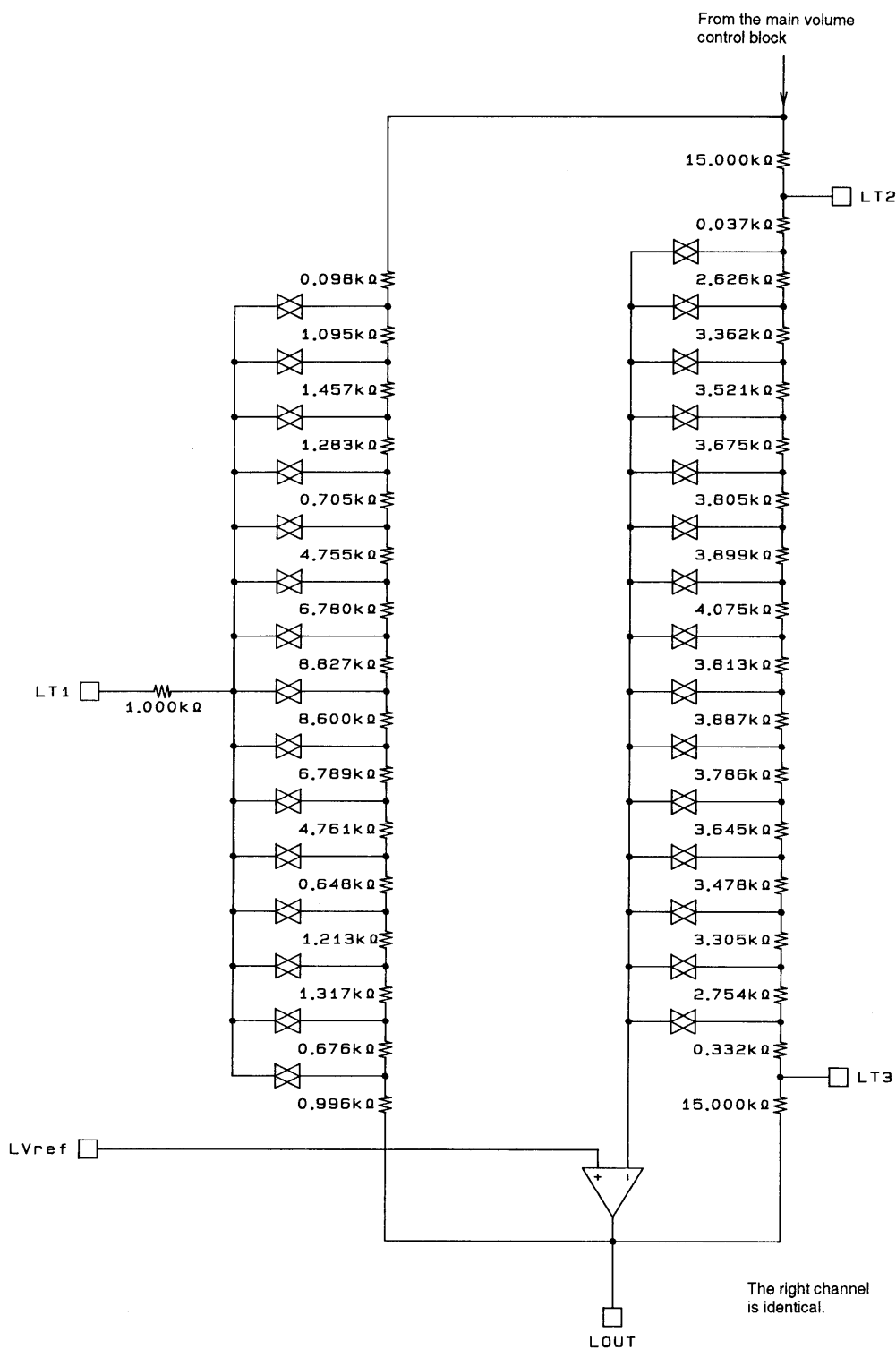
A05035

Main Volume Control Equivalent Circuit

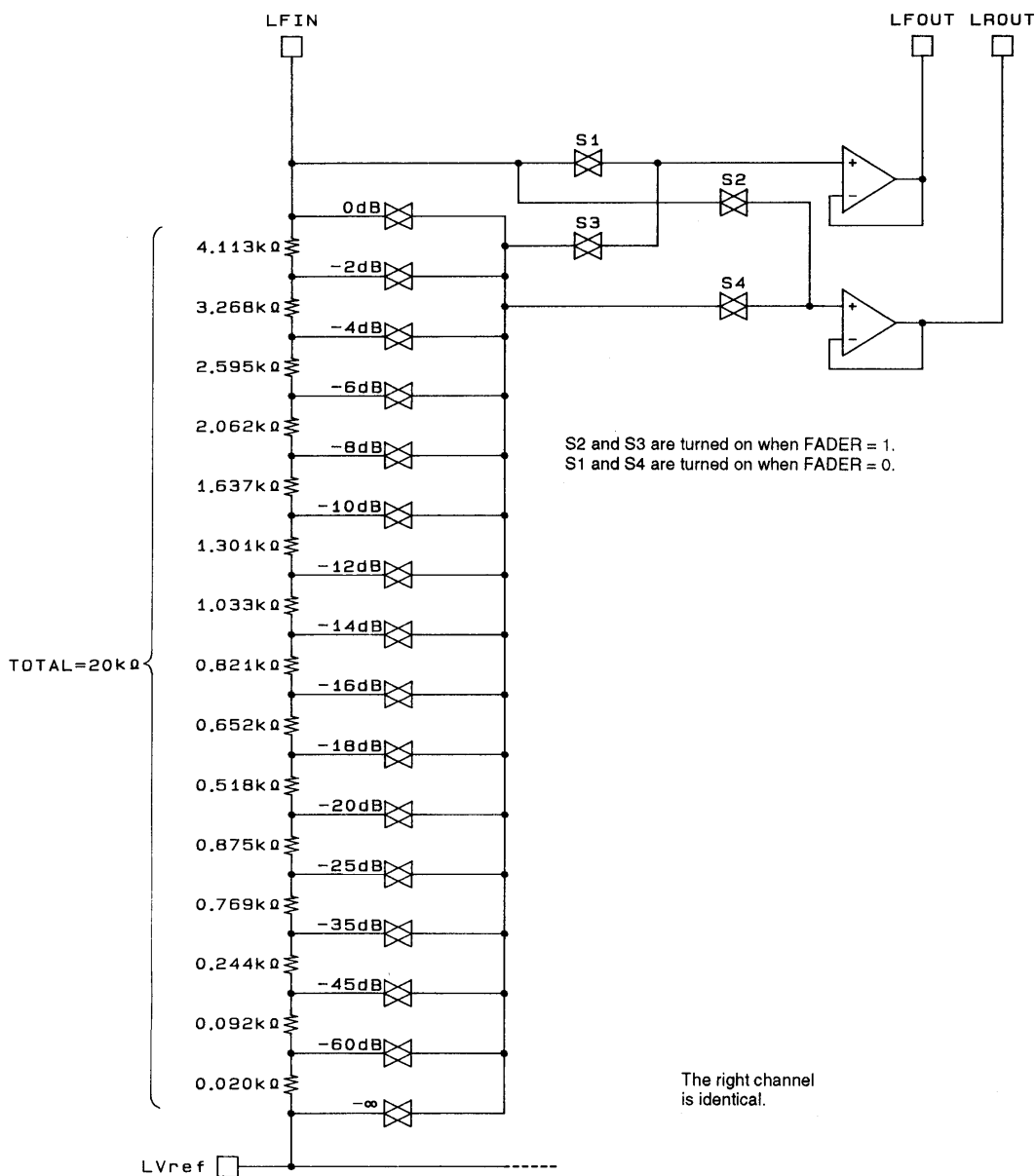


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Tone Control Block Equivalent Circuit



Fader Volume Control Block Equivalent Circuit



When data indicating an gain of $-\infty$ is sent to the main volume control 1-dB step function, S1 and S2 open, and S3 and S4 go on at the same time.

A05038

Sample Calculation of the Loudness Circuit External Constants

First, see the LC75372E 10-dB step internal equivalent circuit shown on page 10. Figure 1 shows a circuit to which the loudness circuit external components have been added, and which has been simplified for this calculation. The sample calculation below uses this circuit diagram to acquire a 5-dB boost at $f = 100$ Hz.

($f = 100$ Hz, 5-dB boost)

Assuming that the resistors and capacitors in Figure 1 have the following values:

$$R1 = R2 = 50 \text{ k}\Omega$$

$$R3 = 5 \text{ k}\Omega$$

$$\text{And } C1 = Z1 \text{ and } C2 = Z2.$$

Then:

$$V_{\text{OUT}} = \frac{\frac{R2 (R3 + Z2)}{R2 + R3 + Z2}}{\frac{R1 \cdot Z1}{R1 + Z1} + \frac{R2 (R3 + Z2)}{R2 + R3 + Z2}} = -20 \text{ dB}$$

(at = 1 kHz)

$$V_{\text{OUT}} = \frac{\frac{R2 (R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}}{\frac{R1 \cdot 10 \cdot Z1}{R1 + 10 \cdot Z1} + \frac{R2 (R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}} = -15 \text{ dB}$$

(at = 100 Hz)

From the above equations we find:

$$Z1 \neq 891.5 \text{ k}\Omega \text{ and } Z2 = 880 \Omega.$$

Therefore, the specifications will be met if capacitors that have these impedances at $f = 1$ kHz are connected externally.

The result is that $C1 = 178.5 \text{ pF}$ and $C2 = 0.18 \mu\text{F}$.

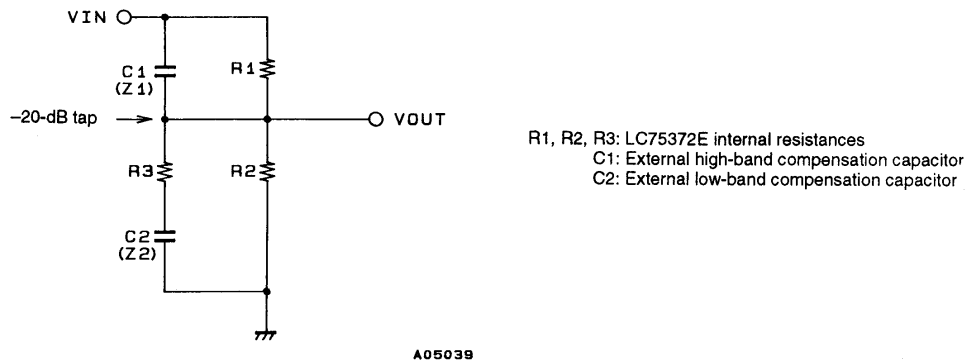
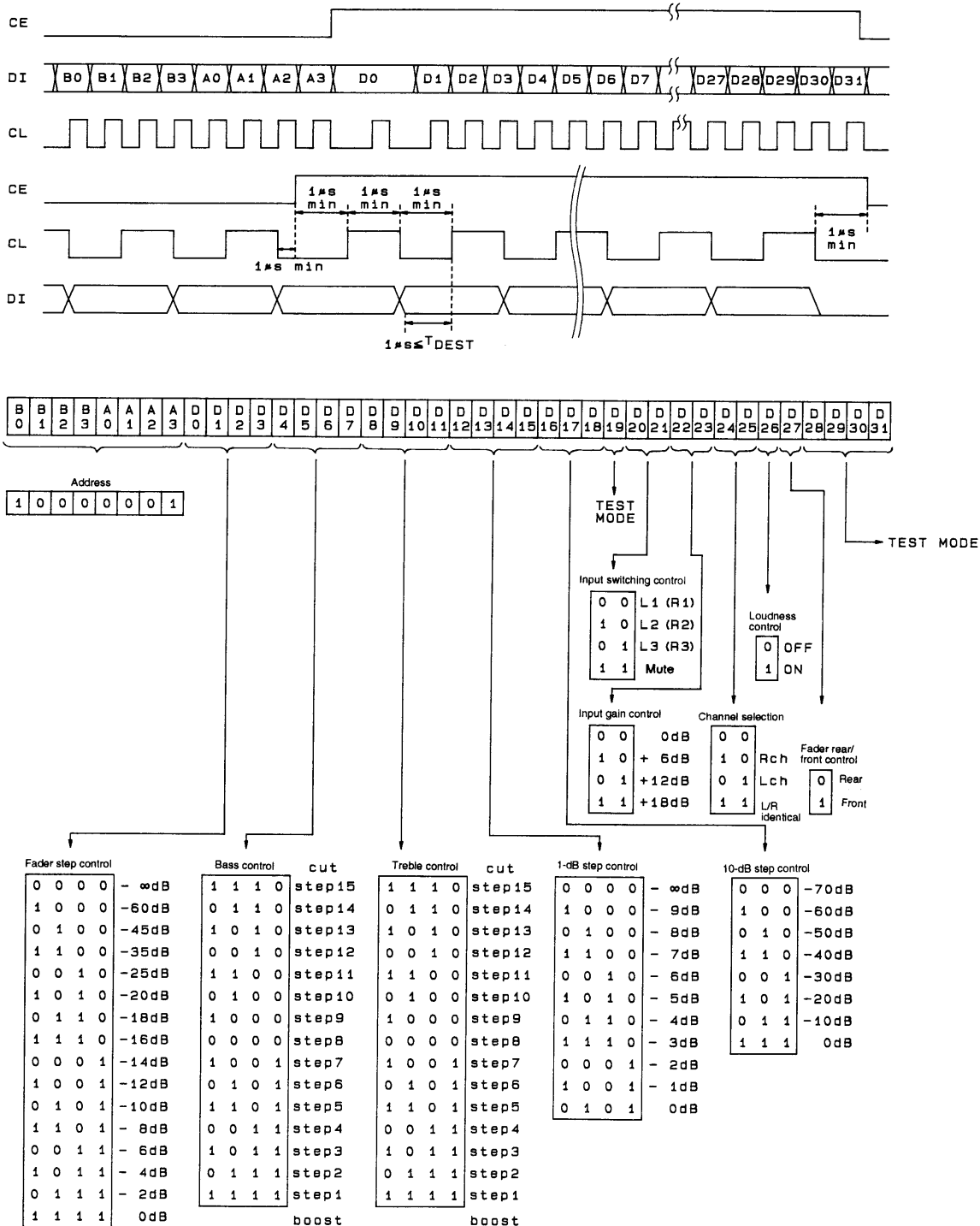


Figure 1

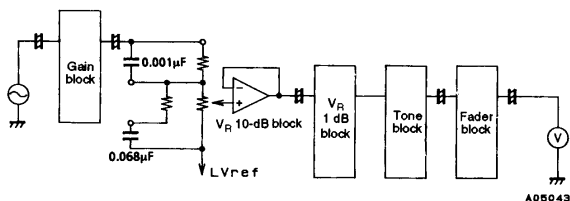
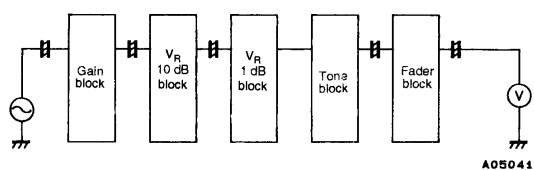
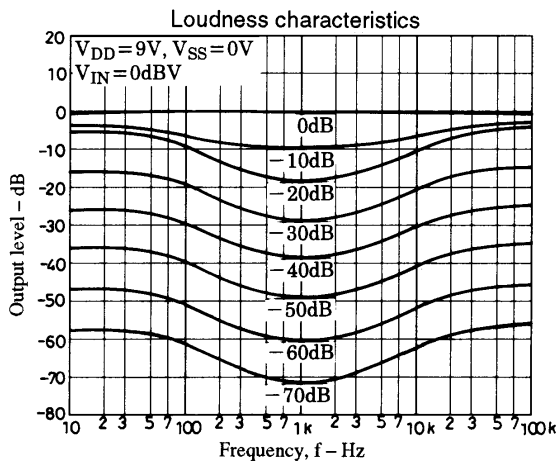
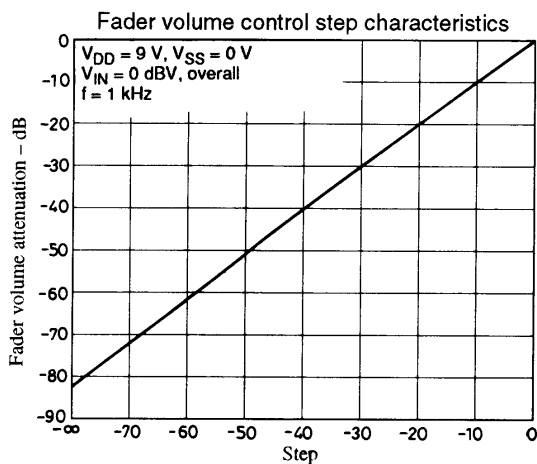
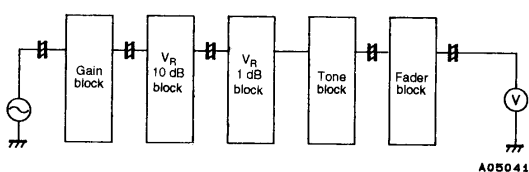
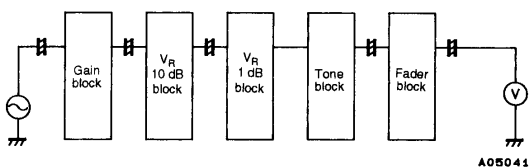
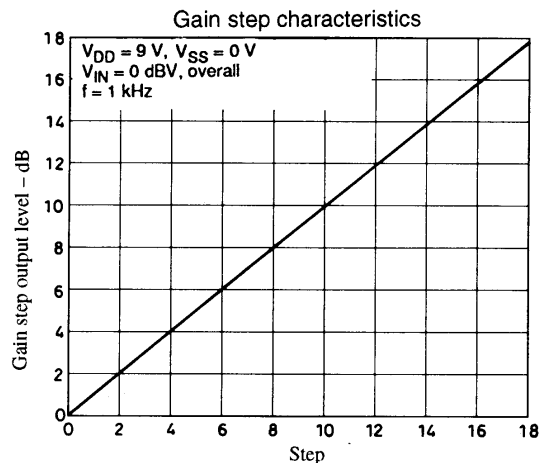
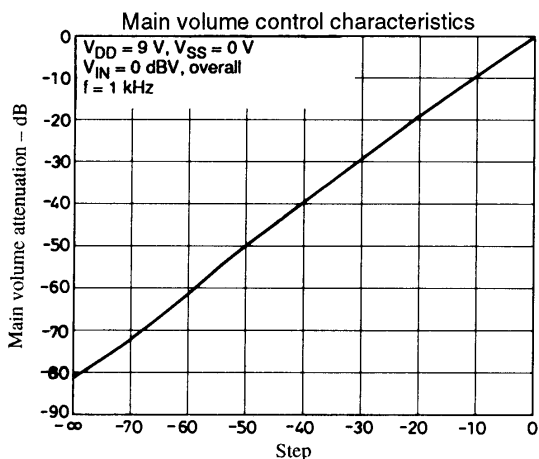
Control System Timing and Data Format

The LC75372E is controlled by applying data in the stipulated format to the CE, CL, and DI pins. The data consists of 40 bits, of which 8 bits are the chip address and 32 bits are the data.

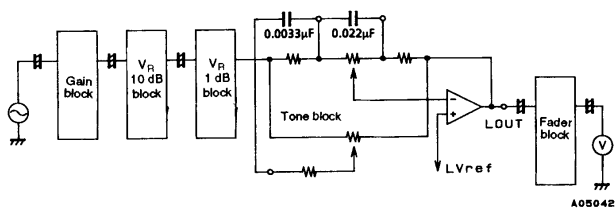
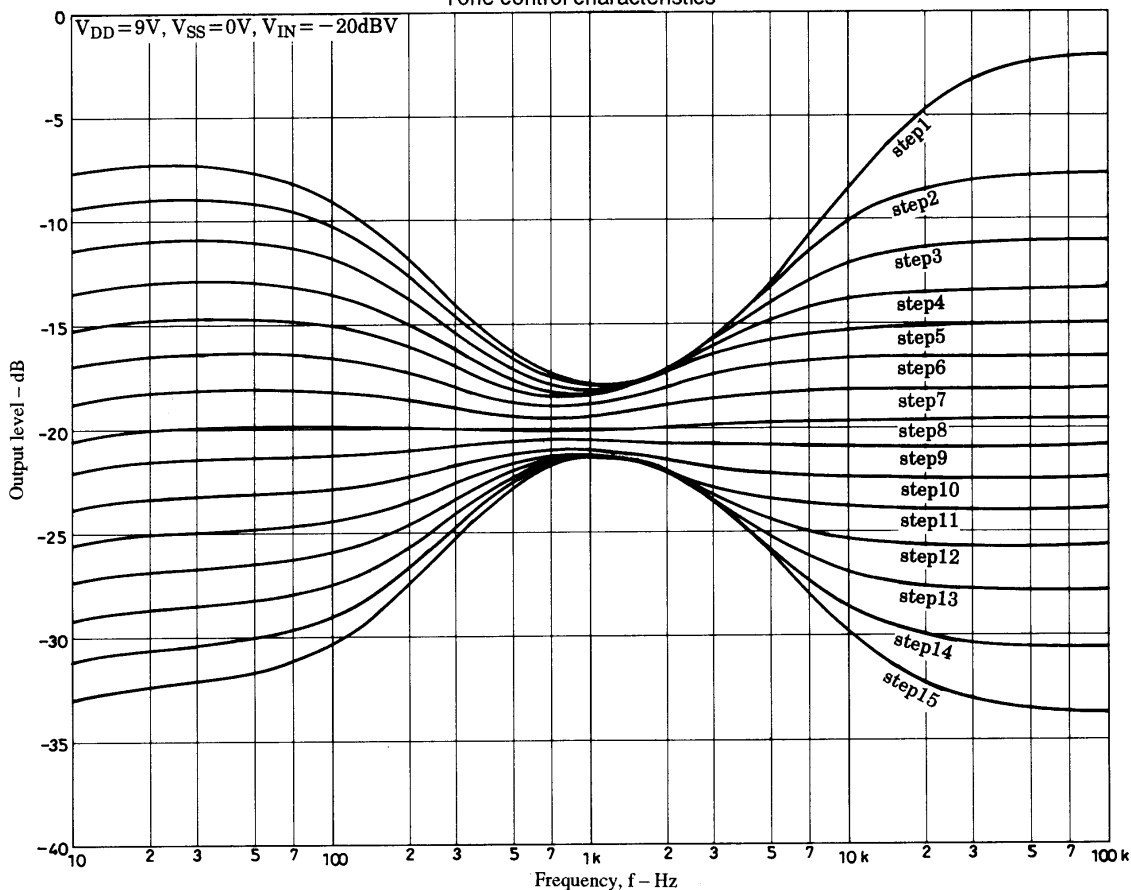


Note: The bits D19 and D28 to D31 are LSI test bits, and must be set to 0.

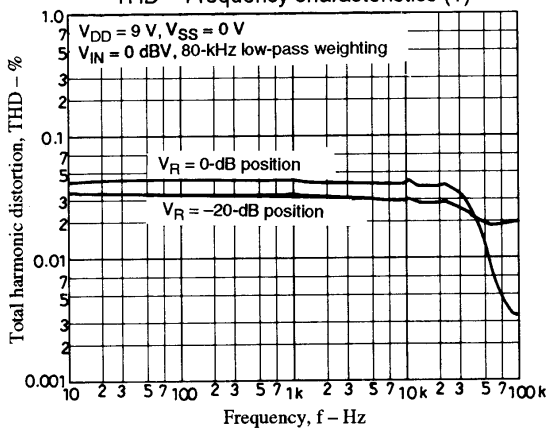
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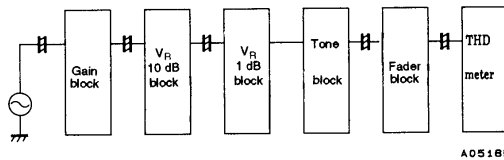
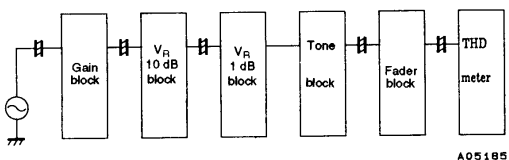
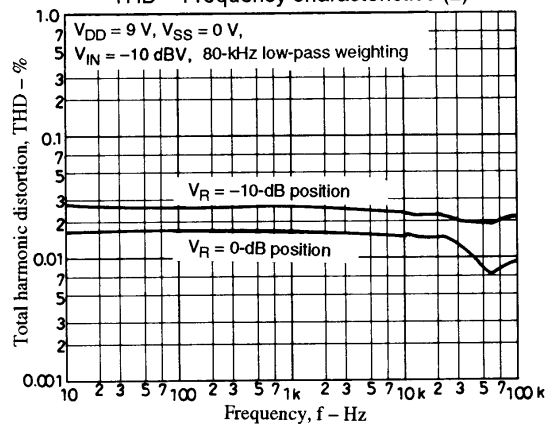
Tone control characteristics

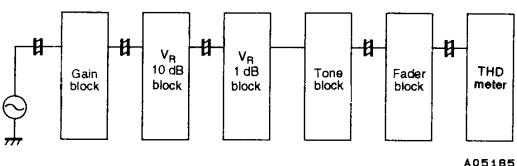
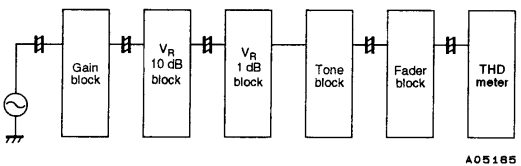
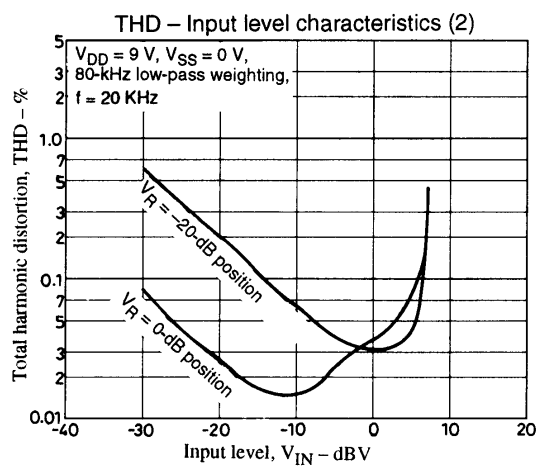
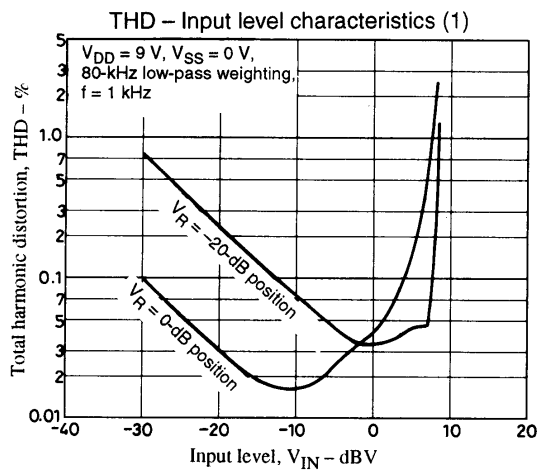
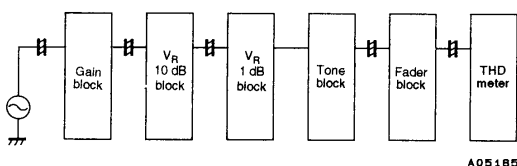
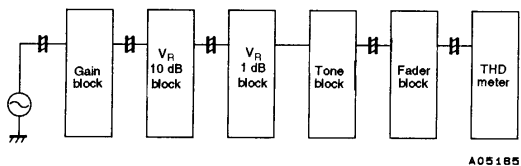
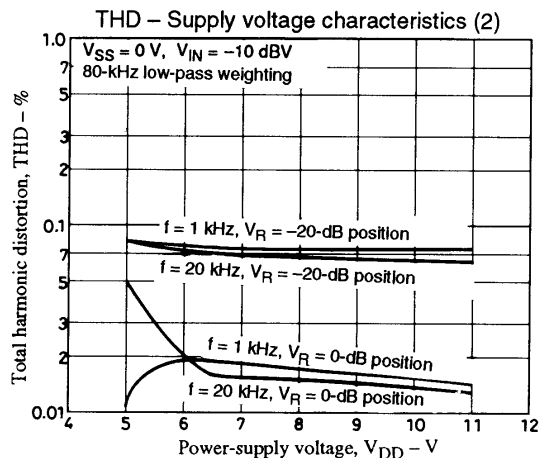
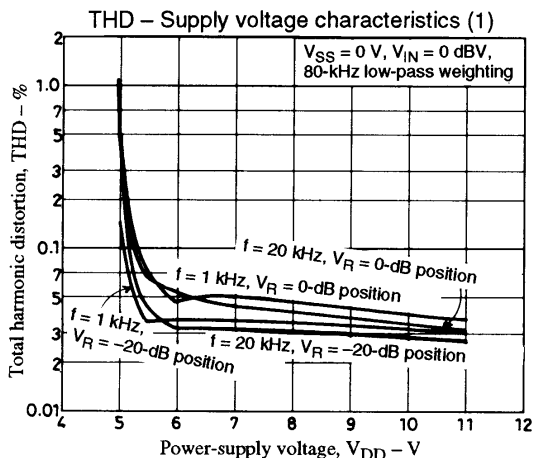


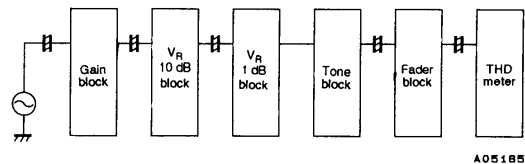
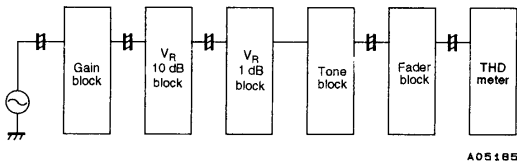
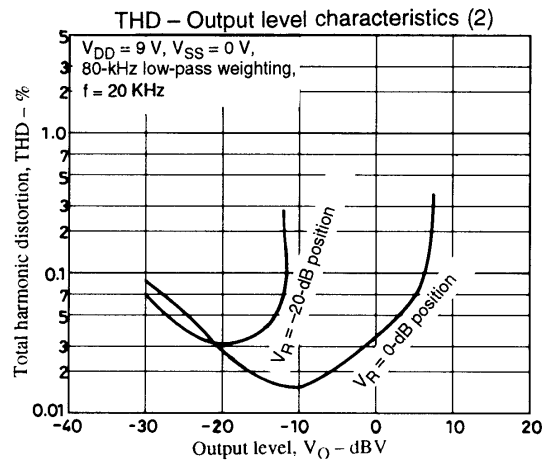
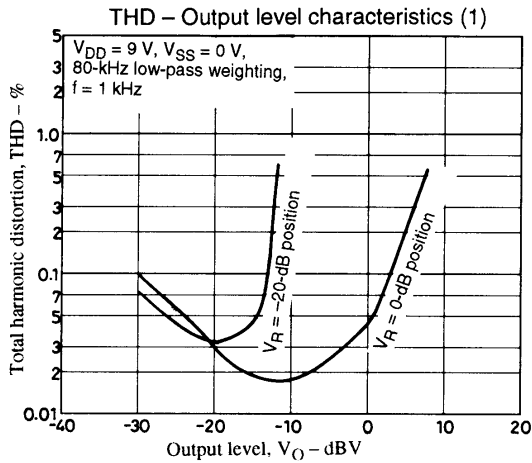
THD - Frequency characteristics (1)



THD - Frequency characteristics (2)







Usage Notes

1. The states of the internal analog switches are undefined when power is first applied. Use an external muting circuit or other technique to mute the outputs until correct control data has been set up in the LC75372E.
2. Either cover the lines connected to the CL, DI, and CE pins with the ground pattern or use shielded cable for those lines to prevent the high-frequency digital signals on those lines from entering the analog system.
3. Muting by input switching must be used in conjunction with the volume control setting when the maximum volume control attenuation (the VOL = $-\infty$ position) is used.

■ No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.

■ Anyone purchasing any products described or contained herein for an above-mentioned use shall:

- ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
- ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.

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