



## Specifications

### Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max	V <sub>DD</sub>	11	V
Maximum input voltage	V <sub>IN</sub> max	CL, DI, CE	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
Allowable power dissipation	Pd max	When Ta ≤ 85°C and mounted on a printed circuit board	720	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-50 to +125	°C

### Allowable Operating Ranges at Ta = -40 to +85°C, VSS = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V <sub>DD</sub>	V <sub>DD</sub>	7.5		9.7	V
High-level input voltage	V <sub>IH</sub>	CL, DI, CE	4.0		V <sub>DD</sub>	V
Low-level input voltage	V <sub>IL</sub>	CL, DI, CE	V <sub>SS</sub>		1.0	V
Input voltage amplitude	V <sub>IN</sub>	CL, DI, CE, LVRIN, RVRIN, L1 to L4, R1 to R4, LFIN, RFIN, LSIN, RSIN	V <sub>SS</sub>		V <sub>DD</sub>	Vp-p
Input pulse width	t <sub>φ</sub> W	CL	1			μs
Setup time	t <sub>setup</sub>	CL, DI, CE	1			μs
Hold time	t <sub>hold</sub>	CL, DI, CE	1			μs
Operating frequency	fopg	CL			500	kHz

### Electrical Characteristics at Ta = 25°C, VDD = 8 V, VSS = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Input Block]						
Maximum input gain	Gin max			+18.75		dB
Step resolution	Gstep			+1.25		dB
Output load resistance	R <sub>L</sub>		10			kΩ
Output impedance	R <sub>O</sub>	LSEL0, RSEL0 : R <sub>L</sub> = 10 kΩ, f = 1 kHz, V <sub>IN</sub> = 1 Vrms		46		Ω
[Output Block]						
Maximum output gain	Gout max			+8.5		dB
Output load resistance	R <sub>L</sub>		10			kΩ
Output impedance	R <sub>O</sub>	LFOUT, LROUT, RFOUT, RROUT : R <sub>L</sub> = 10 kΩ, f = 1 kHz, V <sub>IN</sub> = 1 Vrms		35		Ω
[Volume Control Block]						
Step resolution	ATstep			1		dB
Step error	ATerr	STEP = 0 dB to -20 dB	-1	0	+1	dB
		STEP = -20 dB to -50 dB	-3	0	+3	dB
Output load resistance	R <sub>L</sub>		10			kΩ
Output impedance	R <sub>O</sub>	LTOUT, RTOUT : R <sub>L</sub> = 10 kΩ, f = 1 kHz, V <sub>IN</sub> = 1 Vrms		46		Ω
[Fader Volume Control Block]						
Step resolution	ATstep	STEP = 0 dB to -20 dB		2		dB
		STEP = -20 dB to -25 dB		5		dB
		STEP = -25 dB to -45 dB		10		dB
Step error	ATerr	STEP = 0 dB to -45 dB	-2	0	+2	dB
		STEP = -45 dB to -60 dB	-3	0	+3	dB
Output load resistance	R <sub>L</sub>		10			kΩ
Output impedance	R <sub>O</sub>	LFOUT, LROUT, RFOUT, RROUT : R <sub>L</sub> = 10 kΩ, f = 1 kHz, V <sub>IN</sub> = 1 Vrms		46		Ω
[Bass and Treble Control Block]						
Bass control range	Gbass	Max. Boost/Cut	±8	±11.9	±13	dB
Treble control range	Gtre	Max. Boost/Cut	±8	±11.9	±13	dB
Output load resistance	R <sub>L</sub>		10			kΩ
Output impedance	R <sub>O</sub>	LTOUT, RTOUT : R <sub>L</sub> = 10 kΩ, f = 1 kHz, V <sub>IN</sub> = 1 Vrms		46		Ω

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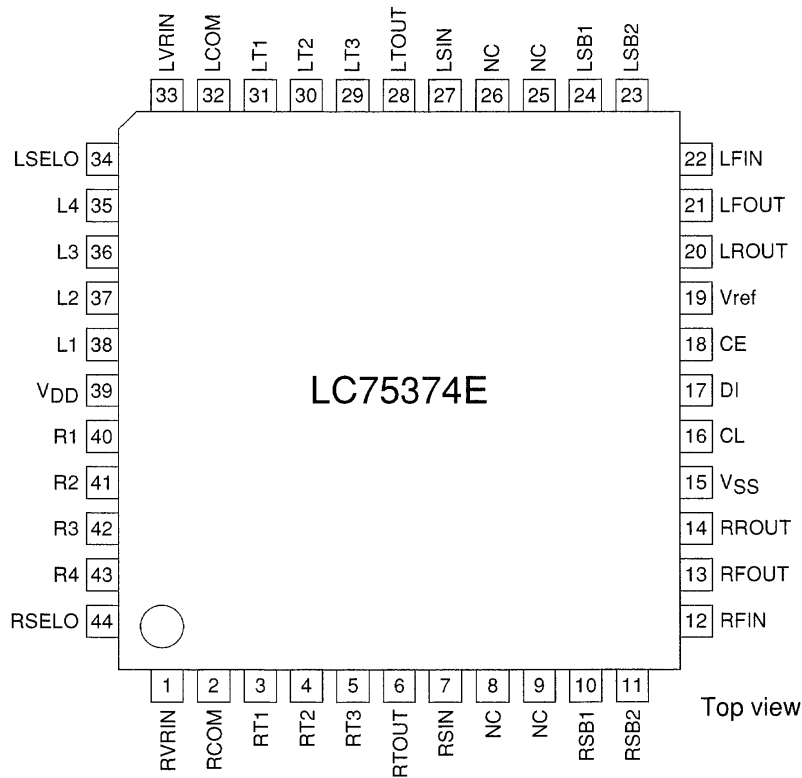
## LC75374E

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### Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{DD} = 8\text{ V}$ , $V_{SS} = 0\text{ V}$

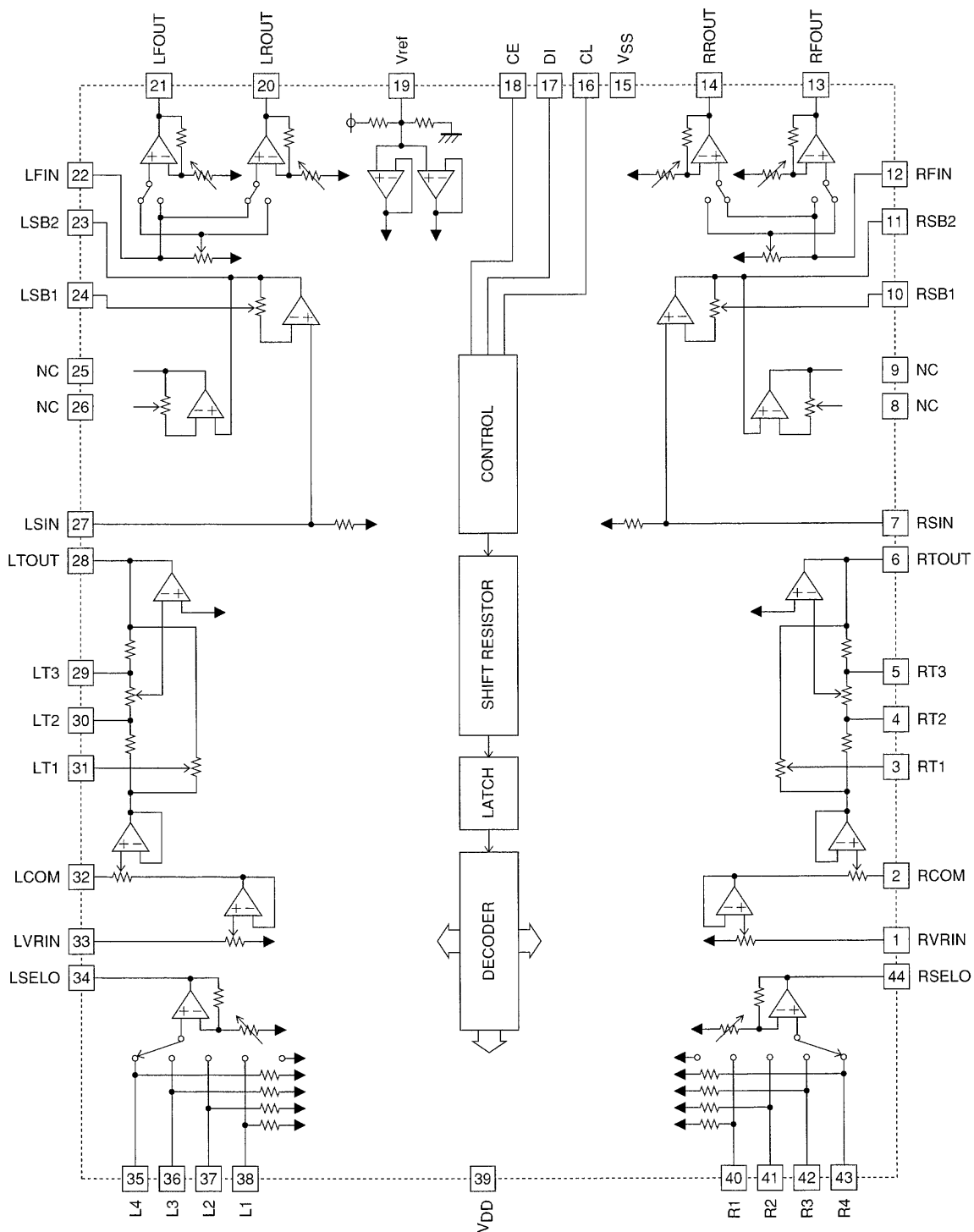
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Super-Bass Block] (T type)						
Control range	Crange	Max. Boost		+20		dB
Step resolution	ATstep			+2.0		dB
Output load resistance	$R_L$		10			$k\Omega$
Output impedance	$R_O$	LSB2, RSB2 : $R_L = 10\text{ k}\Omega$ , $f = 1\text{ kHz}$ , $V_{IN} = 1\text{ V}_{rms}$		70		$\Omega$
[Overall]						
Total harmonic distortion	THD	$V_{IN} = 1\text{ V}_{rms}$ , $f = 1\text{ kHz}$ , All controls flat overall		0.003	0.01	%
Crosstalk	CT	$V_{IN} = 1\text{ V}_{rms}$ , $f = 1\text{ kHz}$ , All controls flat overall, $R_g = 1\text{ k}\Omega$		80.5		dB
Output at maximum attenuation	$V_o\text{ min}$	$V_{IN} = 1\text{ V}_{rms}$ , $f = 1\text{ kHz}$ , Main volume setting: $-\infty$		-80		dB
Output noise voltage	$V_{N1}$	All controls flat overall, (IHF-A), $R_g = 1\text{ k}\Omega$		8		$\mu\text{V}$
	$V_{N2}$	All controls flat overall, (DIN-AUDIO), $R_g = 1\text{ k}\Omega$		10		$\mu\text{V}$
High-level input voltage	$I_{IH}$	CL, DI, CE, $V_{IN} = 8\text{ V}$			10	$\mu\text{A}$
Low-level input voltage	$I_{IL}$	CL, DI, CE, $V_{IN} = 0\text{ V}$	-10			$\mu\text{A}$

### Pin Assignment



A10540

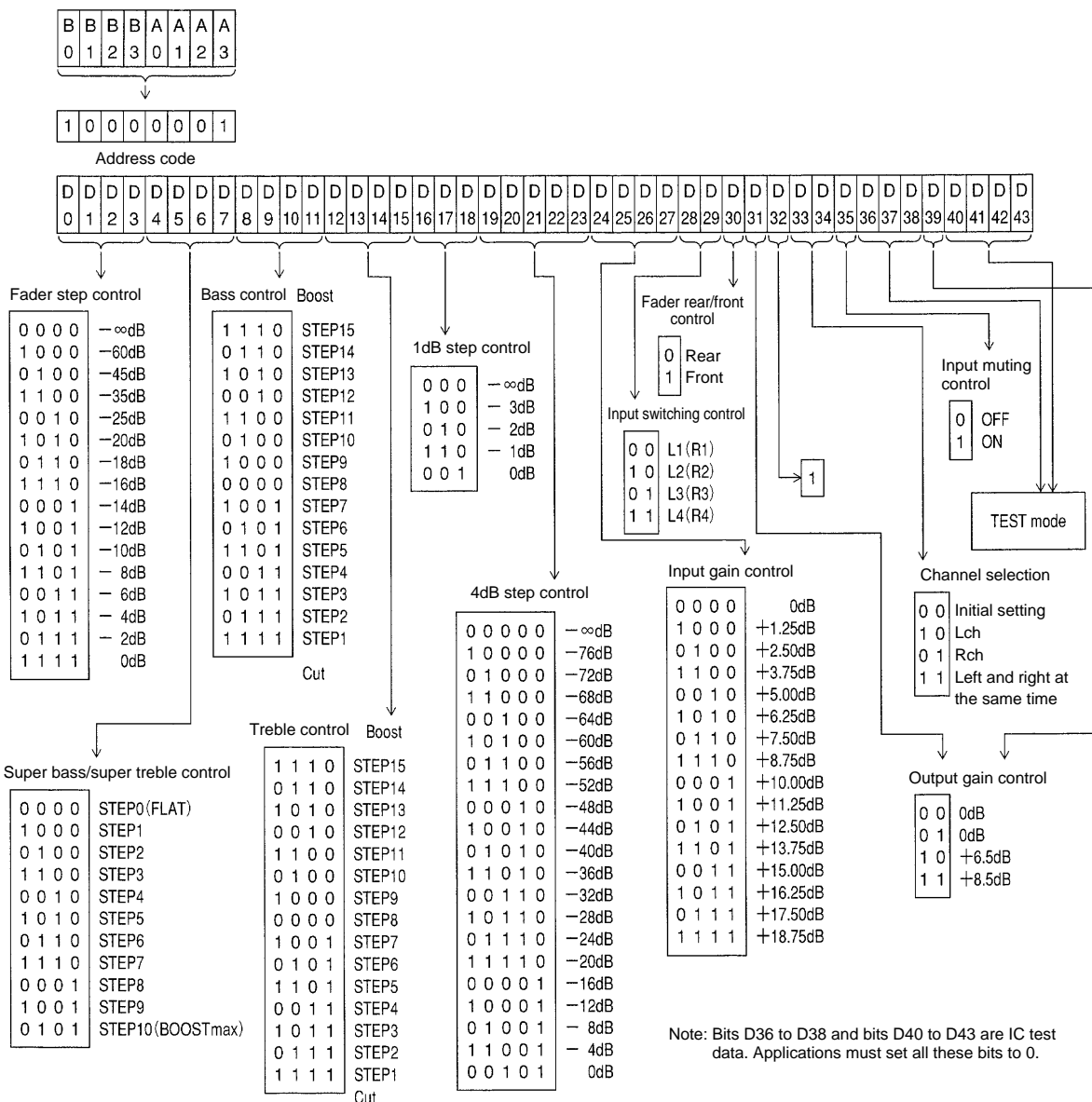
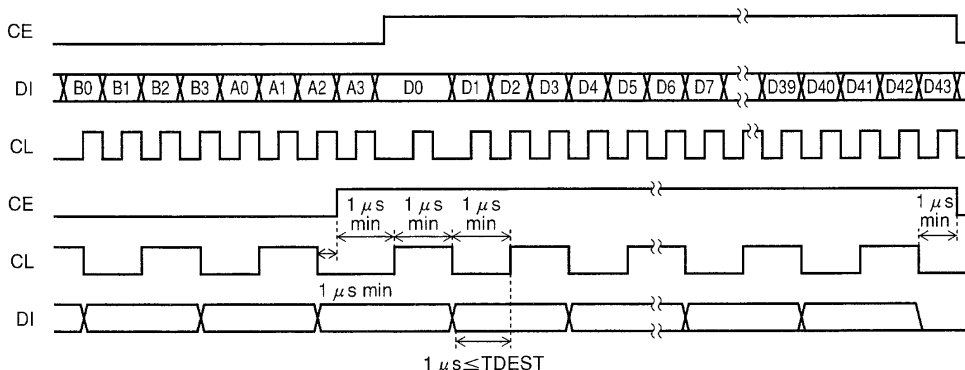
Equivalent Circuit



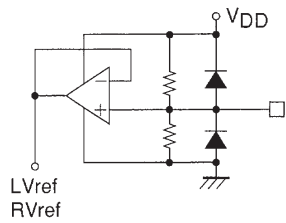
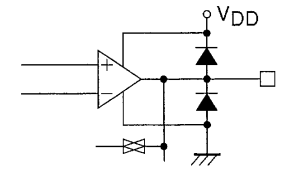
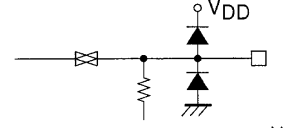
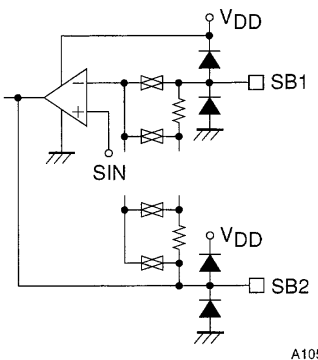
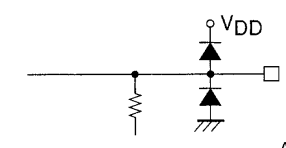
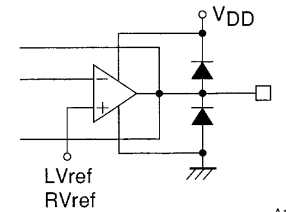
A10541

**Control System Timing and Data Format**

Applications must input the stipulated serial data to the CE, CL, and DI pins to control the LC75374E. The data consists of a total of 52 bits, of which 8 bits are address and 44 bits are data.



Pin Functions

Pin No.	Pin	Description	Notes
19	Vref	<ul style="list-style-type: none"> <li>Supply voltage generator (<math>0.525 \times V_{DD}</math>) used for the analog ground. A capacitor must be connected between Vref and <math>V_{SS}</math> to remove power supply ripple.</li> </ul>	 <p>A10543</p>
20 21 14 13	LROUT LFOUT RROUT RFOUT	<ul style="list-style-type: none"> <li>Fader outputs. The front and rear outputs can be attenuated independently.</li> </ul>	 <p>A10544</p>
22 12	LFIN RFIN	<ul style="list-style-type: none"> <li>Fader inputs</li> <li>These inputs must be driven by low-impedance circuits.</li> </ul>	 <p>A10545</p>
24 23 10 11	LSB1 LSB2 RSB1 RSB2	<ul style="list-style-type: none"> <li>Left channel super bass compensation capacitor connection</li> <li>Left channel super bass output and compensation capacitor connection</li> <li>Right channel super bass compensation capacitor connection</li> <li>Right channel super bass output and compensation capacitor connection</li> </ul>	 <p>A10547</p>
22 7	LSIN RSIN	<ul style="list-style-type: none"> <li>Super bass input</li> <li>These inputs must be driven by low-impedance circuits.</li> </ul>	 <p>A10548</p>
28 6	LTOUT RTOUT	<ul style="list-style-type: none"> <li>Tone control outputs</li> </ul>	 <p>A10549</p>

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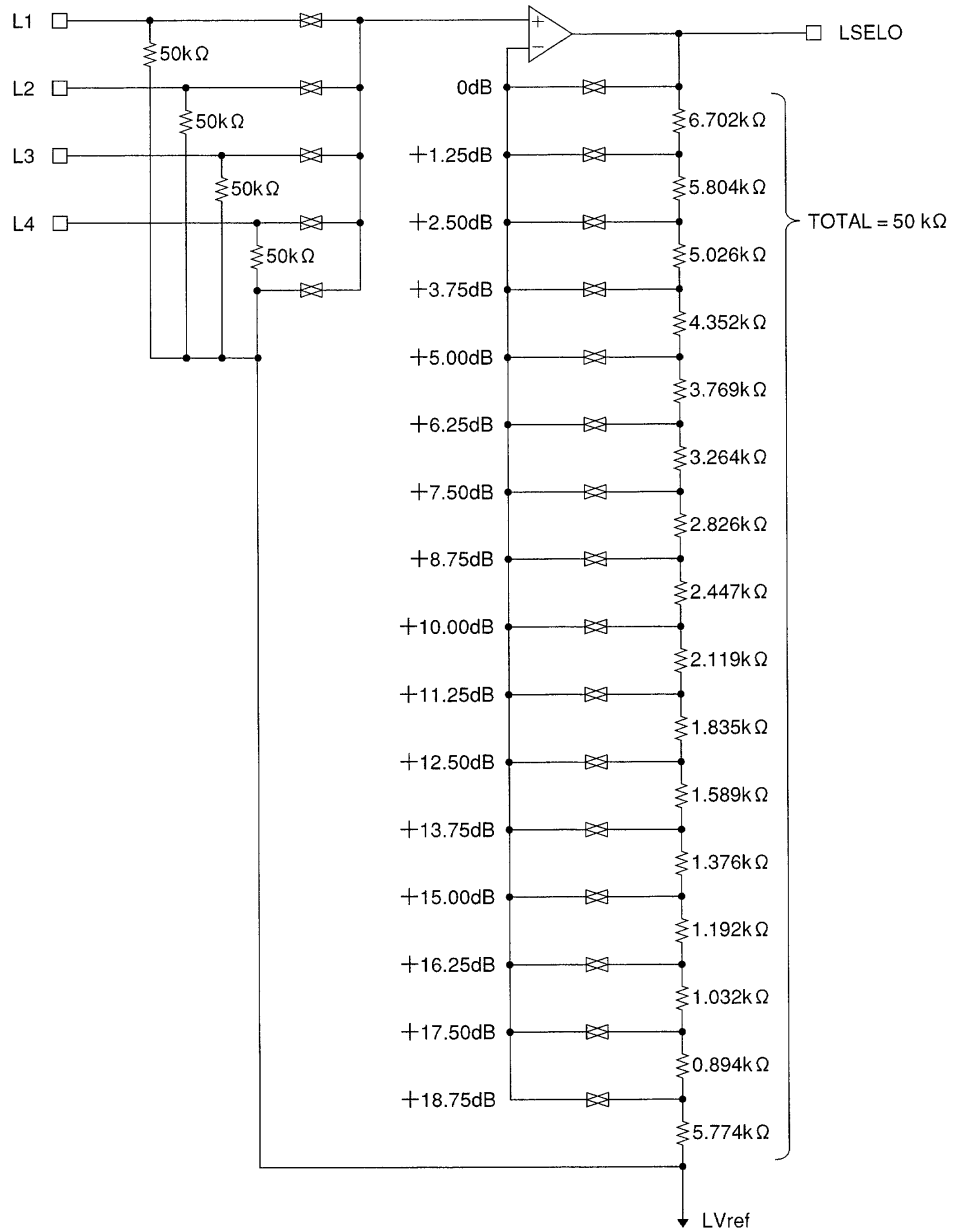
## LC75374E

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Pin No.	Pin	Description	Notes
31 30 29 3 4 5	LT1 LT2 LT3 RT1 RT2 RT3	<ul style="list-style-type: none"> <li>Tone control circuit bass and treble compensation capacitor connections.</li> </ul> <p>Connect the high band compensation capacitors between the pins T1 and T2.</p> <p>Connect the low band compensation capacitors between the pins T2 and T3.</p>	<p style="text-align: right;">A10550</p>
32 2	LCOM RCOM	<ul style="list-style-type: none"> <li>1dB volume control common connections</li> </ul>	<p style="text-align: right;">A10551</p>
33 1	LVRIN RVRIN	<ul style="list-style-type: none"> <li>4dB volume control inputs</li> <li>These inputs must be driven by low-impedance circuits.</li> </ul>	<p style="text-align: right;">A10552</p>
34 44	LSEL0 RSEL0	<ul style="list-style-type: none"> <li>Input selector outputs</li> </ul>	<p style="text-align: right;">A10553</p>
38 37 36 35 40 41 42 43	L1 L2 L3 L4 R1 R2 R3 R4	<ul style="list-style-type: none"> <li>Signal inputs</li> </ul>	<p style="text-align: right;">A10554</p>
39	V <sub>DD</sub>	<ul style="list-style-type: none"> <li>Power supply</li> </ul>	
15	V <sub>SS</sub>	<ul style="list-style-type: none"> <li>Ground</li> </ul>	
16 17	CL DI	<ul style="list-style-type: none"> <li>Serial data and clock inputs used for transferring control data</li> </ul>	
18	CE	<ul style="list-style-type: none"> <li>Chip enable input. Data is written into the internal latches and the analog switches operate when this pin goes from high to low. Data transfers are enabled when this pin is high.</li> </ul>	<p style="text-align: right;">A10555</p>
8, 26 9, 25	NC	<ul style="list-style-type: none"> <li>Unused pins. These pins must be connected to V<sub>SS</sub>.</li> <li>Unused pins. These pins must be left open.</li> </ul>	

# LC75374E

## Input Block Equivalent Circuit

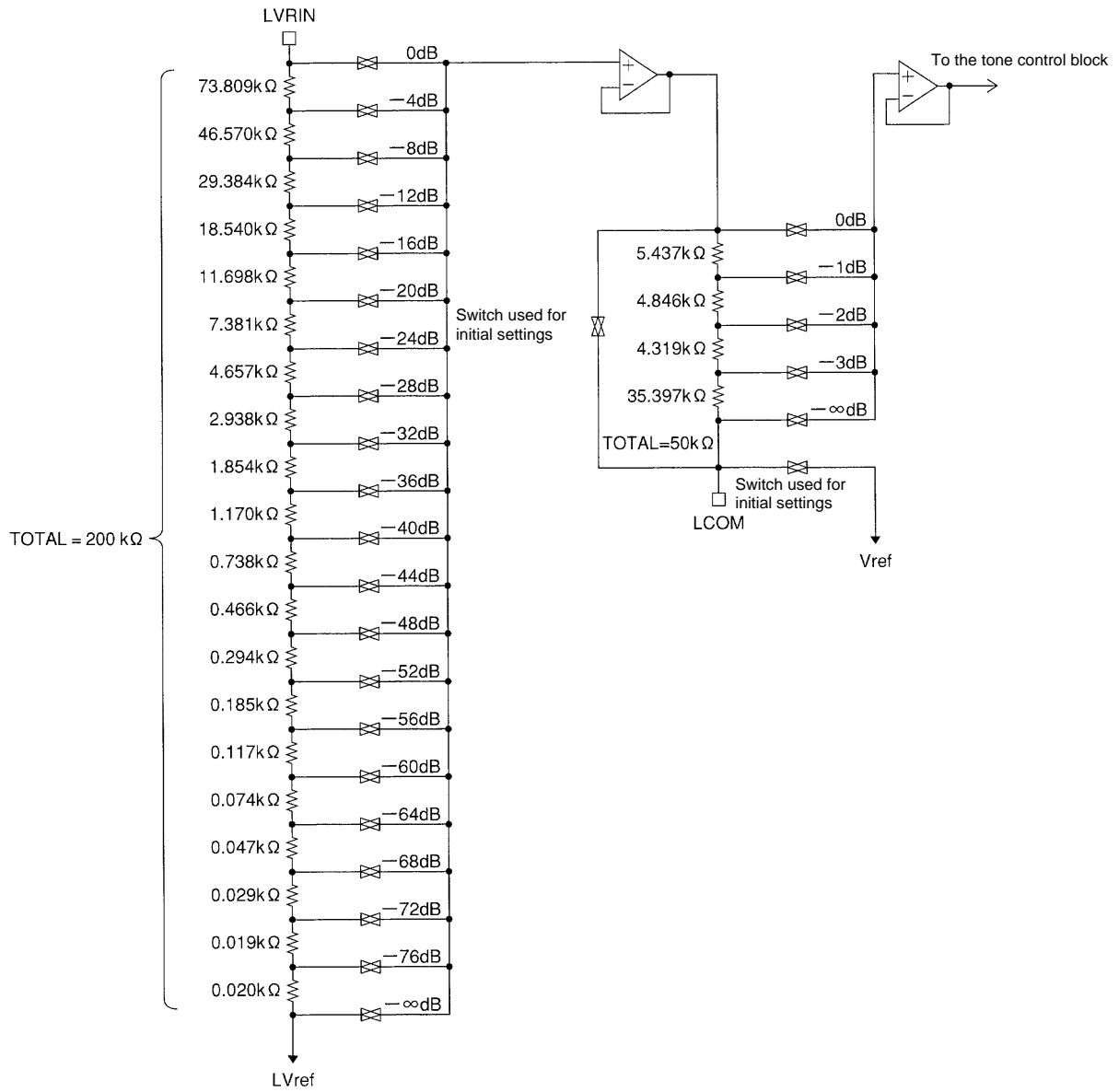


A10556

The right channel is identical.



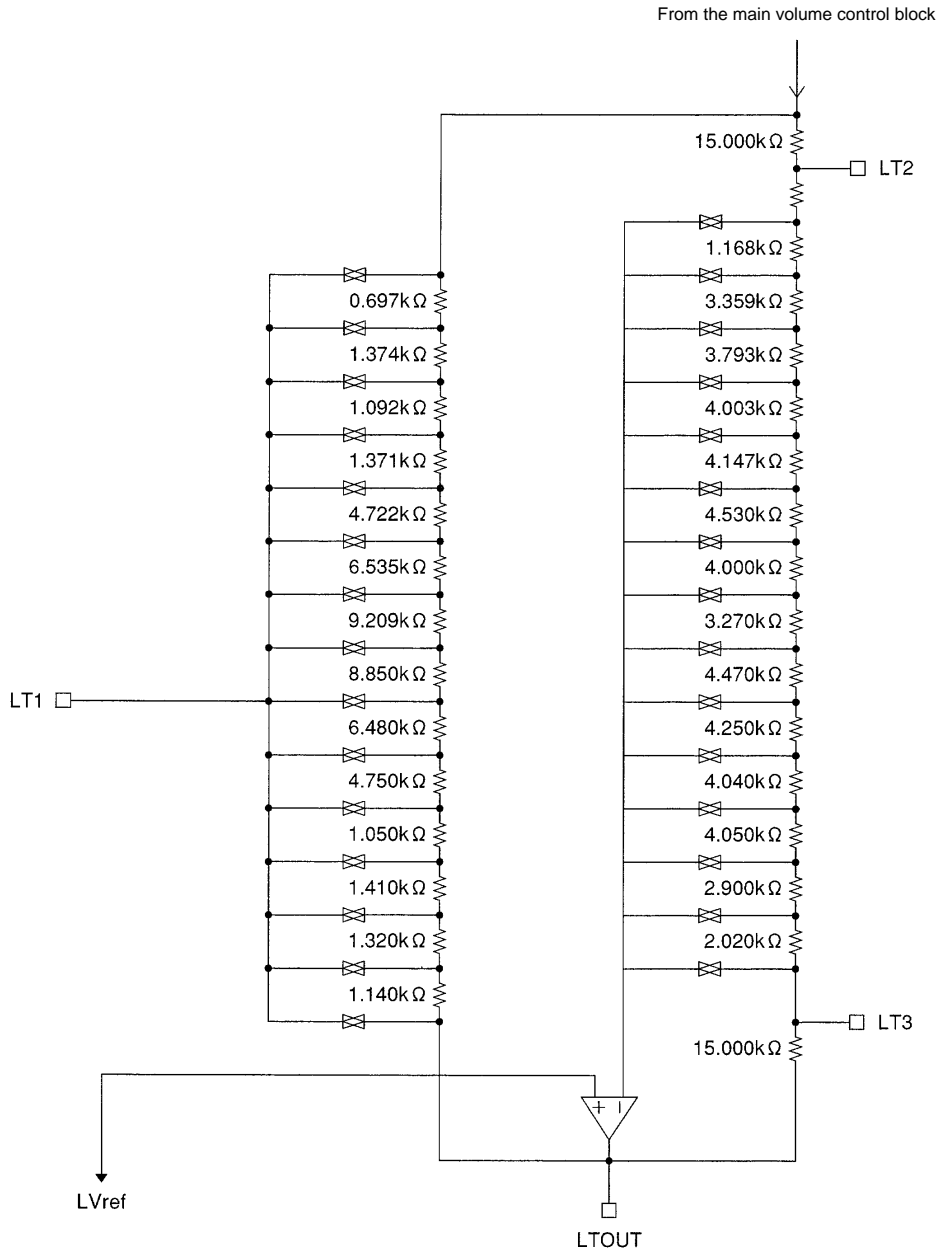
Main Volume Control Block Equivalent Circuit



A10557

The right channel is identical.

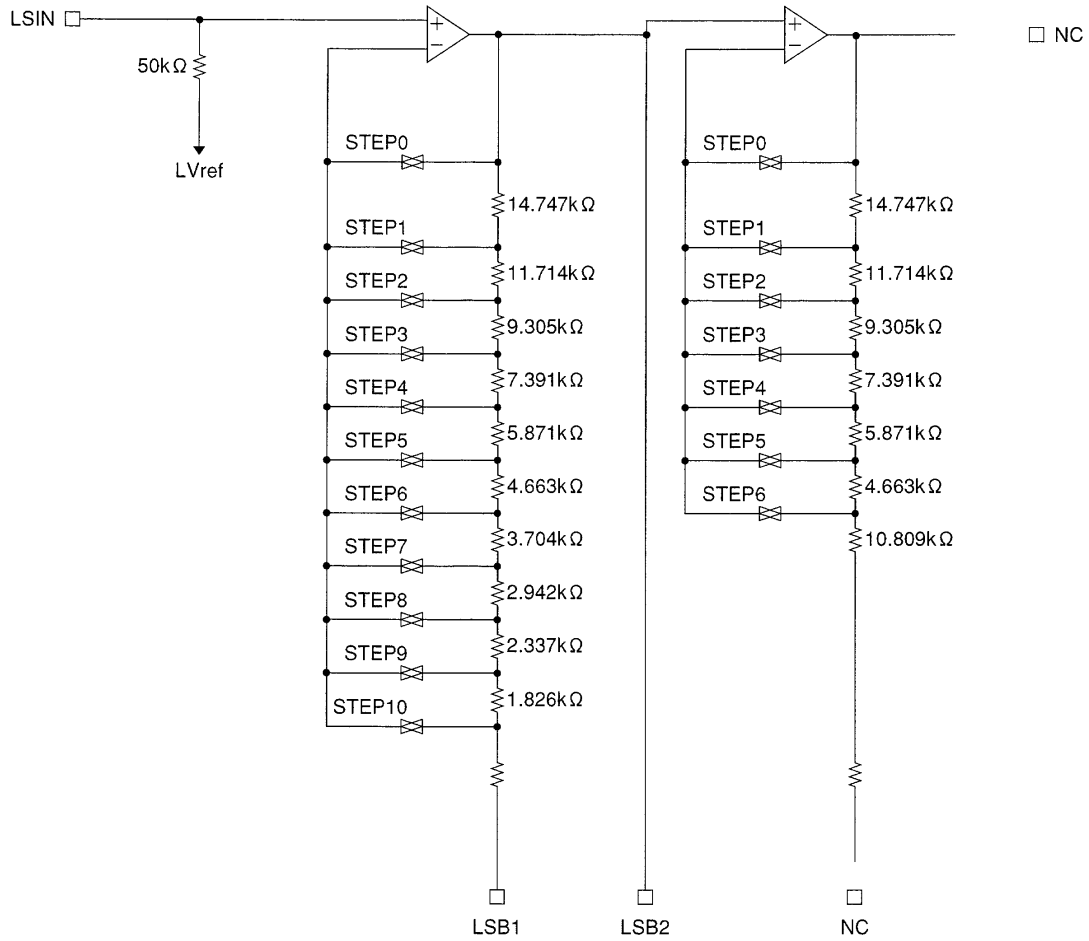
Tone Block Equivalent Circuit



A10558

The right channel is identical.

Super Bass Block Equivalent Circuit



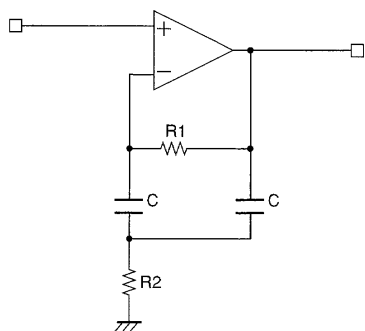
A10559

The right channel is identical.

**Sample external constant calculations for the super bass (T type) circuit when full boost is used**

The external constants required when full boost is used with the super bass block (T type) are calculated as follows.

- Super bass (T type) equivalent circuit



A10560

Sample calculation

Assume:

R1 = 64.5 kΩ, and

G = 20.65 dB, and

f0 = 72.7 Hz.

- Calculation

(1) Center frequency

$$f_0 = \frac{1}{2 \times \pi \times \sqrt{R_1 \times R_2 \times C \times C}}$$

(2) Gain

$$G = 20 \log \left( 1 + \frac{R_1}{2 \times R_2} \right)$$

(3) Q

$$Q = \frac{C \times C \times R_1}{2 \times C} \times \frac{1}{\sqrt{R_1 \times R_2 \times C \times C}}$$

- Determine R2

Determine R2 from formula (2).

$$R_2 = \frac{64.5}{2 \times (10.78 - 1)} \approx 3.3 \text{ (k}\Omega\text{)}$$

- Determine C

Determine C from formula (1).

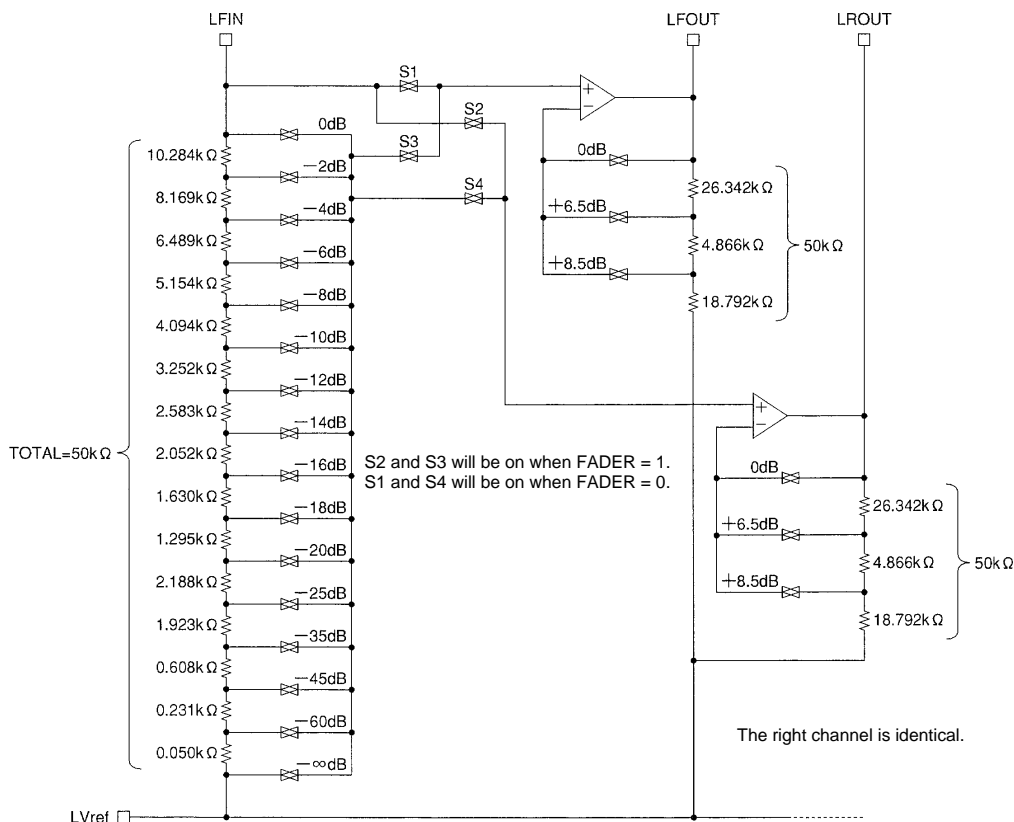
$$C = \frac{1}{\sqrt{R_1 \times R_2 \times (2 \times \pi \times f_0) \times (2 \times \pi \times f_0)}} \approx 0.15 \text{ (}\mu\text{F)}$$

- Determine Q

Determine Q from formula (3).

Here, Q will be 2.21.

**Fader Volume Control Block Equivalent Circuit**



S2 and S3 will be on when FADER = 1.  
S1 and S4 will be on when FADER = 0.

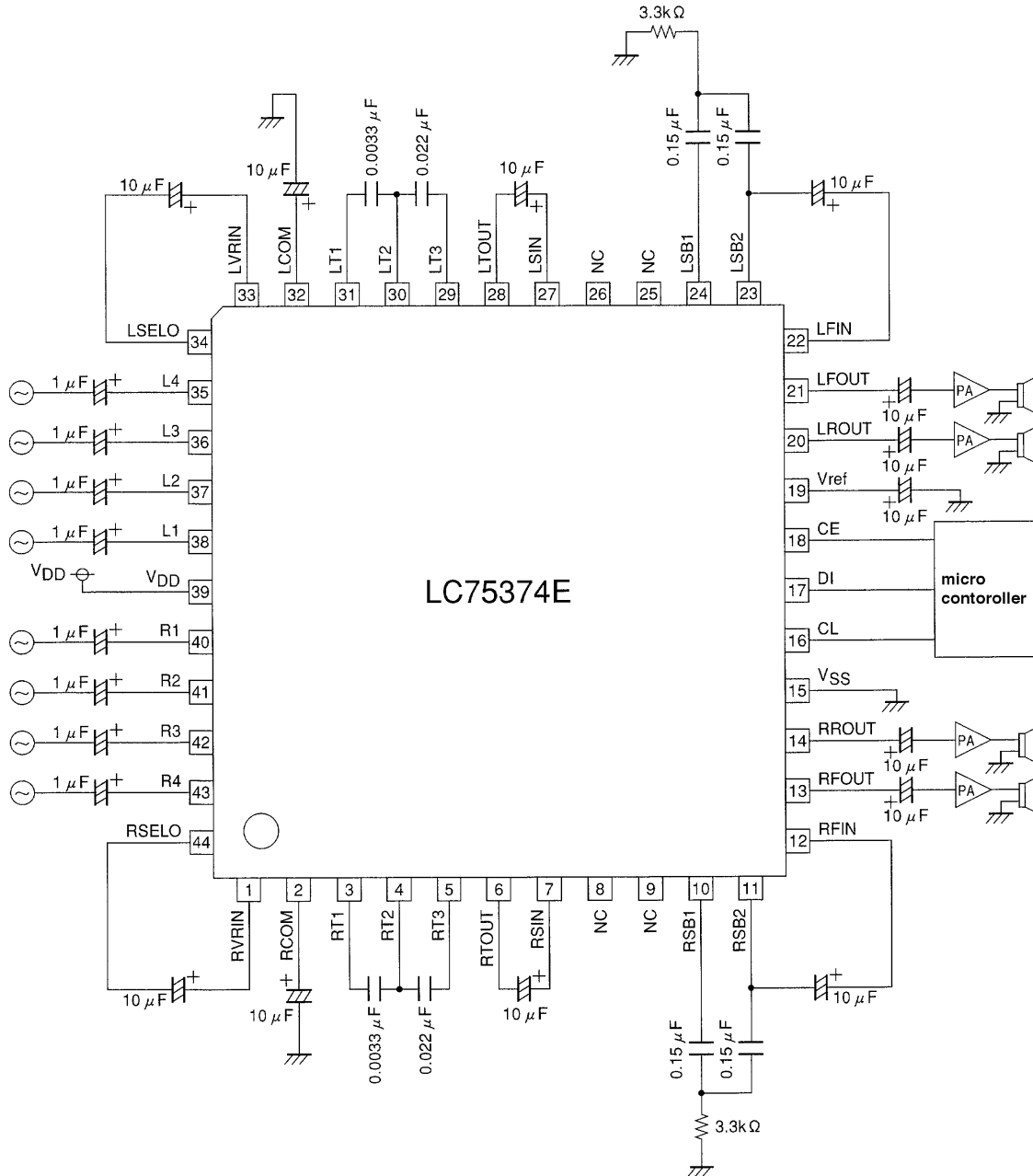
The right channel is identical.

A10561

At the point that data corresponding to  $-\infty$  is transferred to the 1dB -step main volume control block, S1 and S2 will go to the open state. S3 and S4 will go to the on state at the same time.

## LC75374E

### Sample Application Circuit

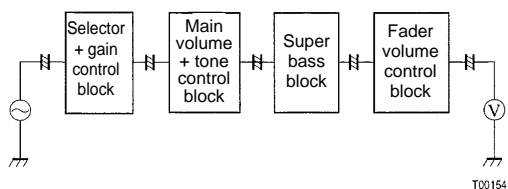
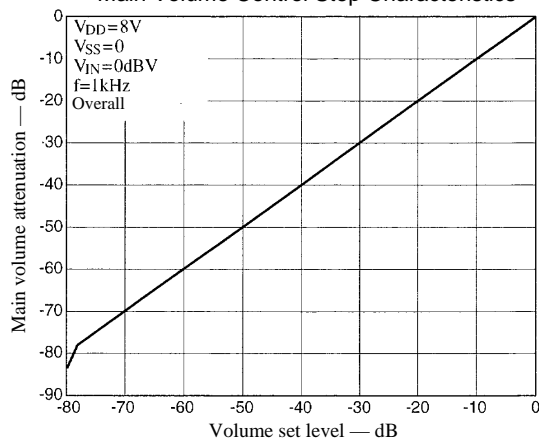


A10562

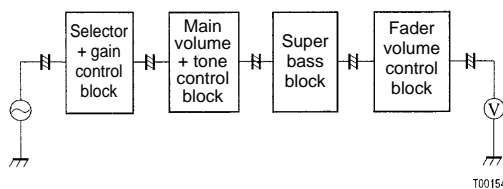
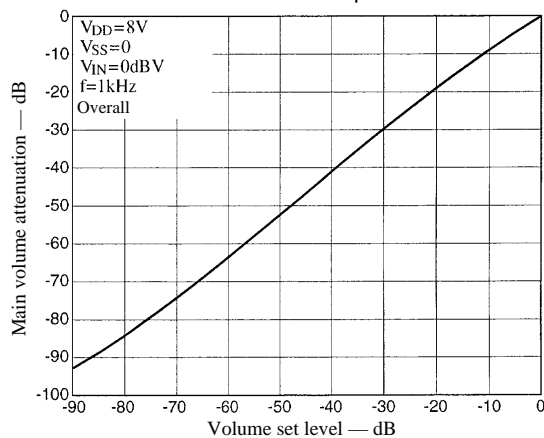
### Usage Notes

- The internal analog switches are in undefined states when power is first applied. Applications must therefore use external circuits to mute the output until control data has been transferred.
- When setting up the initial data after power is first applied, applications must first transfer a set of IC initialization data. This initialization data consists of an address field of (10000001) and a data field of all zeros (D0 to D4 = 0). Applications must only send the actual initial data after this initialization data has been sent.
- Applications must either cover the CL, DI, and CE lines with the ground pattern or use shielded cables for these lines to prevent the high-frequency digital signals that are transmitted over these lines from entering the analog signal system.

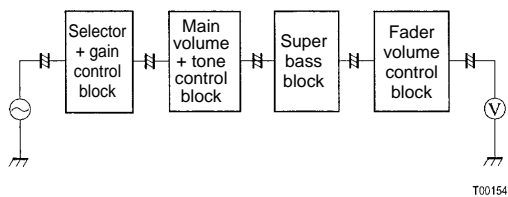
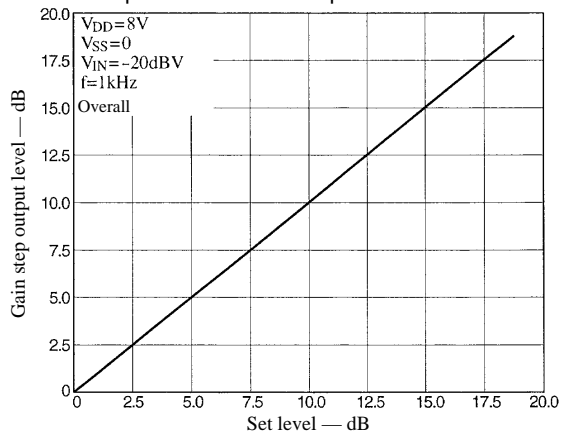
Main Volume Control Step Characteristics



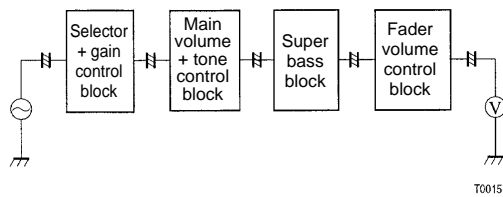
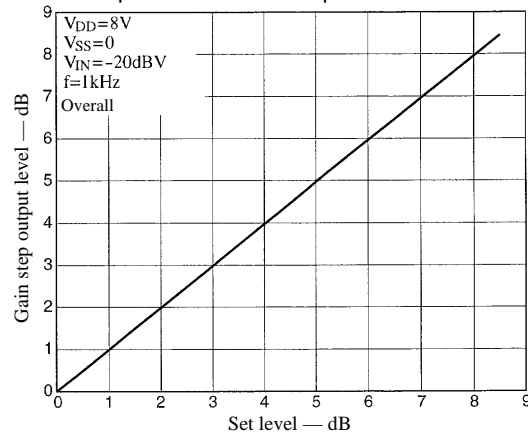
Fader Volume Control Step Characteristics



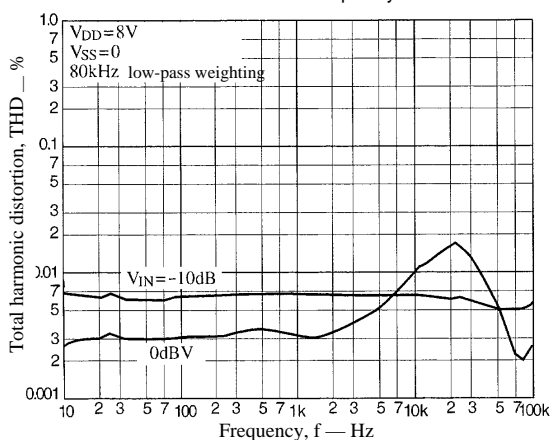
Input Gain Control Step Characteristics



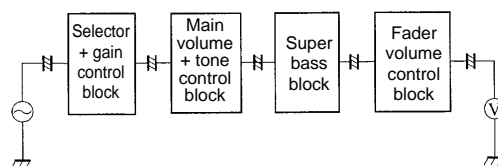
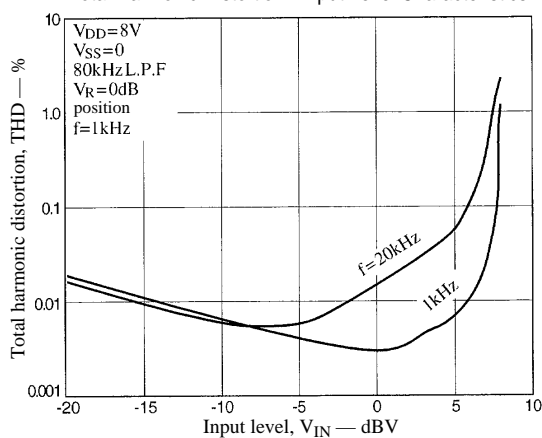
Output Gain Control Step Characteristics



Total Harmonic Distortion - Frequency Characteristics

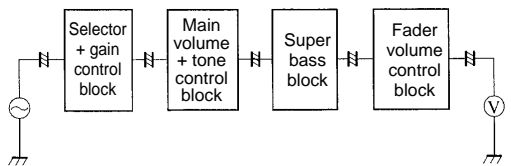
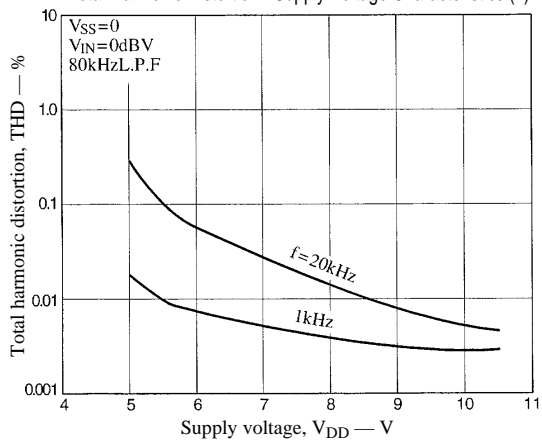


Total Harmonic Distortion - Input Level Characteristics



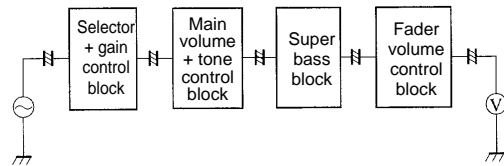
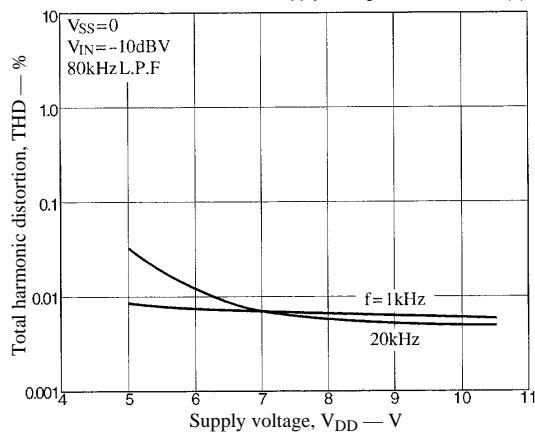
T00154

Total Harmonic Distortion - Supply Voltage Characteristics (1)



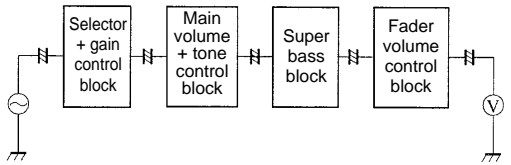
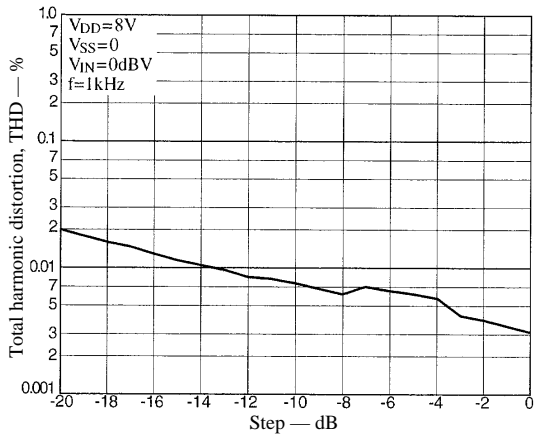
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Total Harmonic Distortion - Supply Voltage Characteristics (2)



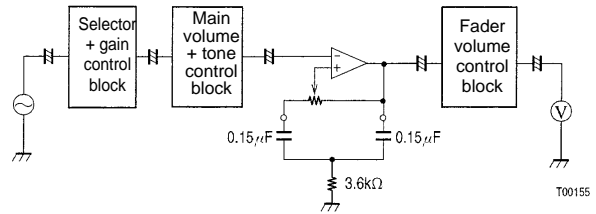
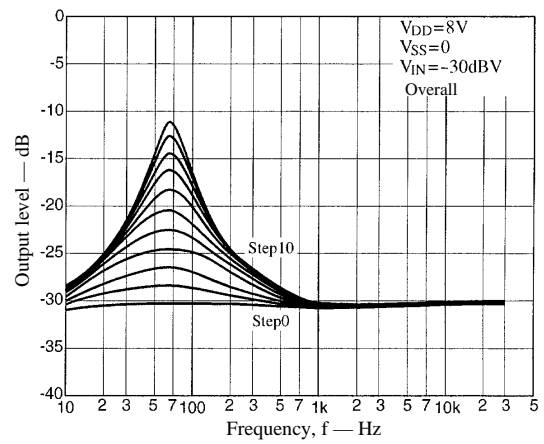
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Total Harmonic Distortion – Main Volume Control Step Characteristics



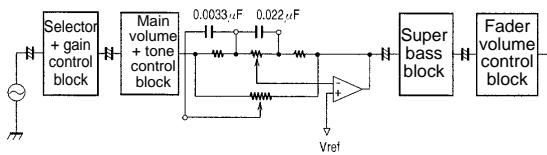
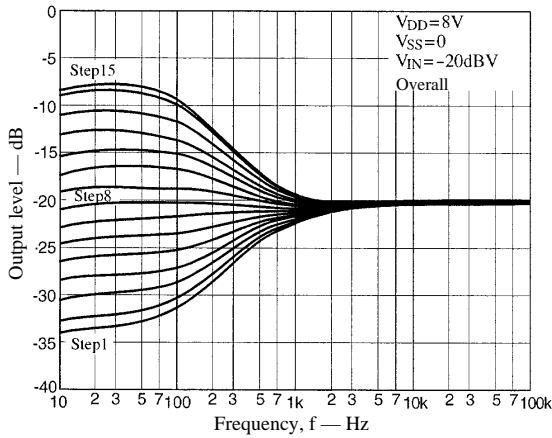
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Super Bass Characteristics



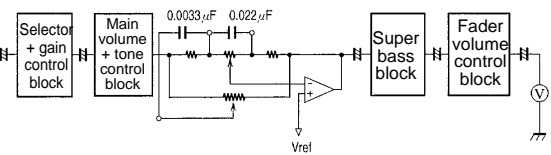
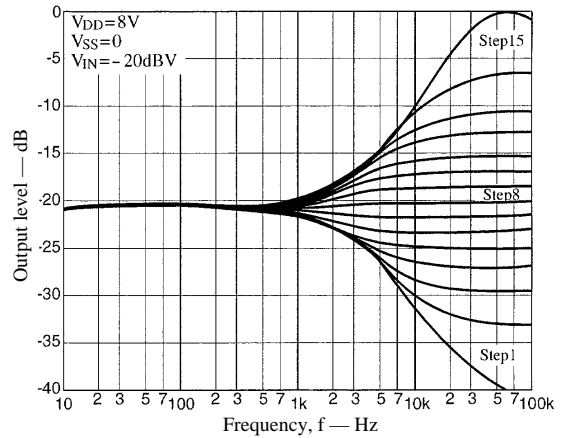
T00155

Bass Characteristics



T00156

Treble Characteristics



T00156



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