

Single Chip Electronic Volume and Tone Control System



LC75397E

Overview

The LC75397 is an electronic volume control system providing control over volume, balance, 4-band equalizer, bass, and input switching based on serial inputs.

Functions

• Volume control:

The chip provides 81 levels of volume attenuation: in 1-dB step between 0 dB and -79 dB and $-\infty$.

This circuit can control a total of 5 independent channels.

• Equalizer:

The chip provides control in 2-dB steps over the range between +10 dB and -10 dB. Three of the four bands have peaking equalization; the remaining one, shelving equalization.

• Selector:

The left and right channels each offer a choice of six inputs. The L6 and R6 inputs can be turned on and off independently. An external constant determines the amplification for the input signal.

• Input gain:

The input signal can be amplified by 0 to +30 dB in 2-dB steps.

• Bass control:

The bass can be controlled over a $\pm 10 \text{ dB}$ range in 2-dB steps.

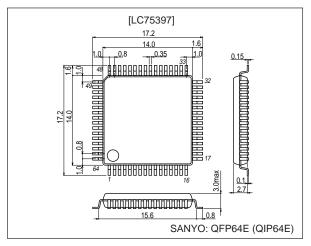
Features

- Built-in buffer amplifiers reduce the number of external parts required.
- Silicon gate CMOS process reduces the noise of built-in switch.
- Built-in analog ground reference voltage generator circuit
- All functions are controlled by serial input data. This IC supports the CCB standard.

Package Dimensions

unit: mm

3159-QFP64E



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Specifications Absolute Maximum Ratings at Ta = 25°C, $V_{SS} = 0 V$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} max	V _{DD}	11	V
Maximum input voltage	V _{IN} max	CL, DI, CE, L1 to L6, R1 to R6, LTIN, RTIN, LVR1IN, RVR1IN, LVR2IN, RVR2IN, LVR3IN	V _{SS} – 0.3 to V _{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 75°C, with PC board*	1000	mW
Operating temperature	Topr		-30 to +75	°C
Storage temperature	Tstg		-40 to +125	°C

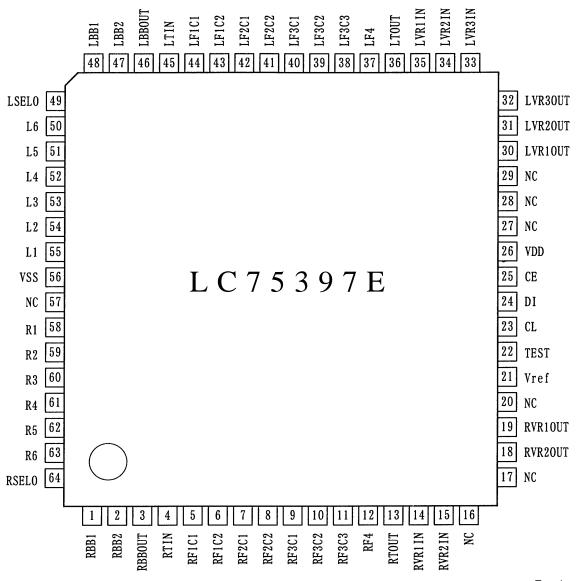
Note : * Printed circuit board size: 76.1 × 114.3 × 1.6 mm, printed circuit board material: glass/Epoxy resin

Allowable Operating Ranges at Ta=- 30 to + 75°C, V_{SS} = 0 V

Parameter	Symbol	Symbol Conditions -		Ratings				
Parameter	Symbol			typ	max	Unit		
Supply voltage	V _{DD}	V _{DD}	6.0		10.5	V		
Input high level voltage	V _{IH}	CL, DI, CE	4.0		V _{DD}	V		
Input low level voltage	VIL	CL, DI, CE	V _{SS}		1.0	V		
Input voltage amplitude	V _{IN}	CL, DI, CE, L1 to L6, R1 to R6, LTIN, RTIN, LVR1IN, RVR1IN, LVR2IN, RVR2IN, LVR3IN	V _{SS}		V _{DD}	Vp-p		
Input pulse width	t _{øW}	CL	1.0			μs		
Setup time	t _{SETUP}	CL, DI, CE	1.0			μs		
Hold time	t _{HOLD}	CL, DI, CE	1.0			μs		
Operating frequency	fopg	CL			500	kHz		

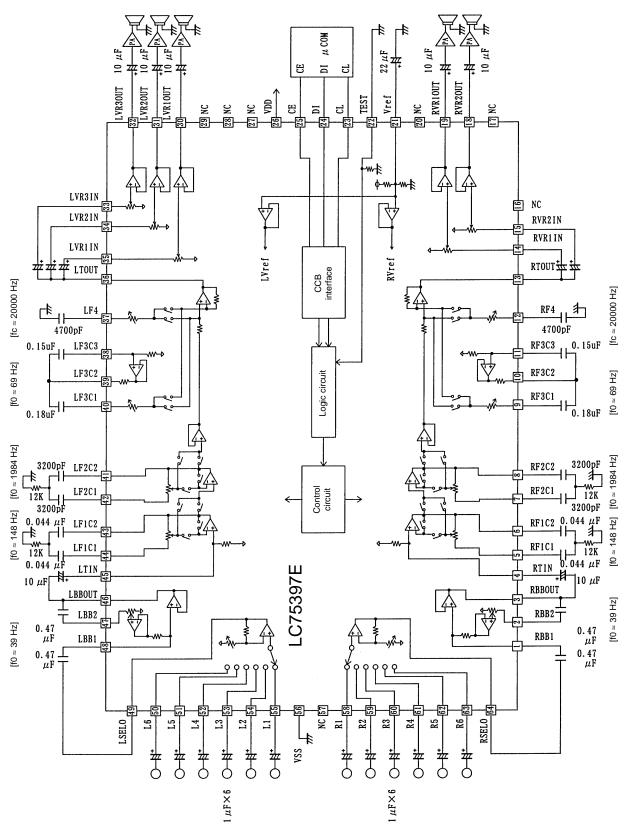
Electrical Characteristics at Ta = 25 $^{\circ}C,\,V_{DD}$ = 10 V, V_{SS} = 0 V

Parameter	Sumbol	Symbol Conditions		Ratings		Unit
Symbo		Conditions	min	typ	max	
[Input block]						
Input resistance	Rin	L1 to L6, R1 to R6		50		kΩ
Clipping level	Vcl	LSELO, RSELO: THD = 1.0%		3.00		Vrms
Output load resistance	RL	LSELO, RSELO	10			kΩ
[Volume control block]		·				
Input resistance	Rin	LVR1IN, RVR1IN, LVR2IN, RVR2IN, LVR3IN		50		kΩ
[Bass control block]		•				
Control range	Geq	Max, boost/cut	±8	±10	±12	dB
Step resolution	Estep		1	2	3	dB
	Rbb1			1.3		kΩ
Internal feedback resistance	Rbb2			58		- K12
[F1/F2 band equalizer control block]	•				
Control range	Geq	Max. boost/cut	±8	±10	±12	dB
Step resolution	Estep		1	2	3	dB
Internal feedback resistor	Rfeed		31	51.8	73	kΩ
[F3/F4 band equalizer control block]					
Control range	Geq	Max. boost/cut	±8	±10	±12	dB
Step resolution	Estep		1	2	3	dB
Internal feedback resistor	Rfeed		17	28	39	kΩ
[Overall characteristics]		·	·			
Total harmonic distortion	THD	$V_{IN} = 1$ Vrms, f = 1 kHz, with all controls flat overall			0.01	%
Crosstalk	СТ	V_{IN} = 1 Vrms, f = 1 kHz, with all controls flat overall, Rg = 1 k Ω	80			dB
Output noise voltage	V _N 1	With all controls flat overall, 80 kHz, L.P.F		10.2		μV
Output hoise voltage	V _N 2	Bass band = +10dB, With all controls overall, 80 kHz, L.P.F		10.6		μV
Output at maximum attenuation	V _o min	With all controls flat overall		-90		dB
Current drain	I _{DD}	$V_{DD} - V_{SS} = 10.5 V$		58		mA
Input high level current	III	CL, DI, CE, V _{IN} = 10.5 V			10	μA
Input low level current I _{IL} CL, DI, CE, V _{IN} = 0 V						μA



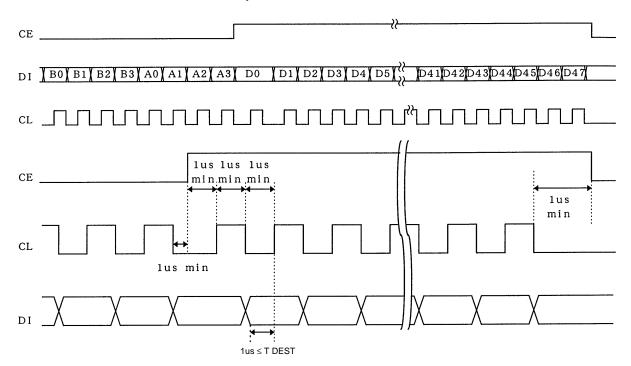
Top view

Sample Application Circuit



Control System Timing and Data Formats

To control the LC75397E, specified sequences are required to be input through the pins CE, CL, and DI. Each sequence consists of 48 bits: an 8-bit address followed by 56 bits of data.



1. Address Code (B0 to A3)

This product uses an 8-bit address code, and supports the same specifications as other Sanyo CCB serial bus products.

Address code (LSB)

B0	B1	B2	B3	A0	A1	A2	A3	
0	1	0	0	0	0	0	1	(82HEX)

2. Control Code Allocations

Input switching control (L1, L2, L3, L4, L5, R1, R2, R3, R4, R5)

D0	D1	D2	Operation		
0	0	0	L1 (R1)	ON	
1	0	0	L2 (R2)	ON	
0	1	0	L3 (R3)	ON	
1	1	0	L4 (R4)	ON	
0	0	1	L5 (R5)	OFF	
1	0	1	Switch all	OFF	
0	1	1	Switch all	OFF	
1	1	1	Switch all	OFF	

Input switching control	D3	Operation
(L6, R6)	1	L6 (R6) OFF
	0	L6 (R6) ON

D4	D5	D6	D7	Operation
0	0	0	0	0 dB
1	0	0	0	+2 dB
0	1	0	0	+4 dB
1	1	0	0	+6 dB
0	0	1	0	+8 dB
1	0	1	0	+10 dB
0	1	1	0	+12 dB
1	1	1	0	+14 dB
0	0	0	1	+16 dB
1	0	0	1	+18 dB
0	1	0	1	+20 dB
1	1	0	1	+22 dB
0	0	1	1	+24 dB
1	0	1	1	+26 dB
0	1	1	1	+28 dB
1	1	1	1	+30 dB

Bass and 4-band equalizer control

			-	
D8	D9	D10	D11	Bus
D12	D13	D14	D15	f1 band
D16	D17	D18	D19	f2 band
D20	D21	D22	D23	f3 band
D24	D25	D26	D27	f4 band
1	0	1	0	+10 dB
0	0	1	0	+8 dB
1	1	0	0	+6 dB
0	1	0	0	+4 dB
1	0	0	0	+2 dB
0	0	0	0	0 dB
1	0	0	1	–2 dB
0	1	0	1	-4 dB
1	1	0	1	6 dB
0	0	1	1	–8 dB
1	0	1	1	-10 dB

LC75397E

Volume control	D28	D29	D30	D31	D32	D33	D34	D35
	0	0	0	0	0	0	0	0
	1	0	0	0	0	0	0	0
	0	1	0	0	0	0	0	0
	1	1	0	0	0	0	0	0
	0	0	1	0	0	0	0	0
	1	0	1	0	0	0	0	0
	0	1	1	0	0	0	0	0
	1	1	1	0	0	0	0	0
	0	0	0	1	0	0	0	0
	1	0	0	1	0	0	0	0
	0	1	0	1	0	0	0	0
	1	1	0	1	0	0	0	0
	0	0	1	1	0	0	0	0
	1	0	1	1	0	0	0	0
	0	1	1	1	0	0	0	0
	1	1	1	1	0	0	0	0
	0	0	0	0	1	0	0	0
	1	0	0	0	1	0	0	0
	0	1	0	0	1	0	0	0
	1	1	0	0	1	0	0	0
	0	0	1	0	1	0	0	0
	1	0	1	0	1	0	0	0
	0	1	1	0	1	0	0	0
	1	1	1	0	1	0	0	0
	0	0	0	1	1	0	0	0
	1	0	0	1	1	0	0	0
	0	1	0	1	1	0	0	0
	1	1	0	1	1	0	0	0
	0	0	1	1	1	0	0	0
	1	0	1	1	1	0	0	0
	0	1	1	1	1	0	0	0
	1	1	1	1	1	0	0	0
	0	0	0	0	0	1	0	0
	1	0	0	0	0	1	0	0
	0	1	0	0	0	1	0	0
	1	1	0	0	0	1	0	0
	0	0	1	0	0	1	0	0
	1	0	1	0	0	1	0	0
	0	1	1	0	0	1	0	0
	1	1	1	0	0	1	0	0
	0	0	0	1	0	1	0	0
	1	0	0	1	0	1	0	0
	0	1	0	1	0	1	0	0
	1	1	0	1	0	1	0	0
	0	0	1	1	0	1	0	0
	1	0	1	1	0	1	0	0
	0	1	1	1	0	1	0	0
	1	1	1	1	0	1	0	0
	0	0	0	0	1	1	0	0

0

1

1

0

0

0

0

0

1

1

–50 dB Continued on next page.

0

0

1

1

0

0

Operation 0 dB -1 dB –2 dB –3 dB -4 dB –5 dB –6 dB –7 dB –8 dB –9 dB -10 dB –11 dB –12 dB –13 dB –14 dB –15 dB -16 dB -17 dB –18 dB –19 dB –20 dB –21 dB –22 dB –23 dB –24 dB –25 dB –26 dB –27 dB –28 dB –29 dB -30 dB –31 dB –32 dB –33 dB –34 dB –35 dB -36 dB –37 dB –38 dB -39 dB –40 dB –41 dB –42 dB –43 dB –44 dB –45 dB -46 dB –47 dB –48 dB –49 dB

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D28	D29	D30	D31	D32	D33	D34	D35	Operation
1	1	0	0	1	1	0	0	–51 dB
0	0	1	0	1	1	0	0	–52 dB
1	0	1	0	1	1	0	0	–53 dB
0	1	1	0	1	1	0	0	–54 dB
1	1	1	0	1	1	0	0	–55 dB
0	0	0	1	1	1	0	0	–56 dB
1	0	0	1	1	1	0	0	–57 dB
0	1	0	1	1	1	0	0	–58 dB
1	1	0	1	1	1	0	0	–59 dB
0	0	1	1	1	1	0	0	-60 dB
1	0	1	1	1	1	0	0	–61 dB
0	1	1	1	1	1	0	0	-62 dB
1	1	1	1	1	1	0	0	–63 dB
0	0	0	0	0	0	1	0	-64 dB
1	0	0	0	0	0	1	0	–65 dB
0	1	0	0	0	0	1	0	-66 dB
1	1	0	0	0	0	1	0	–67 dB
0	0	1	0	0	0	1	0	–68 dB
1	0	1	0	0	0	1	0	-69 dB
0	1	1	0	0	0	1	0	–70 dB
1	1	1	0	0	0	1	0	–71 dB
0	0	0	1	0	0	1	0	–72 dB
1	0	0	1	0	0	1	0	–73 dB
0	1	0	1	0	0	1	0	–74 dB
1	1	0	1	0	0	1	0	–75 dB
0	0	1	1	0	0	1	0	–76 dB
1	0	1	1	0	0	1	0	–77 dB
0	1	1	1	0	0	1	0	–78 dB
1	1	1	1	0	0	1	0	–79 dB
0	0	0	0	1	0	1	0	-∞
							·I	
D36	D37	0	Operation					
0	0	Ini	tial setting					

Channel selection control	D36	D37	Operation						
	0	0	Initial setting						
	1	0	Rię	Righ channel					
	0	1	Le	ft channel					
	1	1	Simulatan	eous left a	nd right				
Volume 1 control	D38	C	peration					d when D36 is set to 1.	
	0	С	ontrol off		Left chan	inel control	is enabled	when D37 is set to 1.	
	1	Cont	trol enabled						
Volume 2 control	D39	Operation			Right channel control is enabled when D36 is set to 1. Left channel control is enabled when D37 is set to 1.				
	0	С	ontrol off		Leit chan		is enabled		
	1	Cont	trol enabled						
		•							
Volume 3 control	D40	0	peration		Control of this function is enabled when D37 is set to 1.				
	0	С	ontrol off						
	1	Cont	trol enabled						
			1					1	
Test mode control	D41	D42	D43	D44	D45	D46	D47		
	0	0	0	0	0	0	0		

These bits are for chip testing and must all be set to 0 in application systems.

Pin Functions

Pin No.	Pin	Function	Equivalent circuit			
55	L1					
54	L2					
53	L3					
52	L4					
51	L5					
50	L5 L6		VDD ← 🖂 🚽 🙀 VDD			
		Signal inputs				
58	R1					
59	R2					
60	R3		Rn The second se			
61	R4		vref ₩			
62	R5		m m			
63	R6					
49	LSELO	Input selector outputs				
64	RSELO					
48 47 1 2 46 3	LBB1 LBB2 RBB1 RBB2 LBBOUT RBBOUT	Bass circuit inputs and outputs	VDD VDD VDD Vref WDD BB1 WDD Vref WDD WDD WDD WDD WDD WDD WDD WDD WDD WD			
			VDD			
45	LTIN	Equalizer inputs	β _γ VDD			
4	RTIN					
44	LF1C1					
43	LF1C2	Connections for the resistors and capacitors that form the F1 band equalizer.	Vref 😽 🚧 📶			
5	RF1C1					
6	RF1C2					
	111102		VDD VDD P P			
42	LF2C1		FnC1			
41	LF2C2	Connections for the resistors and capacitors that form the F2				
7	RF2C1	band equalizer.				
8	RF2C2					

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Pin No.	Pin	Function	Equivalent circuit
37 12	LF4 RF4	Connections for the capacitors that form the equqlizer F4 band filters Connections for external capacitors	VDD F4 F4
40 39 38 9 10 11	LF3C1 LF3C2 LF3C3 RF3C1 RF3C2 RF3C3	Connections for the resistors and capacitors that form the F3 band equalizer.	VDD F3C1 VDD F3C2 VDD F3C2 VDD F3C3 VDD F3C3 VDD VDD VDD VDD VDD VDD VDD VDD VDD VD
36 13	LTOUT RTOUT	Connections for the resistors and capacitors that form the F3 band equalizer.	
35 34 33 14 15	LVR1IN LVR2IN LVR3IN RVR1IN RVR2IN	 Left channel volume input 1 Left channel volume input 2 Left channel volume input 3 Right channel volume input 1 Right channel volume input 2 	→ VDD → W→ ↓ ↓ → ₩→ ↓ → ₩→ ↓ ₩→ ↓ ₩→ ↓
32 31 30 18 19	LVR3OUT LVR2OUT LVR1OUT RVR2OUT RVR1OUT	 Left channel volume output 3 Left channel volume output 2 Left channel volume output 1 Right channel volume output 2 Right channel volume output 1 	VDD VRnOUT

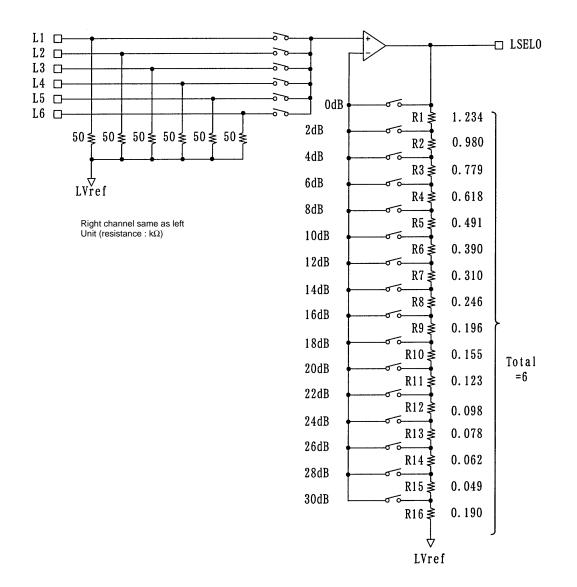
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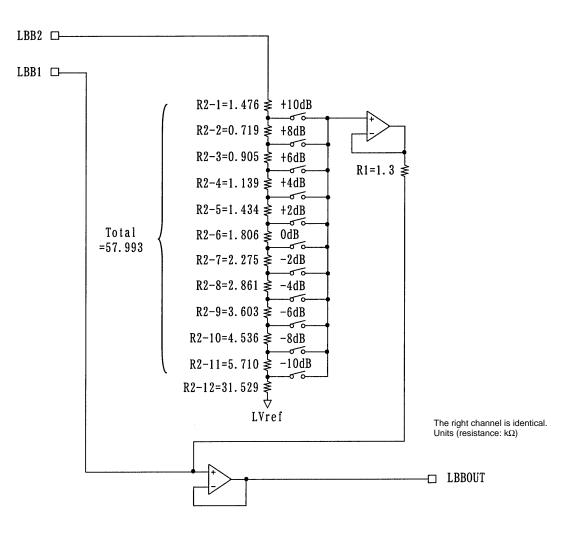
Pin No.	Pin	Function	Equivalent circuit
21	Vref	• A capacitor with a value of a few tens of μF must be inserted between Vref and AV _{SS} (V _{SS}) to reduce power supply ripple in the 0.5 \times V _{DD} voltage generator block used for analog ground.	VDD Vref 777
56	V _{SS}	Ground	
26	V _{DD}	Power supply	
25	CE	• Chip enable When this pin goes from high to low, data is written to an internal latch and the analog switches operate. Data transfers are enables when this pin is at the high level.	
24 23	DI CL	Serial data and clock inputs for chip control	
22	TEST	• Electronic volume control test pin. This pin must be held at the V _{SS} potential.	VDD
16 17 20 27 28 29 57	NC	• Unused pins. These pins must either be left open or connected to V _{SS} .	

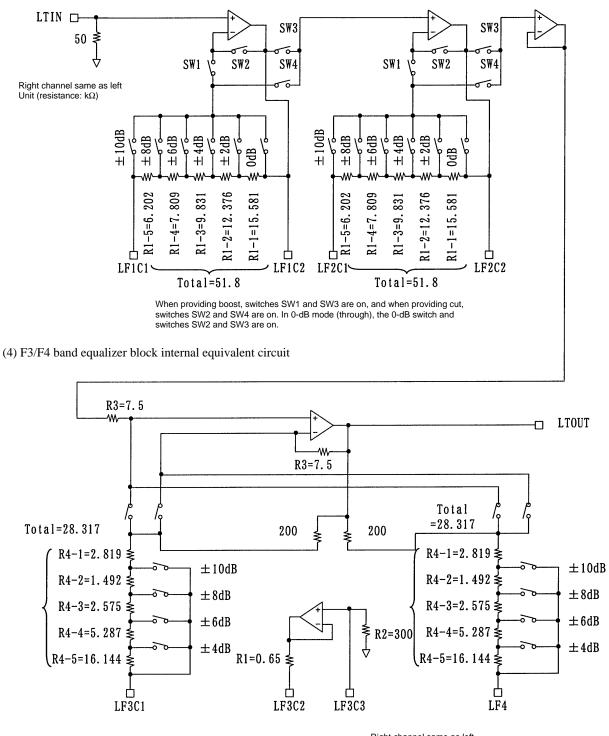
Equivalent Circuit Diagram

(1) Selector Control Block



(2) Bass control block internal equivalent circuit





(3) F1/F2 band equalizer block internal equivalent circuit

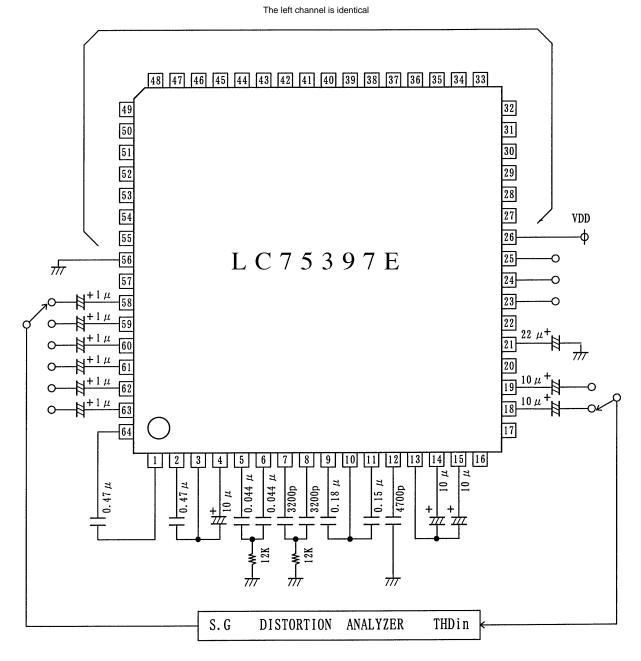
Right channel same as left Unit (resistance: $k\Omega$)

LVR1IN LVR2IN LVR3IN 다	odB [LVR10UT LVR20UT
R1=5434 ≱	 	R28=243≩2	8dB	R55=87≩	-55dB	LVR3OUT
R2=4845 ≩	-2dB	R29=216≩ -2	9dB	R56=77 ≩	-56dB	
R3=4319 ≩	-3dB	R30=193 -3	DdB	R57=69 奏	-57dB	
R4=3850 ≩		R31=172 ≩3	1 dB	R58=61 ≩	-58dB	
R5=3431 ≩	-5dB		2dB	R59=55 ≩	-59dB	
R6=3058 ≰		R33=137≹3;	3dB	R60=49 ≩	-60dB	
R7=2726		R34=122	4dB	R61=87≩	-61dB	
R8=2429 🛓		R35=108 ₹3	5dB	R62=78≩	-62dB	
R9=2165 🚔		R36=97 ≩3	5dB	R63=69≩	-63dB	
R10=1930	-10dB	R37=86 \$ -3'	7dB	R64=62 ≰	-64dB	
R11=1720	-11dB	R38=77 ≩3	BdB	R65=55 ≰	-65dB	
R12=1533	-12dB	R39=68 -39	9dB	R66=49≩	-66dB	
R13=1366 ≩	-13dB	R40=61 ≨4(DdB	R67=87 ≩	-67dB	
R14=1218	-14dB	R41=54	ldB	R68=78≸	-68dB	
R15=1085 ≸	-15dB	R42=48	2dB	R69=69≩	-69dB	
R16=967 ≸	-16dB	R43=86 ₹	BdB	R70=62 ≩	-70dB	
R17=862 ≩	17dB	R44=77 ₹44	4dB	R71=55 ≩	-71dB	
R18=768 ≸	-18dB	R45=69	5dB	R72=49 ≩	-72dB	
R19=685 🛓		R46=61 -46	SdB R73	=87	-73dB	
R20=610	-20dB	R47=55	7dB R74	=78	-74dB	
R21=544 ≰	-21dB	R48=49 ₹ -48	BdB R75	=69	-75dB	
R22=485	-22dB	R 49=87 ₹49	BdB R76	=62	-76dB	
R23=432 ≸	-23dB	R 50=77 ₹	DdB R77	=55	-77dB	
R24=385 ≩	-24dB	R 51=69 ₹ -51	dB R78	=49	-78dB	
R25=343 ≩	-25dB	R 52=61 ₹ -52	2dB R79	=44	-79dB	
R26=306		R 53=55 ₹ -53	BdB R80	=359	- ∞	
R27=273 ₹		R 54=49 ₹ -54	ldB			
	704				Pight ch	annel same as left
	794 R81	≰ \$796 \$ 798 	800 ≤ R84	\$ 802 \$ 804 R85 R86		sistance: $k\Omega$)
		Ld				
				LVref		
				LAIGI		

Volume block internal equivalent circuit

Test Circuits

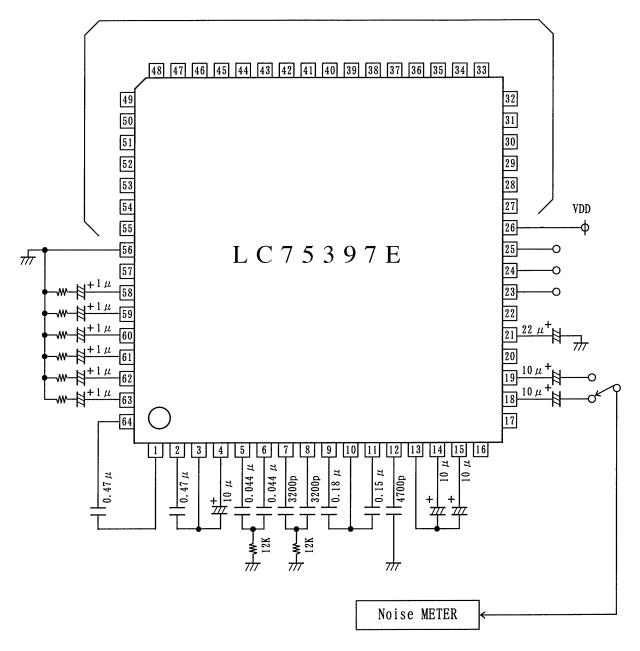
Total Harmonic Distortion



Unit (capacitance : F)

Output Noise Voltage

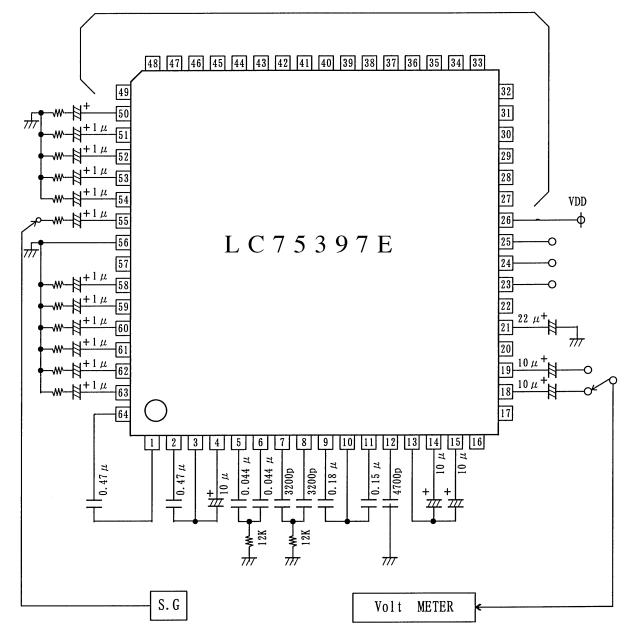
The left channel is identical



Unit (resistance : Ω , capacitance : F)

Crosstalk

The left channel is identical

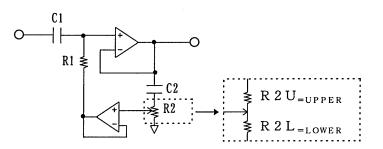


Unit (resistance : Ω , capacitance : F)

External Capacitor Calculations

1. Bass circuit

The value of the external capacitor used by the LC75397E bass control can be calculated as shown in the example below.



Sample calculation: For a center frequency f0 of 39 Hz

Substitute the LC75397E internal resistors R1 and R2 shown below into the above formula. This allows the value of the capacitor, C, to be calculated.

$$R1 = 1.3 \text{ k}\Omega$$
$$R2 = 57.993 \text{ k}\Omega$$

Assume C1 = C2 = C.

$$C = \frac{1}{2\pi f0 \sqrt{R1R2}}$$
$$C = \frac{1}{2\pi \times 39 \times \sqrt{1300 \times 58000}} \neq 0.47 \,\mu\text{F}$$

Formula for calculating the gain:

$$\label{eq:R1} \begin{split} R1 &= 1.3 \; k\Omega \\ R2U &= 1.476 \; k\Omega \\ R2L &= 56.517 \; k\Omega \end{split}$$

$$G = \sqrt{(\frac{R1}{R1 + R2U})^2 + (\frac{R1 (R2U + R2L)}{(R1 + R2U)\sqrt{R1 (R2U + R2L)}})^2} = 3.16 = 10 \text{ dB}$$

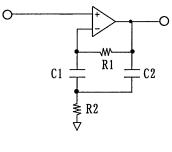
Formula for calculating Q:

$$Q = \sqrt{\frac{R1 (R2U + R2L)}{(R1 + R2U) \sqrt{R1 (R2U + R2L)}}} \neq G$$

2. F1/F2 band circuits

This section presents the equivalent circuit and the formulas used to calculate the external resistor and capacitor values to provide a center frequency of 148 Hz.

• F1/F2 band equivalent circuit



• Sample calculation

- Specifications: Center frequency: f0 = 148 HzGain at maximum boost: $G_{+10dB} = 10 \text{ dB}$ Assume $R1 = 51.8 \text{ k}\Omega$ and C1 = C2 = C.
- (1) Determine R2 from the specification that $G_{+10dB} = 10 \text{ dB}$.

$$G_{+10dB} = 20 \times \text{LOG}_{10} \left(1 + \frac{\text{R1}}{2\text{R2}} \right)$$
$$\text{R2} = \frac{\text{R1}}{2(10^{\text{G}+10\text{dB}/20} - 1)} = \frac{51800}{2 \times (3.162 - 1)} = 11979.7 \neq 12 \text{ k}\Omega$$

(2) Determine C from the specification that the center frequency f0 = 148 Hz.

$$f0 = \frac{1}{2\pi f \sqrt{R1R2C1C2}}$$

$$C = \frac{1}{2\pi f 0 \sqrt{R1R2}} = \frac{1}{2\pi \times 148 \sqrt{51800 \times 12000}} = 0.0431 \times 10^{-6} \neq 0.044 \,\mu\text{F}$$

(3) Determine Q.

$$Q = \frac{C \cdot C \cdot R1}{2C} \cdot \frac{1}{\sqrt{R1R2CC}} = \frac{51800}{2\sqrt{51800 \times 12000}} = 1.039$$

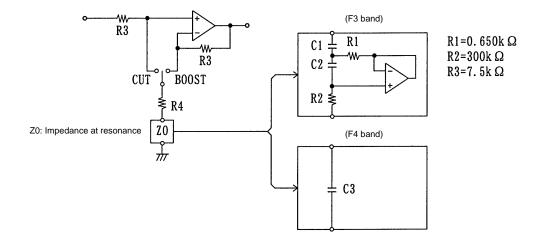
3. F3/F4 band circuits

The F3 band circuit supports peaking characteristics and the F4 band circuit supports shelving characteristics.

(1) Peaking characteristics (F3 band)

The external capacitor is used to construct a simulated inductor. This section presents the equivalent circuit and the formulas for determining the desired center frequency.

(a) Simulated inductor equivalent circuit



(b) Sample calculation

Specifications: 1) Center frequency: f0 = 107 Hz2) Q at maximum boost: $Q_{+10dB} = 0.8$

- (1) Determine the sharpness, Q0, of the simulated inductor itself. $Q_0 = (R1 + R4) / R1 \times Q_{+10dB} \approx 4.270$
- (2) Determine C1. C1 = $1/2\pi f 0 R 1 Q_0 \approx 0.536 (\mu F)$
- (3) Determine C2.

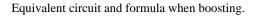
 $C2 = Q_0 / 2\pi f 0 R2 \approx 0.021 \ (\mu F)$

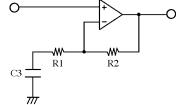
(c) Reference values for C1 and C2

Center frequency f0 (Hz)	C1 (F)	C2 (F)
107	0.536 µ	0.021 µ
340	0.169 µ	6663P
1070	0.054 µ	2117P
3400	0.017 µ	666P

(2) Shelving characteristics (F4 band)

Gains of ± 10 dB (in 2-dB steps) with respect to a target frequency can be achieved by using an external capacitor C3 with a calculated according to the formula F shown below.

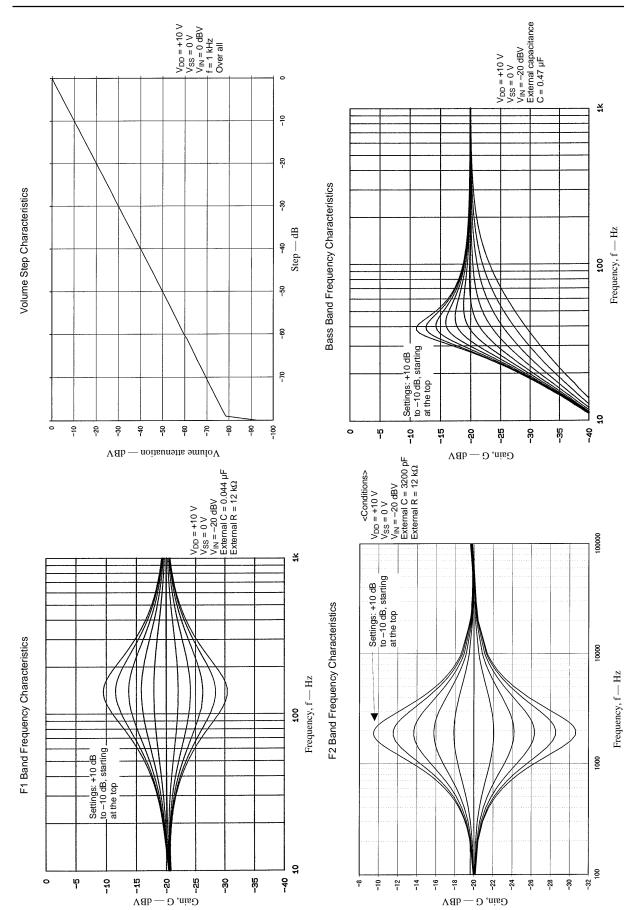




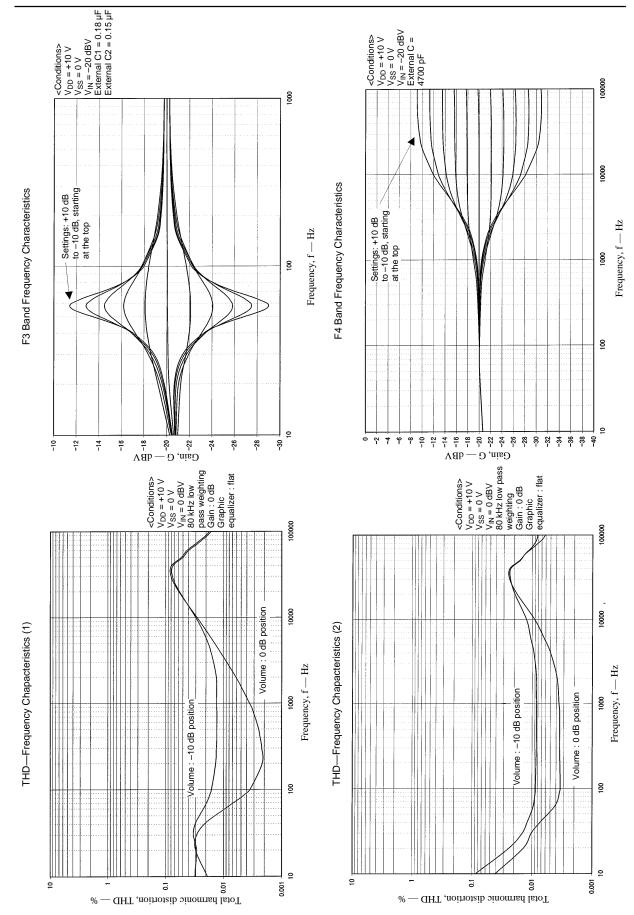
Sample calculation

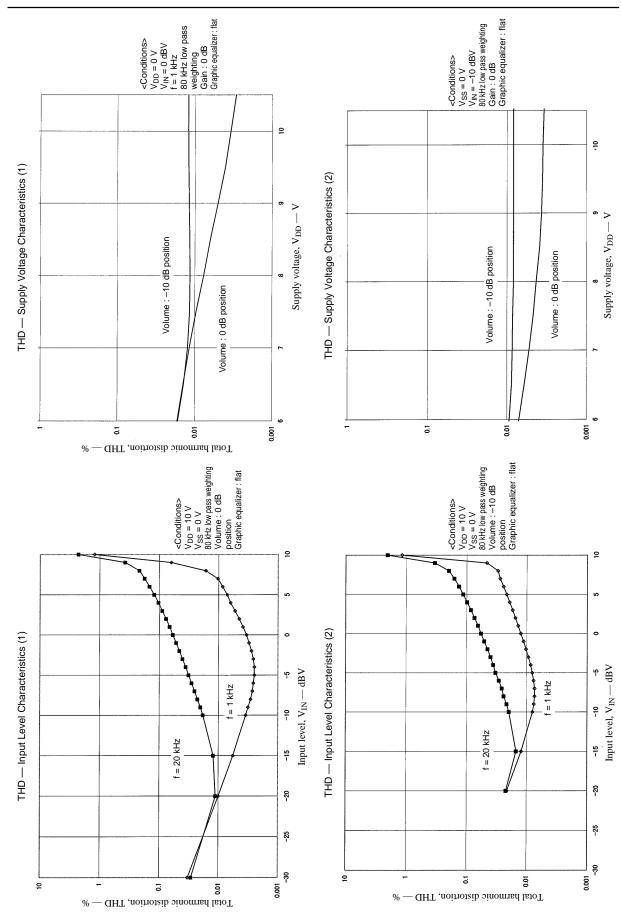
Specifications: 1) Target frequency: f = 17,000 Hz 2) R1= 2,819 k\Omega, R2 = 7.5 k\Omega

$$C = \frac{1}{2\pi f \sqrt{\left(\frac{R2}{10^{G/20} - 1}\right)^2 - R1^2}}$$
$$= \frac{1}{2\pi \times 17000 \sqrt{\left(\frac{7500}{3.16 - 1}\right)^2 - (2819)^2}}$$
$$\neq 4600 \text{ (pF)}$$



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Usage Notes

- When the power is first applied, the internal analog switches are in indeterminate states. The chip therefore requires muting or other external measures until it has received the proper data.
- After power is first applied, applications must initialize this chip by sending the initial data (1) and (2) described below.
- Provide grounding patterns or shielding for the lines to the CL, DI, and CE pins so as to prevent their high-frequency
 digital signals from interfering with the operation of nearby analog circuits.

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