Ordering number : EN5914

CMOS IC

LC75396NE

Single-Chip Electronic Volume Control System

Overview

The LC75396NE is an electronic volume control system providing control over volume, balance, 5-band equalizer, and input switching based on serial inputs.

Functions

- Volume control:
  The chip provides 81 levels of volume attenuation: in 1-dB step between 0 dB and –79 dB and –∞.
  Independent control over left front/rear and right front/rear channels provides balance control.
- Equalizer:
  The chip provides control in 2-dB steps over the range between +10 dB and –10 dB. Four of the five bands have peaking equalization; the remaining one, shelving equalization.
- Selector:
  The left and right channels each offer a choice of five inputs. The L5 and R5 inputs can be turned on and off independently. An external constant determines the amplification for the input signal.
- Serial data input
  — Supports CCB* format communication with the system controller.

Features

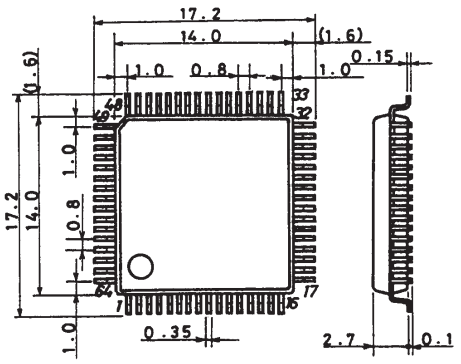
- Built-in buffer amplifiers reduce the number of external parts required.
- Silicon gate CMOS process reduces the noise of built-in switch.
- $V_{DD}/2$ reference voltage generation circuit built in.

Package Dimensions

unit: mm

3159-QFP64E

[LC75396NE]



SANYO: QFP64E

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	11	V
Maximum input voltage	V_{IN} max	CL, DI, CE, L1 to L5, R1 to R5, LTIN, RTIN, LFIN, RFIN, LRIN, RRIN	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 75°C, with PC board	550	mW
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

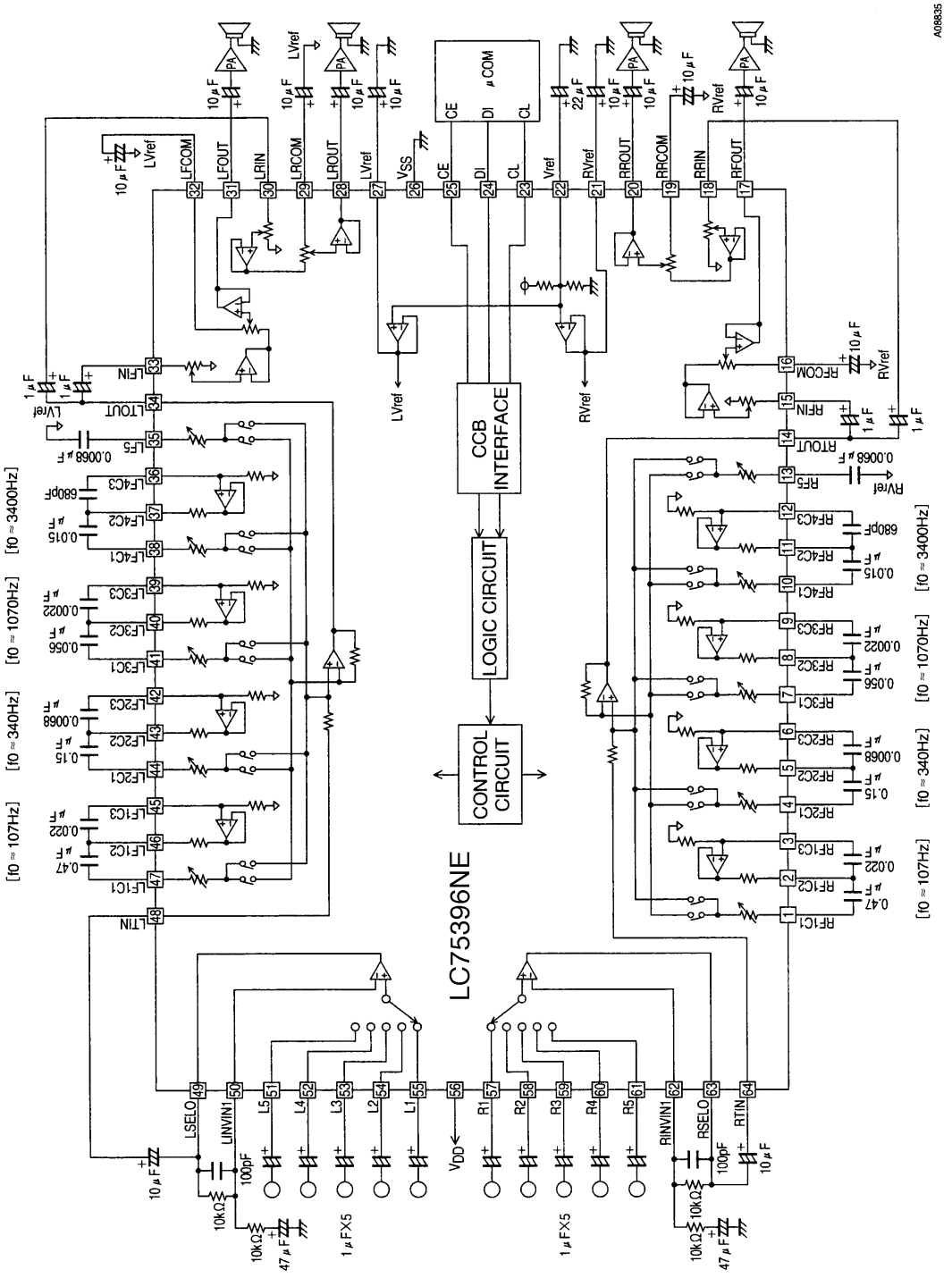
Allowable Operating Ranges at Ta = – 30 to + 75°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	6.0		10.5	V
Input high level voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Input low level voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}	CL, DI, CE, L1 to L5, R1 to R5, LTIN, RTIN, LFIN, RFIN, LRIN, RRIN	V_{SS}		V_{DD}	Vp-p
Input pulse width	$t_{øW}$	CL	1.0			µs
Setup time	t_{SETUP}	CL, DI, CE	1.0			µs
Hold time	t_{HOLD}	CL, DI, CE	1.0			µs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V_{DD} = 10 V, V_{SS} = 0 V

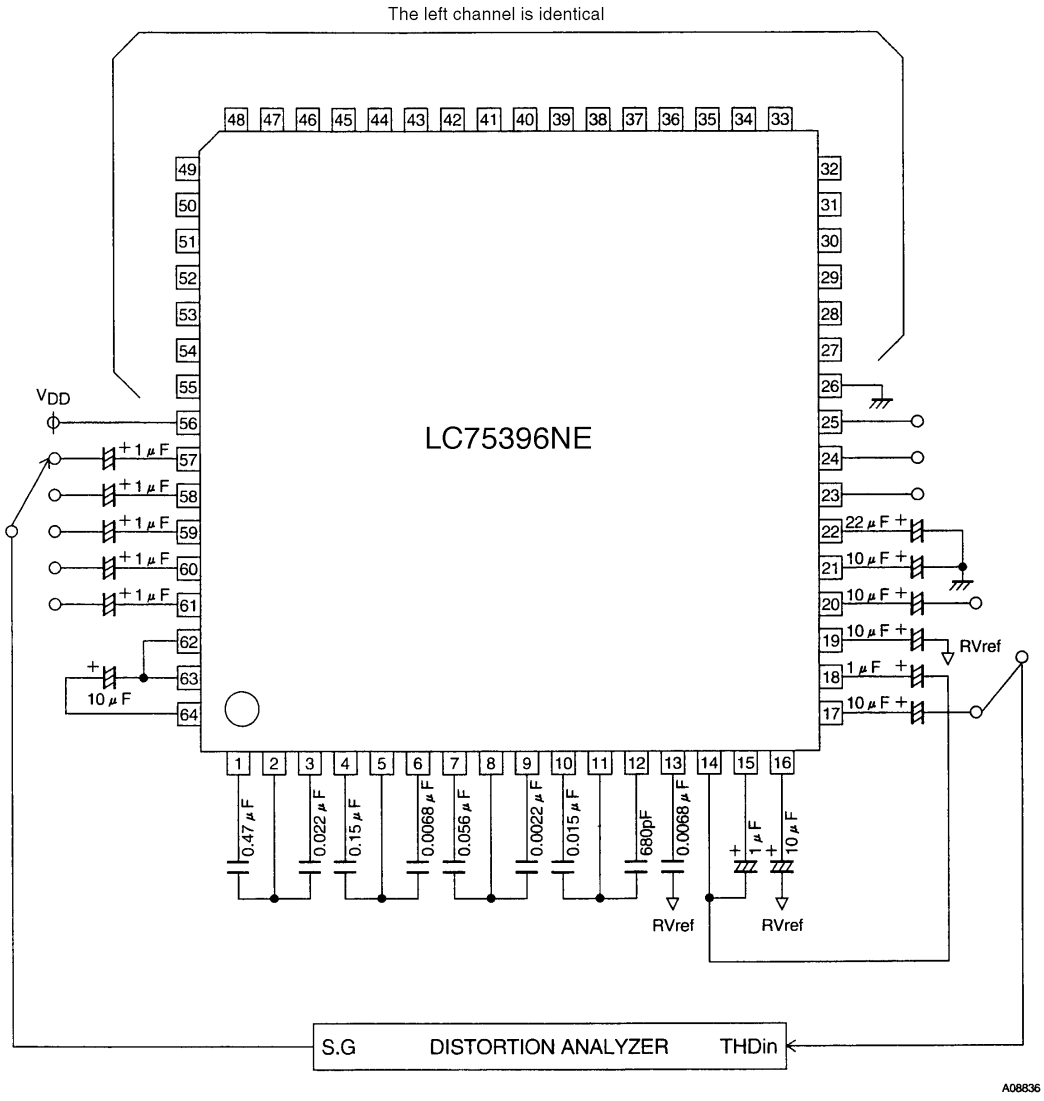
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Input block]						
Input resistance	Rin	L1 to L5, R1 to R5		50		kΩ
Clipping level	Vcl	LSELO, RSELO: THD = 1.0%		3.00		Vrms
Output load resistance	R_L	LSELO, RSELO	10			kΩ
[Volume control block]						
Input resistance	Rin	LFIN, LRIN, RFIN, RRIN		100		kΩ
[Equalizer control block]						
Control range	Geq	Max, boost/cut	±8	±10	±12	dB
Step resolution	Estep		1	2	3	dB
Internal feedback resistance	Rfeed		17	28	39	kΩ
[Overall characteristics]						
Total harmonic distortion	THD	V_{IN} = 1 Vrms, f = 1 kHz, with all controls flat overall			0.01	%
Crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz, with all controls flat overall, Rg = 1 kΩ	80			dB
Output noise voltage	V_N 1	With all controls flat overall, BW = 20 to 20kHz		2.9		µV
	V_N 2	GEQ F1 Band = +10dB, With all controls overall, BW = 20 to 20kHz		17		µV
Output at maximum attenuation	V_O min	V_{IN} = 1 Vrms, f = 1 kHz, main volume –∞		–90		dB
Current drain	I_{DD}	$V_{DD} - V_{SS}$ = 10.5 V		46.5	55.8	mA
Input high level current	I_{IH}	CL, DI, CE, V_{IN} = 10.5 V			10	µA
Input low level current	I_{IL}	CL, DI, CE, V_{IN} = 0 V	–10			µA

Sample Application Circuit

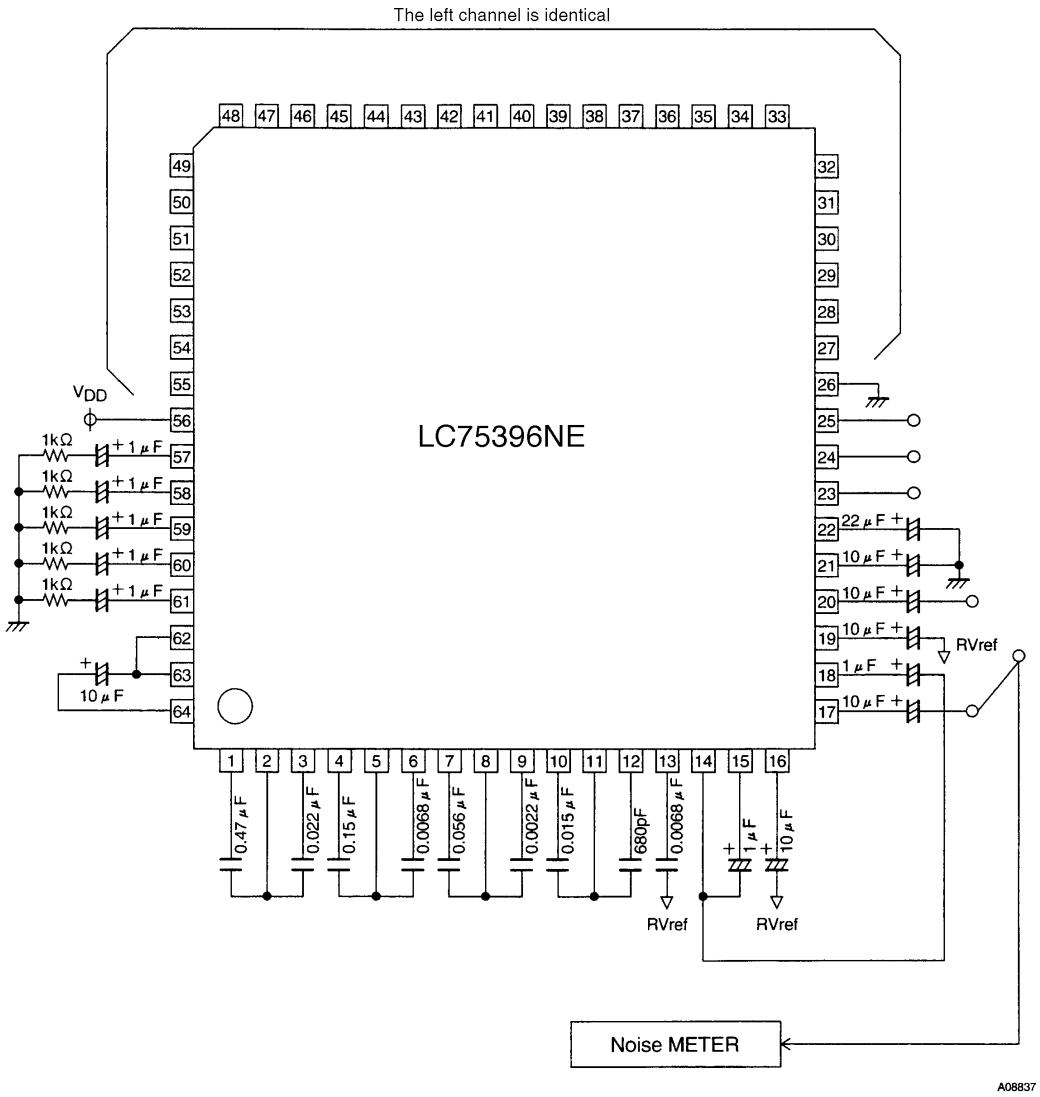


Test Circuits

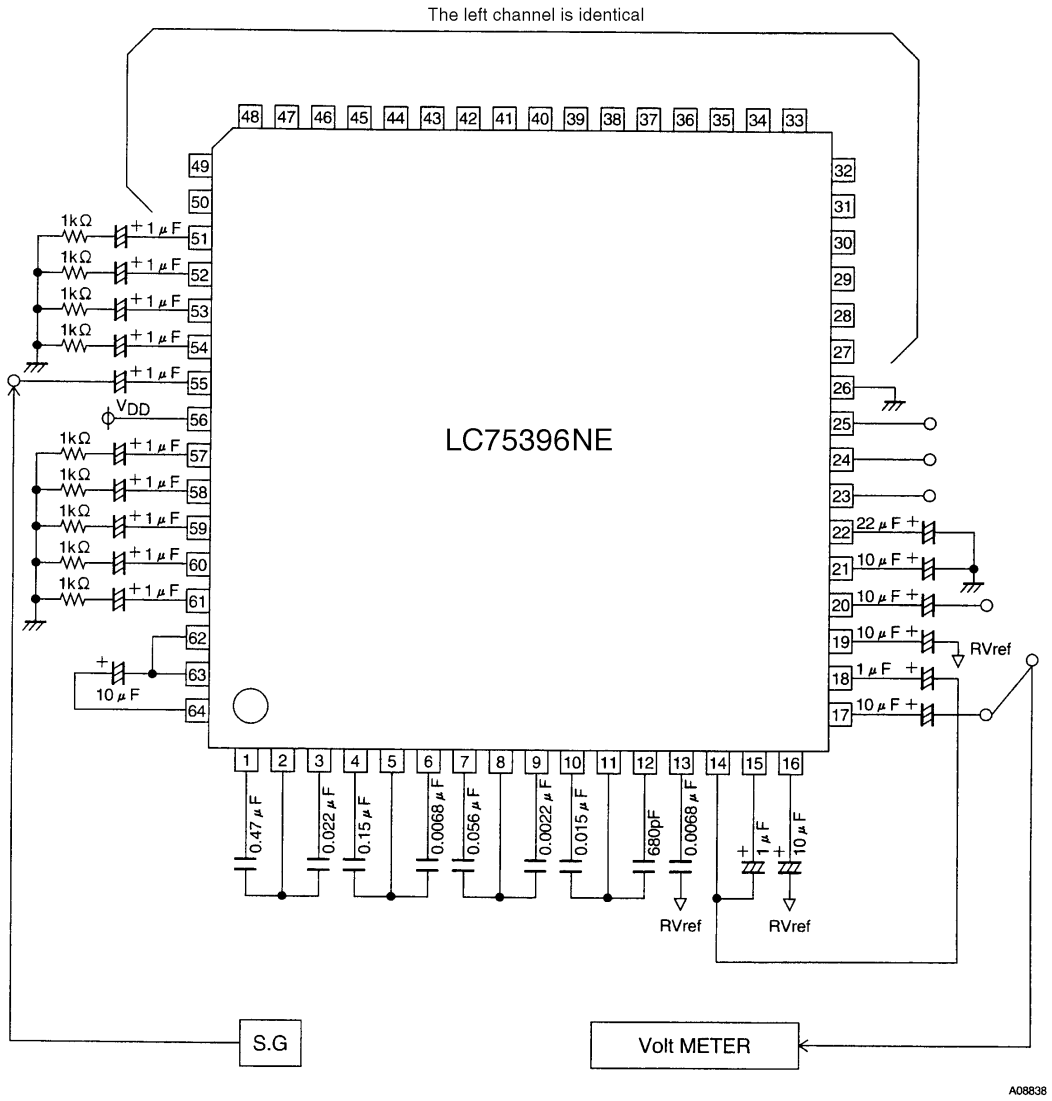
Total Harmonic Distortion



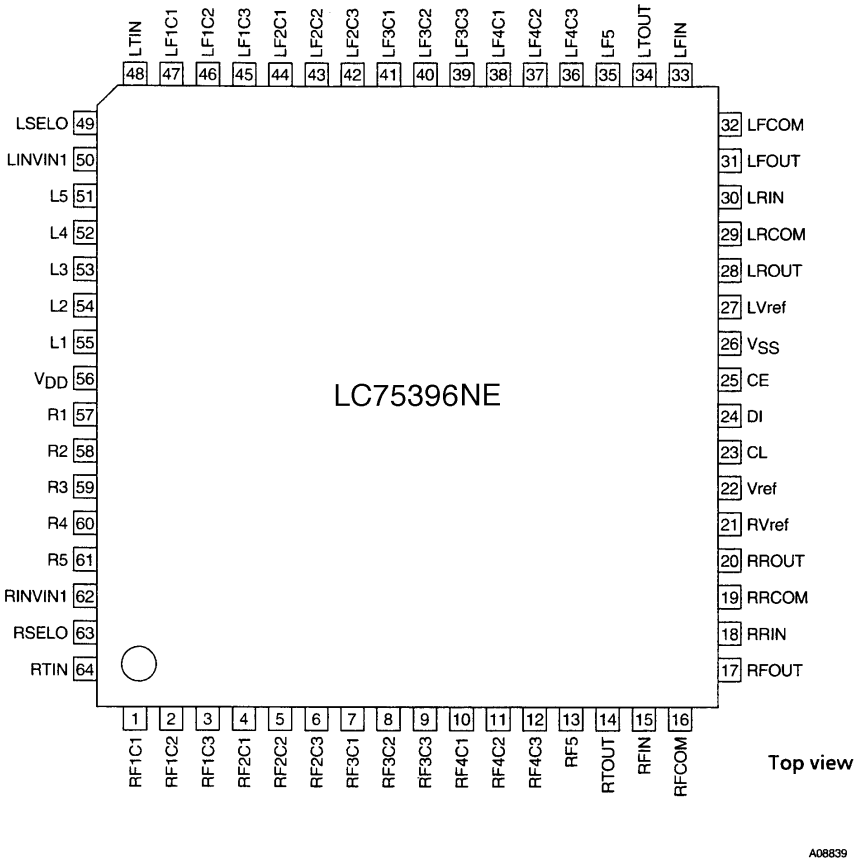
Output Noise Voltage



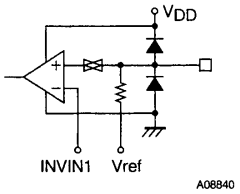
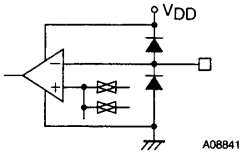
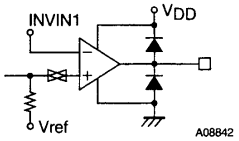
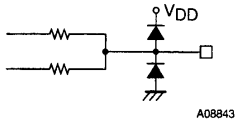
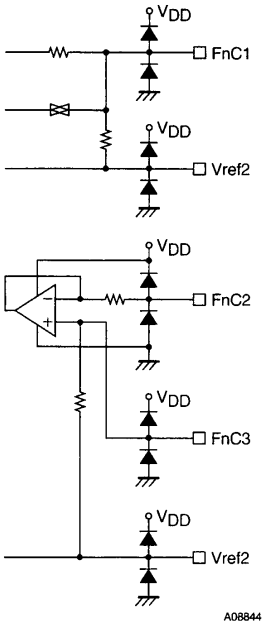
Crosstalk



Pin Assignment



Pin Functions

Pin No.	Pin	Function	Equivalent circuit
55 54 53 52 51 57 58 59 60 61	L1 L2 L3 L4 L5 R1 R2 R3 R4 R5	Signal inputs	
50 62	LINVIN1 RINVIN1	Inverting inputs to the operational amplifier that sets the input gain	
49 63	LSELO RSELO	Input selector outputs	
48 64	LTIN RTIN	Equalizer inputs	
47 46 45 1 2 3	LF1C1 LF1C2 LF1C3 RF1C1 RF1C2 RF1C3	· Connections for the capacitors that form the equalizer F1 band filters Capacitors must be connected between: LF1C1 (RF1C1) and LF1C2 (RF1C2), and between LF1C2 (RF1C2) and LF1C3 (RF1C3).	
44 43 42 4 5 6	LF2C1 LF2C2 LF2C3 RF2C1 RF2C2 RF2C3	· Connections for the capacitors that form the equalizer F2 band filters Capacitors must be connected between: LF2C1 (RF2C1) and LF2C2 (RF2C2), and between LF2C2 (RF2C2) and LF2C3 (RF2C3).	
41 40 39 7 8 9	LF3C1 LF3C2 LF3C3 RF3C1 RF3C2 RF3C3	· Connections for the capacitors that form the equalizer F3 band filters Capacitors must be connected between: LF3C1 (RF3C1) and LF3C2 (RF3C2), and between LF3C2 (RF3C2) and LF3C3 (RF3C3).	
38 37 36 10 11 12	LF4C1 LF4C2 LF4C3 RF4C1 RF4C2 RF4C3	· Connections for the capacitors that form the equalizer F4 band filters Capacitors must be connected between: LF4C1 (RF4C1) and LF4C2 (RF4C2), and between LF4C2 (RF4C2) and LF4C3 (RF4C3).	

Continued on next page.

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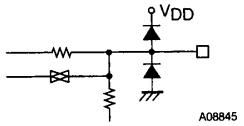
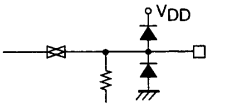
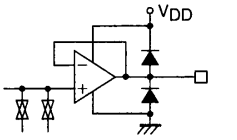
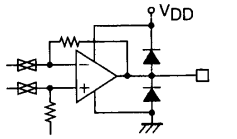
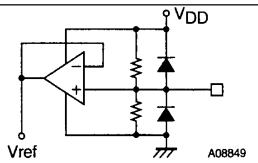
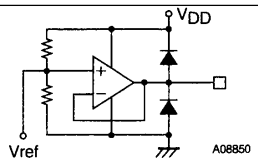
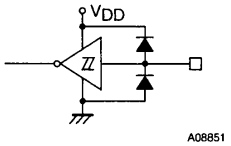
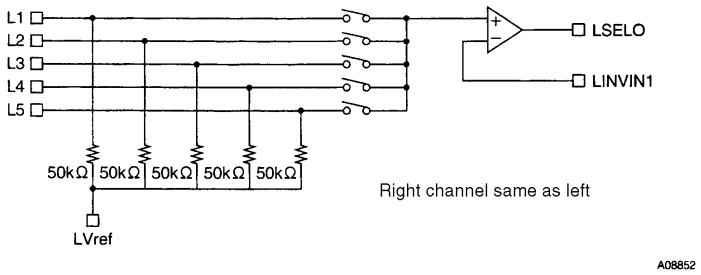
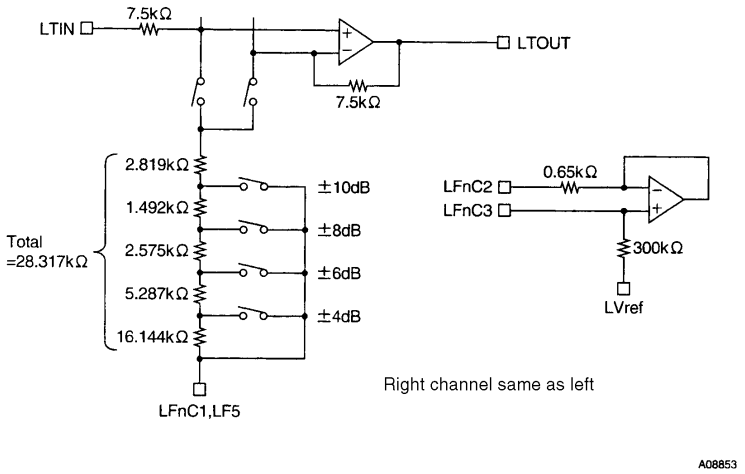
Pin No.	Pin	Function	Equivalent circuit
35 13	LF5 RF5	• Connections for the capacitors that form the equalizer F5 band filters Connections for external capacitors	
33 30 15 18	LFIN LRIN RFIN RRIN	• Input to the left channel front 4-dB step volume control. • Input to the left channel rear 4-dB step volume control. • Input to the right channel front 4-dB step volume control. • Input to the right channel rear 4-dB step volume control.	
32 29 16 19	LFCOM LRCOM RFCOM RRCOM	• Common pin for the left channel front 1-dB step volume control. • Common pin for the left channel rear 1-dB step volume control. • Common pin for the right channel front 1-dB step volume control. • Common pin for the right channel rear 1-dB step volume control.	
31 28 17 20	LFOUT LROUT RFOUT RROUT	• Left channel front volume control output • Left channel rear volume control output • Right channel front volume control output • Right channel rear volume control output	
34 14	LTOUT RTOUT	• Equalizer outputs	
22	Vref	• A capacitor of a few tens of µF must be inserted between Vref and AV_{SS} (V_{SS}) to handle power supply ripple in the $V_{DD}/2$ voltage generation circuit.	
27 21	LVref RVref	• Internal analog system grounds	
56	V_{DD}	• Power supply	
26	V_{SS}	• Ground	
25	CE	• Chip enable When this pin goes from high to low, data is written to an internal latch and the analog switches operate. Data transfers are enabled when this pin is at the high level.	
24 23	DI CL	• Serial data and clock inputs for chip control.	

Equivalent Circuit Diagram

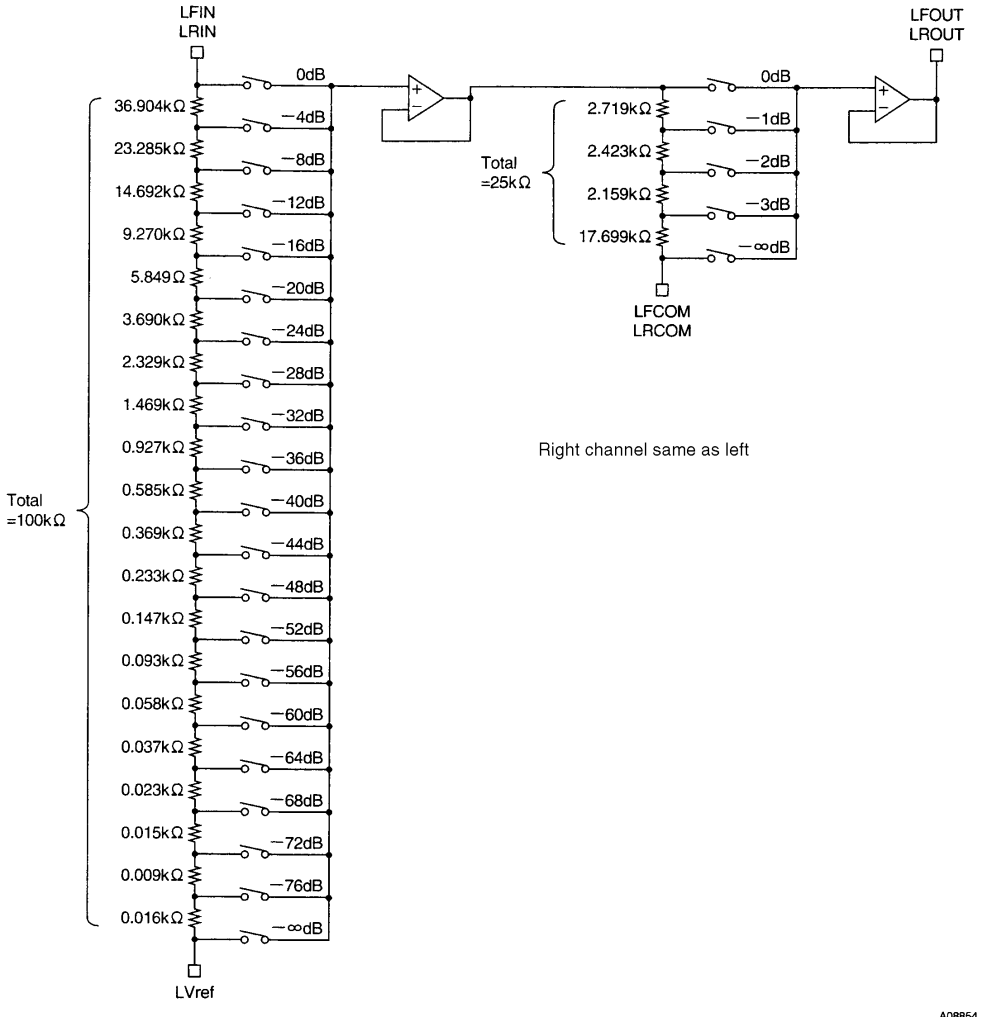
Selector Control Block



Equalizer Control Block



Volume Control Block

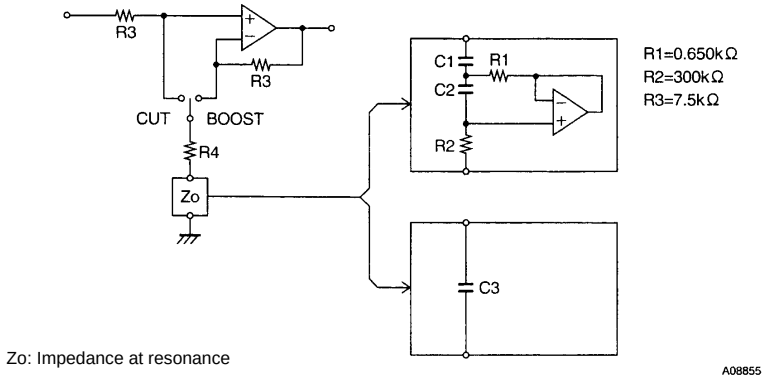


Calculating the Size of External Capacitors

The LC75396NE supports four bands with peaking characteristics and one band with shelving characteristics

1. Peaking Characteristics (bands F1 to F4)
   The external capacitor functions as the structural element of a simulated inductor. The equivalent circuit and the calculations required to achieve the desired center frequency are shown below.

• Equivalent circuit for the simulated inductor



Zo: Impedance at resonance

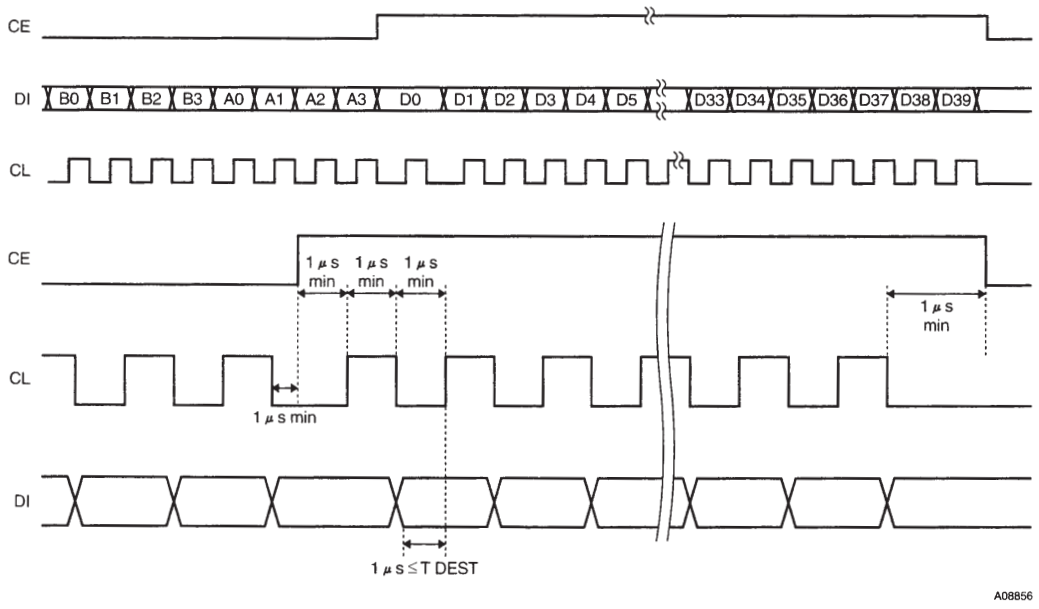
- Calculation example
  Specifications: Central frequency, F_O = 107 Hz
  Q factor at maximum boost, $Q_{+10\ dB}$ = 0.8
  — Calculate Q_O, the sharpness of the simulated inductance itself.
  $Q_O = (R1 + R4)/R1 \times Q_{+10dB}$ Note: R4 is from the separately issued internal block diagram.
  $\neq 4.270$
  — Calculate C1
  $C1 = 1/2\pi F_O R1 Q_O \neq 0.536\ (\mu F)$
  — Calculate C2
  $C2 = Q_O/2\pi F_O R2 \neq 0.021\ (\mu F)$
- Sample results

Central frequency F_O (Hz)	C1 (F)	C2 (F)
107	0.536 µ	0.021 µ
340	0.169 µ	6663 P
1070	0.054 µ	2117 P
3400	0.017 µ	666 P

2. Shelving characteristics (Band F5)
   Achieving the desired control of 2-dB steps over the range between +10 dB to –10 dB requires choosing a capacitor, C3, with an impedance of 650 Ω.

Control System Timing and Data Formats

To control the LC75396NE, specified sequences are required to be input through the pins CE, CL, and DI. Each sequence consists of 48 bits: an 8-bit address followed by 40 bits of data.



1. Address Code (B0 to A3)

   This product uses an 8-bit address code, and supports the same specifications as other Sanyo CCB serial bus products.

Address code (LSB)

B0	B1	B2	B3	A0	A1	A2	A3	
0	1	0	0	0	0	0	1	(82HEX)

2. Control Code Allocations

Input switching control

D0	D1	D2	Operation	
0	0	0	L1 (R1)	ON
1	0	0	L2 (R2)	ON
0	1	0	L3 (R3)	ON
1	1	0	L4 (R4)	ON
0	0	1		OFF
1	0	1		OFF
0	1	1		OFF
1	1	1		OFF

Input switching control

D3	Operation	
0	L5 (R5)	OFF
1	L5 (R5)	ON

Five band equalizer control

D4	D5	D6	D7	Band f1
D8	D9	D10	D11	Band f2
D12	D13	D14	D15	Band f3
D16	D17	D18	D19	Band f4
D20	D21	D22	D23	Band f5
1	0	1	0	+10dB
0	0	1	0	+8dB
1	1	0	0	+6dB
0	1	0	0	+4dB
1	0	0	0	+2dB
0	0	0	0	0dB
1	0	0	1	−2dB
0	1	0	1	−4dB
1	1	0	1	−6dB
0	0	1	1	−8dB
1	0	1	1	−10dB

Volume control

D24	D25	D26	D27	D28	D29	D30	D31	Operation
								1dB STEP
0	0							0dB
1	0							−1dB
0	1							−2dB
1	1							−3dB
								4dB STEP
		0	0	0	0	0	0	0dB
		1	0	0	0	0	0	−4dB
		0	1	0	0	0	0	−8dB
		1	1	0	0	0	0	−12dB
		0	0	1	0	0	0	−16dB
		1	0	1	0	0	0	−20dB
		0	1	1	0	0	0	−24dB
		1	1	1	0	0	0	−28dB
		0	0	0	1	0	0	−32dB
		1	0	0	1	0	0	−36dB
		0	1	0	1	0	0	−40dB
		1	1	0	1	0	0	−44dB
		0	0	1	1	0	0	−48dB
		1	0	1	1	0	0	−52dB
		0	1	1	1	0	0	−56dB
		1	1	1	1	0	0	−60dB
		0	0	0	0	1	0	−64dB
		1	0	0	0	1	0	−68dB
		0	1	0	0	1	0	−72dB
		1	1	0	0	1	0	−76dB
								MUTE
		1	1	1	1	1	0	−∞

Channel selection control

D32	D33	Operation
0	0	Initial setting
1	0	RCH
0	1	LCH
1	1	Simulataneous left and right

Left channel volume rear/front control

D34	Operation
0	Rear
1	Front

Control is enabled when D33 = 1

Right channel volume rear/front control

D35	Operation
0	Rear
1	Front

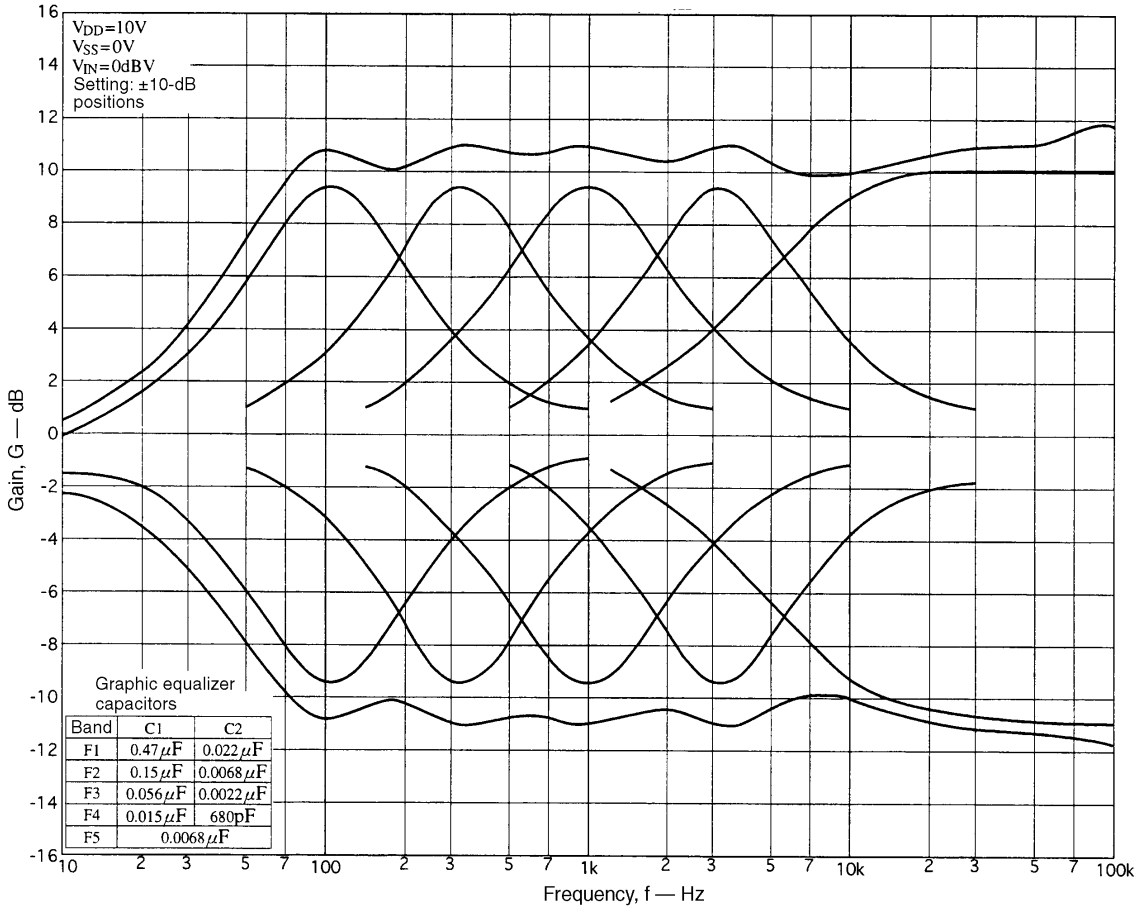
Control is enabled when D32 = 1

Test mode control

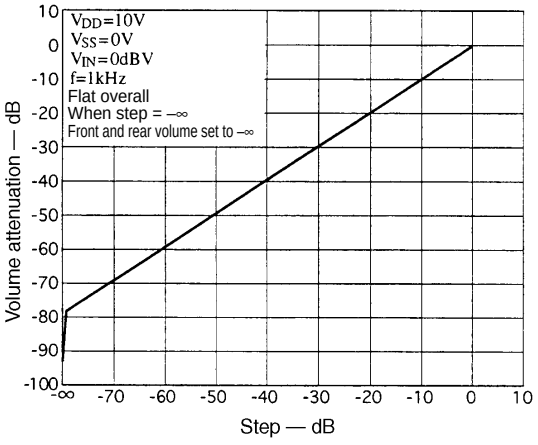
D36	D37	D38	D39	Operation
0	0	0	0	These bits are for chip testing and must all be set to 0 in application systems.

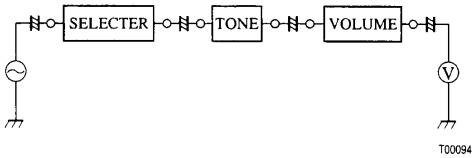
Notes: After power is first applied, applications must initialize this chip by sending the initial data (1) and (2) described below.
Initial data ... (1) Address 01000001
Data: (Set the volume to –∞set both D34 and D35 to 1, and set all other data to 0)
(2) Address 01000001
Data: (Set the volume to –∞, set both D34 and D35 to 0, and set all other data to 0)
After transferring that data, set the left and right channel initial settings before turning off the mute function.

f_O (Center Frequency) Characteristics

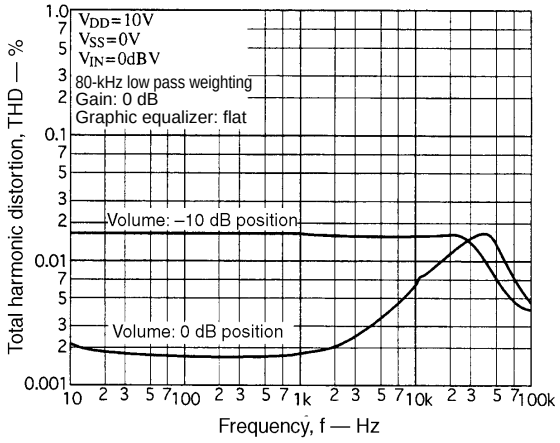


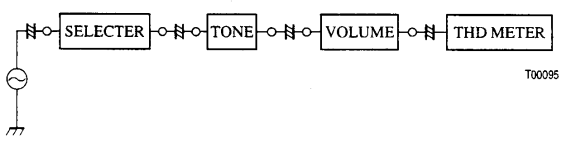
Volume Step Characteristics



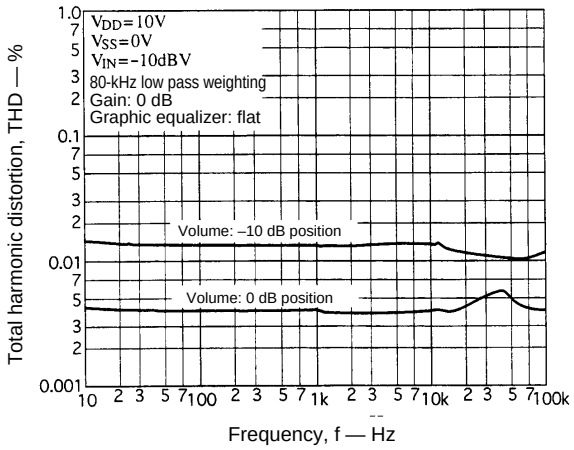


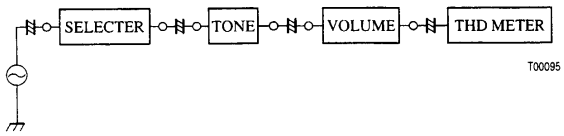
THD – Frequency Characteristics (1)



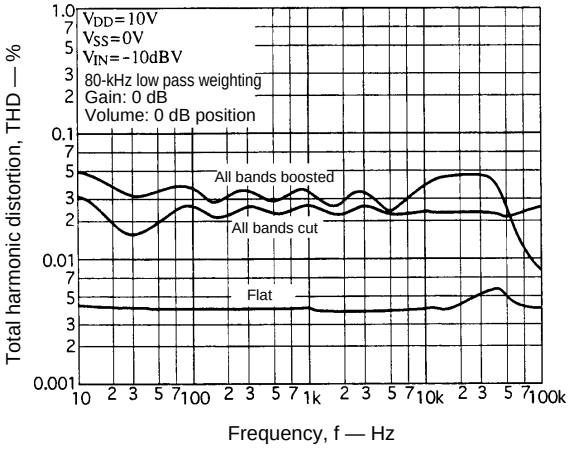


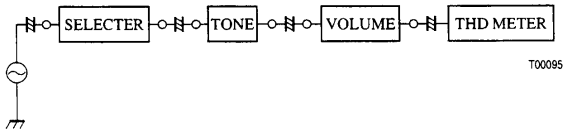
THD – Frequency Characteristics (2)



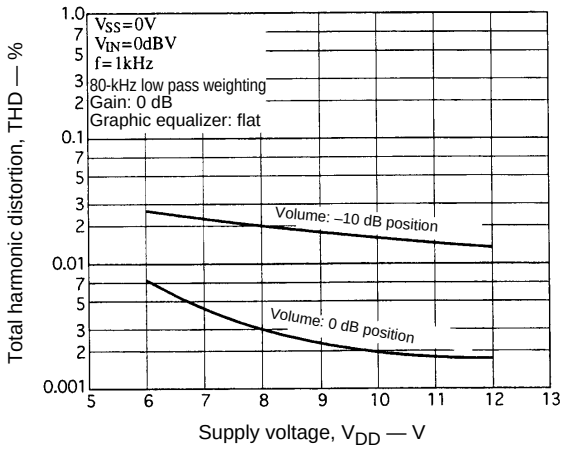


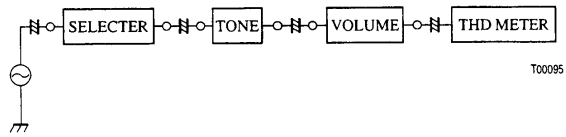
THD – Frequency Characteristics (3)



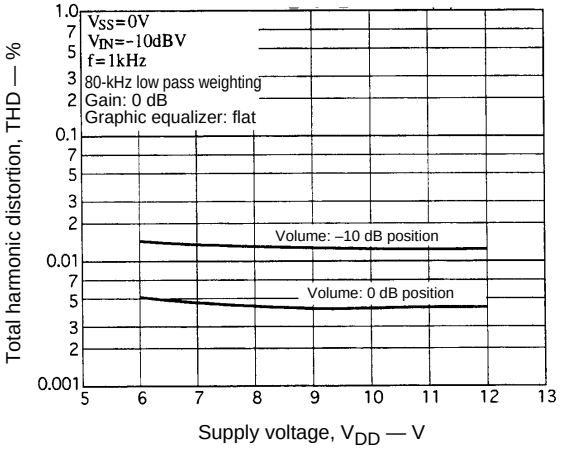


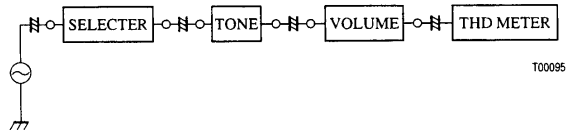
THD – Supply Voltage Characteristics (1)



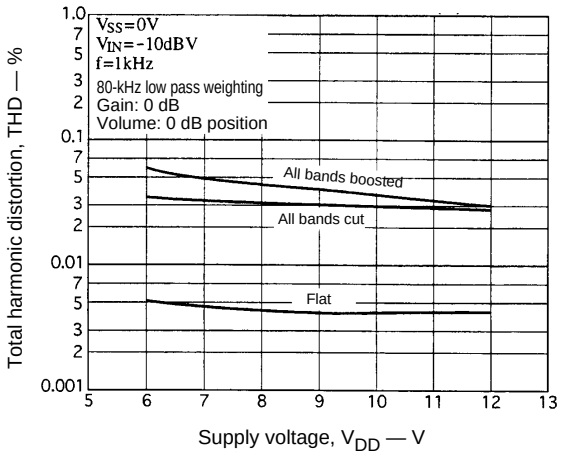


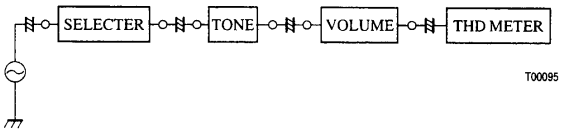
THD – Supply Voltage Characteristics (1)



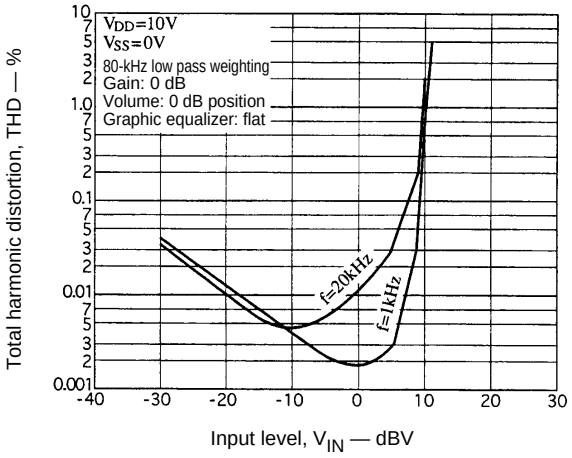


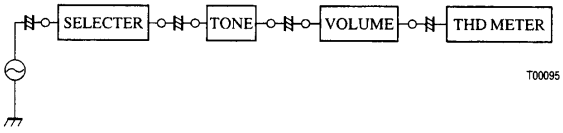
THD – Supply Voltage Characteristics (3)



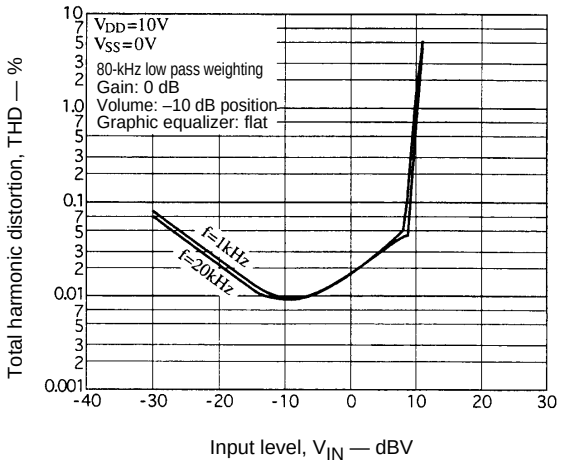


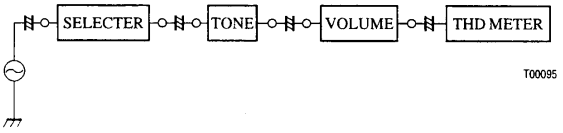
THD – Input Level Characteristics (1)



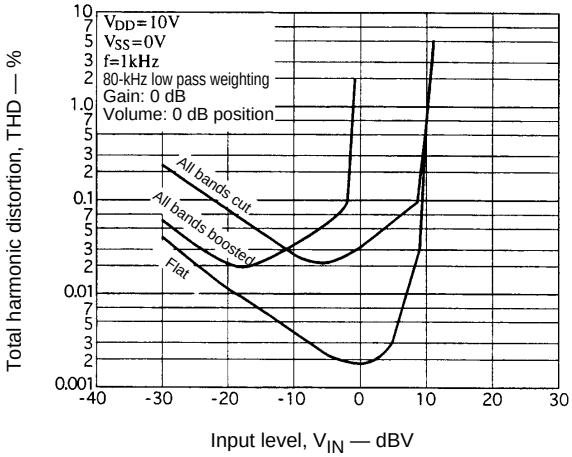


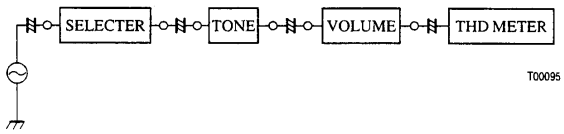
THD – Input Level Characteristics (2)



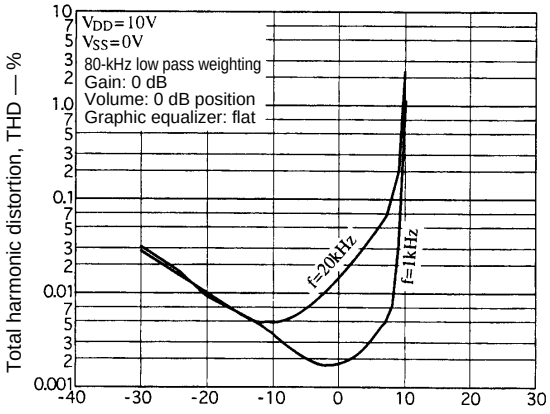


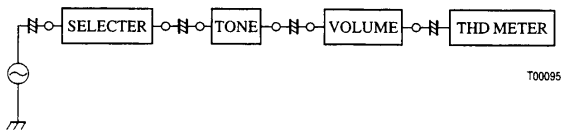
THD – Input Level Characteristics (3)



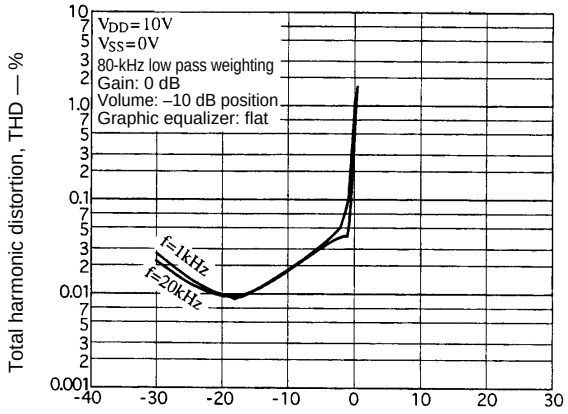


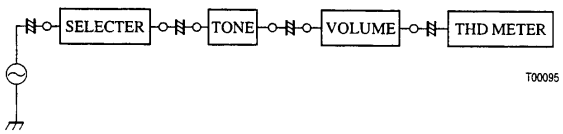
THD – Output Level Characteristics (1)



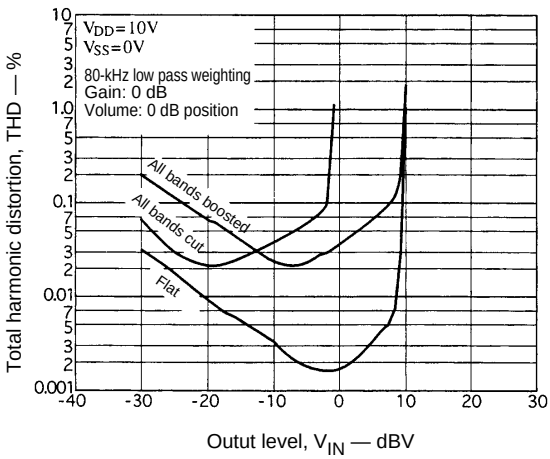


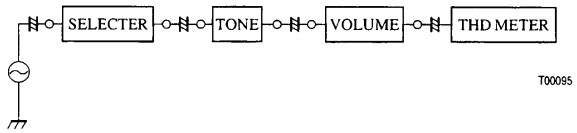
THD – Output Level Characteristics (2)





THD – Output Level Characteristics (3)





Usage Notes

- When the power is first applied, the internal analog switches are in indeterminate states. The chip therefore requires muting or other external measures until it has received the proper data.
- After power is first applied, applications must initialize this chip by sending the initial data (1) and (2) described below.

  Initial data ... (1) Address 01000001
  Data: (Set the volume to –∞, set both D34 and D35 to 0, and set all other data to 0)
  (2) Address 01000001
  Data: (Set the volume to –∞, set both D34 and D35 to 1, and set all other data to 0)

  After transferring that data, set the left and right channel initial settings before turning off the mute function.
- Provide grounding patterns or shielding for the lines to the CL, DI, and CE pins so as to prevent their high-frequency digital signals from interfering with the operation of nearby analog circuits.

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