Ordering number : EN5289A

SANYO Semiconductors

DATA SHEET

LC75883E
LC75883W

CMOS LSI

1/3-Duty LCD Display Drivers with Key Input Function

Overview

The LC75883E and LC75883W are 1/3-duty dynamic LCD display drivers that can directly drive LCDs with up to 171 segments and can control up to four general-purpose output ports. These LSIs also incorporate a key-scan circuit that accepts input from up to 30 keys to reduce the number of lines required between printed circuit boards.

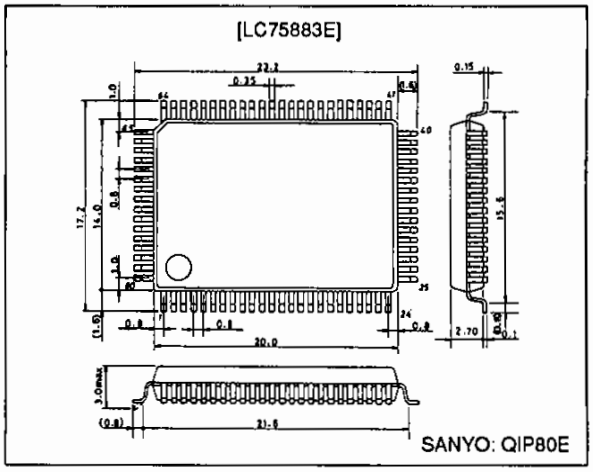
Features

- Supports input from up to 30 keys (This circuit only performs key scans when keys are pressed.)
- The 1/3-duty 1/2-bias and 1/3-duty 1/3-bias drive schemes can be controlled from serial data (for up to 171 segments).
- Sleep mode and forced all segments off function can be controlled from serial data.
- Segment output port and general-purpose output port function switching can be controlled from serial data.
- Serial data I/O supports CCB format communication with the system controller.
- Display data is displayed directly without the intervention of a decoder for high generality.
- Built-in voltage detection type reset circuit allows incorrect displays to be prevented.
- $\overline{\text{RES}}$ pin provided for forcibly initializing the LSI internal circuits.
- RC oscillator circuit

Package Dimensions

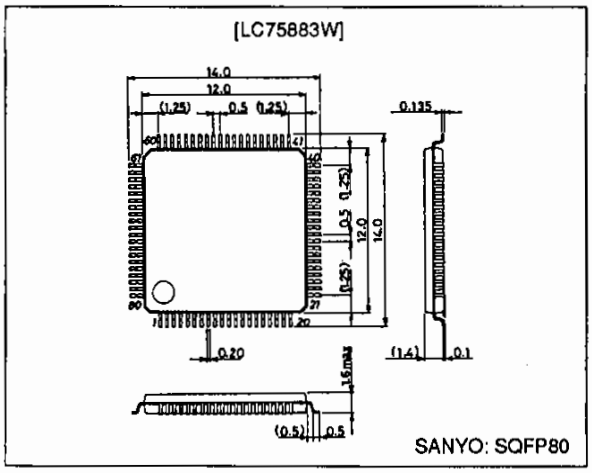
unit: mm

3174-QFP80E



unit: mm

3220-SQFP80



- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +7.0	V
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{RES}$	−0.3 to +7.0	V
	$V_{IN}2$	OSC, KI1 to KI5, TEST, $V_{DD}1$, $V_{DD}2$	−0.3 to V_{DD} + 0.3	V
Output voltage	$V_{OUT}1$	DO	−0.3 to +7.0	V
	$V_{OUT}2$	OSC, S1 to S57, COM1 to COM3, KS1 to KS6, P1 to P4	−0.3 to V_{DD} + 0.3	V
Output current	$I_{OUT}1$	S1 to S57	300	μA
	$I_{OUT}2$	COM1 to COM3	3	mA
	$I_{OUT}3$	KS1 to KS6	1	mA
	$I_{OUT}4$	P1 to P4	5	mA
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

Allowable Operating Ranges at Ta = −40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	4.5		6.0	V
Input voltage	$V_{DD}1$	$V_{DD}1$		2/3 V_{DD}	V_{DD}	V
	$V_{DD}2$	$V_{DD}2$		1/3 V_{DD}	V_{DD}	V
Input high-level voltage	$V_{IH}1$	CE, CL, DI, $\overline{RES}$	0.8 V_{DD}		6.0	V
	$V_{IH}2$	KI1 to KI5	0.6 V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL}	CE, CL, DI, $\overline{RES}$, KI1 to KI5	0		0.2 V_{DD}	V
Recommended external resistance	R_{OSC}	OSC		68		kΩ
Recommended external capacitance	C_{OSC}	OSC		820		pF
Guaranteed oscillator range	f_{OSC}	OSC	19	38	76	kHz
Data setup time	t_{ds}	CL, DI: Figure 2	160			ns
Data hold time	t_{dh}	CL, DI: Figure 2	160			ns
CE wait time	t_{cp}	CE, CL: Figure 2	160			ns
CE setup time	t_{cs}	CE, CL: Figure 2	160			ns
CE hold time	t_{ch}	CE, CL: Figure 2	160			ns
High-level clock pulse width	t_{wH}	CL: Figure 2	160			ns
Low-level clock pulse width	t_{wL}	CL: Figure 2	160			ns
Rise time	t_r	CE, CL, DI: Figure 2		160		ns
Fall time	t_f	CE, CL, DI: Figure 2		160		ns
DO output delay time	t_{dc}	DO, R_{PU} = 4.7 kΩ, C_L = 10 pF*1: Figure 2			1.5	μs
DO rise time	t_{dr}	DO, R_{PU} = 4.7 kΩ, C_L = 10 pF*1: Figure 2			1.5	μs

Note: *1. Since DO is an open drain output, these values vary with the values of the pull-up resistor R_{PU} and the load capacitance C_L.

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Hysteresis	V_H	CE, CL, DI, $\overline{RES}$, KI1 to KI5		0.1 V_{DD}		V
Power-down detection voltage	V_{DET}		2.7	3.0	3.3	V
Input high-level current	I_{IH}	CE, CL, DI, $\overline{RES}$: V_I = 6.0 V			5.0	μA
Input low-level current	I_{IL}	CE, CL, DI, $\overline{RES}$: V_I = 0 V	–5.0			μA
Input floating voltage	V_{IF}	KI1 to KI5			0.05 V_{DD}	V
Pull-down resistance	R_{PD}	KI1 to KI5: V_{DD} = 5.0 V	50	100	250	kΩ
Output off leakage current	I_{OFFH}	DO: V_O = 6.0 V			6.0	μA
Output high-level voltage	$V_{OH}1$	KS1 to KS6: I_O = –500 μA	V_{DD} – 1.2	V_{DD} – 0.5	V_{DD} – 0.2	V
	$V_{OH}2$	P1 to P4: I_O = –1 mA	V_{DD} – 1.0			V
	$V_{OH}3$	S1 to S57: I_O = –20 μA	V_{DD} – 1.0			V
	$V_{OH}4$	COM1 to COM3: I_O = –100 μA	V_{DD} – 1.0			V
Output low-level voltage	$V_{OL}1$	KS1 to KS6: I_O = 25 μA	0.2	0.5	1.5	V
	$V_{OL}2$	P1 to P4: I_O = 1 mA			1.0	V
	$V_{OL}3$	S1 to S57: I_O = 20 μA			1.0	V
	$V_{OL}4$	COM1 to COM3: I_O = 100 μA			1.0	V
	$V_{OL}5$	DO: I_O = 1 mA		0.1	0.5	V
Output middle-level voltage*2	$V_{MID}1$	COM1 to COM3: 1/2 bias, I_O = ±100 μA	1/2 V_{DD} – 1.0		1/2 V_{DD} + 1.0	V
	$V_{MID}2$	S1 to S57: 1/3 bias, I_O = ±20 μA	2/3 V_{DD} – 1.0		2/3 V_{DD} + 1.0	V
	$V_{MID}3$	S1 to S57: 1/3 bias, I_O = ±20 μA	1/3 V_{DD} – 1.0		1/3 V_{DD} + 1.0	V
	$V_{MID}4$	COM1 to COM3: 1/3 bias, I_O = ±100 μA	2/3 V_{DD} – 1.0		2/3 V_{DD} + 1.0	V
	$V_{MID}5$	COM1 to COM3: 1/3 bias, I_O = ±100 μA	1/3 V_{DD} – 1.0		1/3 V_{DD} + 1.0	V
Oscillator frequency	f_{OSC}	OSC: R_{OSC} = 68 kΩ, C_{OSC} = 820 pF	30.4	38	45.6	kHz
Current drain	$I_{DD}1$	Sleep mode			100	μA
	$I_{DD}2$	V_{DD} = 6.0 V, output open, 1/2 bias, f_{OSC} = 38 kHz		230	460	μA
	$I_{DD}3$	V_{DD} = 6.0 V, output open, 1/3 bias, f_{OSC} = 38 kHz		200	400	μA

Note: *2. Excluding the bias voltage generation divider resistors built in the $V_{DD}1$ and $V_{DD}2$.

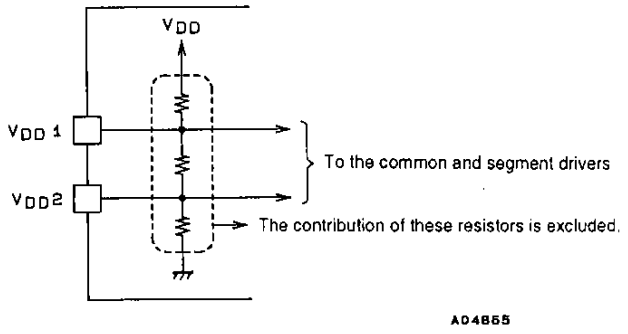
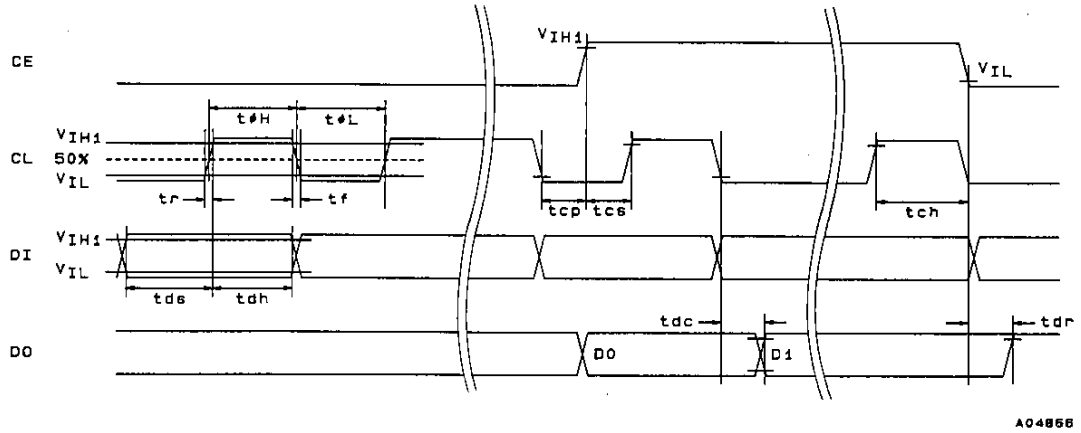


Figure 1

1. When CL is stopped at the low level



2. When CL is stopped at the high level

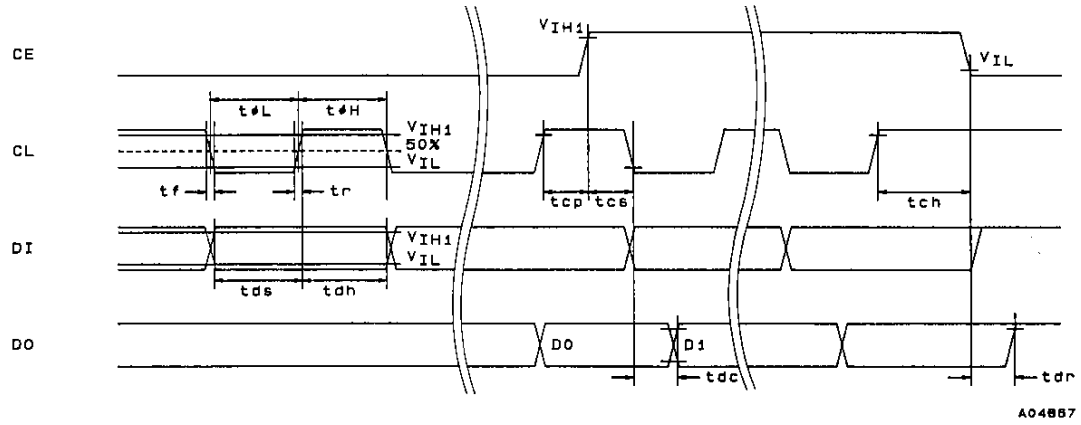
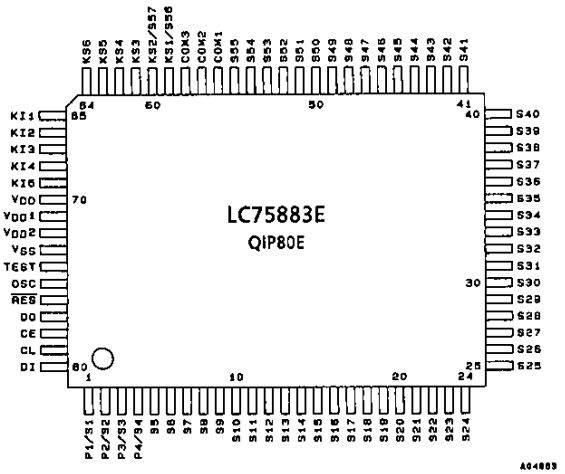
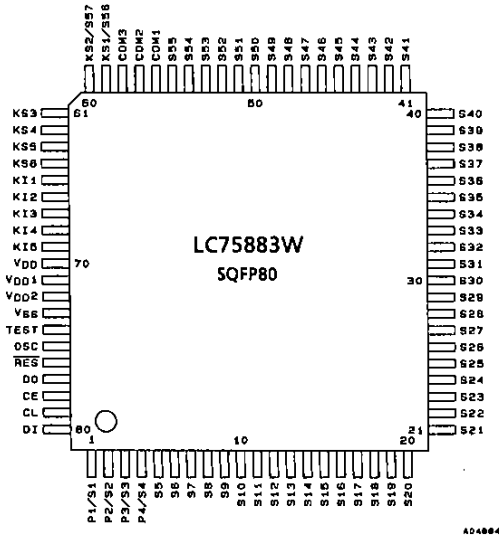


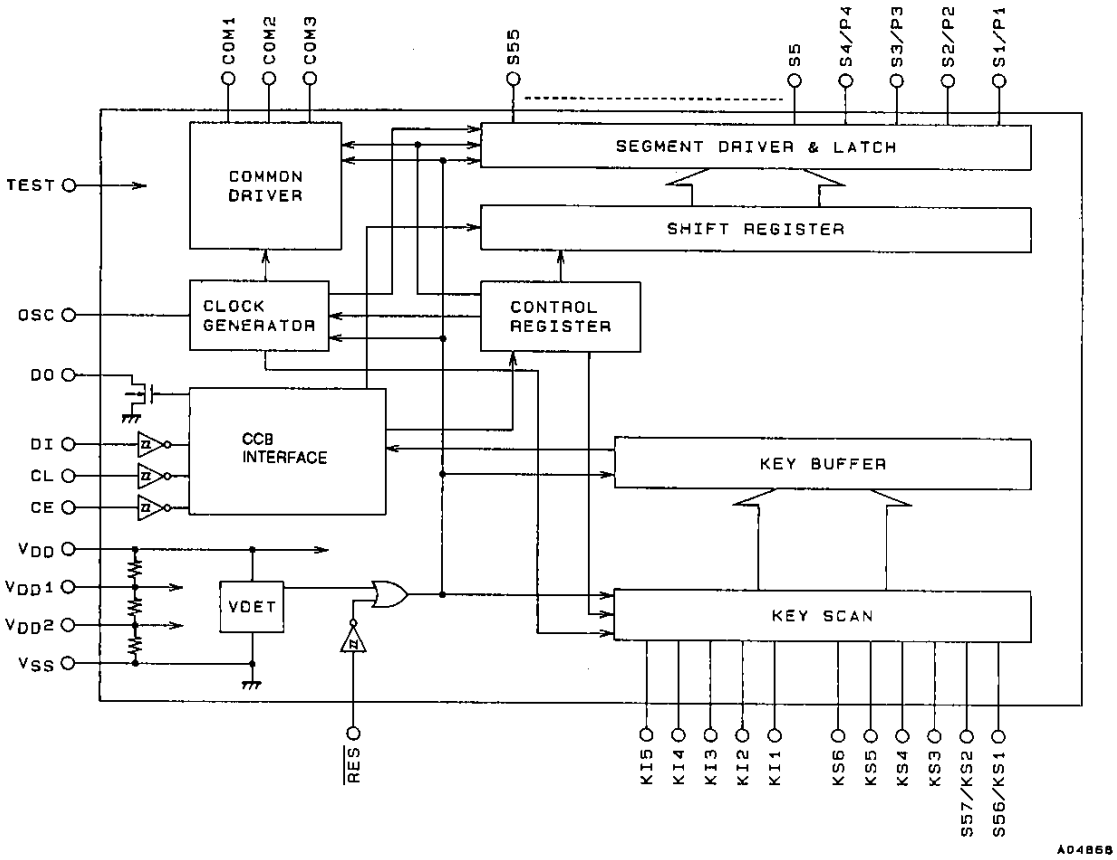
Figure 2

Pin Assignments





Block Diagram

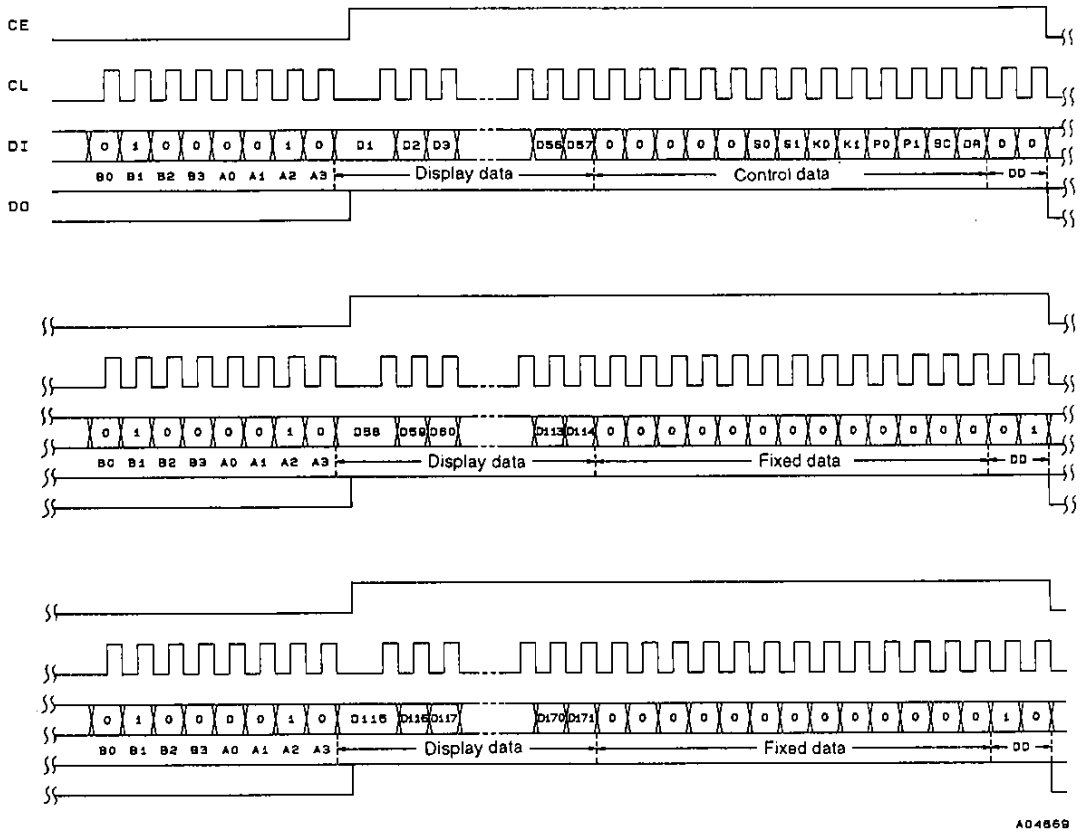


Pin Functions

Pin No.	Symbol	Function	Active	I/O	Handling when unused
1 to 4 5 to 55	S1/P1 to S4/P4 S5 to S55	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports under serial data control.	—	O	Open
56 57 58	COM1 COM2 COM3	Common driver outputs The frame frequency f_O is given by: $f_O = (f_{OSC}/384)$ Hz.	—	O	Open
59, 60, 61 to 64	KS1/S56, KS2/S57, KS3 to KS6	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S56 and KS2/S57 pins can be used as segment outputs when so specified by the control data.	—	O	Open
65 to 69	KI1 to KI5	Key scan inputs These pins have built-in pull-down resistors.	H	I	GND
75	OSC	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor at this pin.	—	I/O	V_{DD}
78	CE	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. CE: Chip enable CL: Synchronization clock DI: Transfer data DO: Data out	H	I	GND
79	CL		↓	I	
80	DI		—	I	
77	DO		—	O	Open
76	$\overline{RES}$	Reset signal input $\overline{RES}$ = low .....Display off Key scan disabled All key data is reset to low $\overline{RES}$ = high .....Display on Key scan enabled However, serial data can be transferred when $\overline{RES}$ is low.	L	I	V_{DD}
74	TEST	This pin must be connected to ground.	—	I	—
71	$V_{DD}1$	Used for applying the LCD drive 2/3 bias voltage externally. Must be connected to $V_{DD}2$ when a 1/2 bias drive scheme is used.	—	I	Open
72	$V_{DD}2$	Used for applying the LCD drive 1/3 bias voltage externally. Must be connected to $V_{DD}1$ when a 1/2 bias drive scheme is used.	—	I	Open
70	V_{DD}	Power supply connection. Provide a voltage of between 4.5 and 6.0 V.	—	—	—
73	V_{SS}	Power supply connection. Connect to ground.	—	—	—

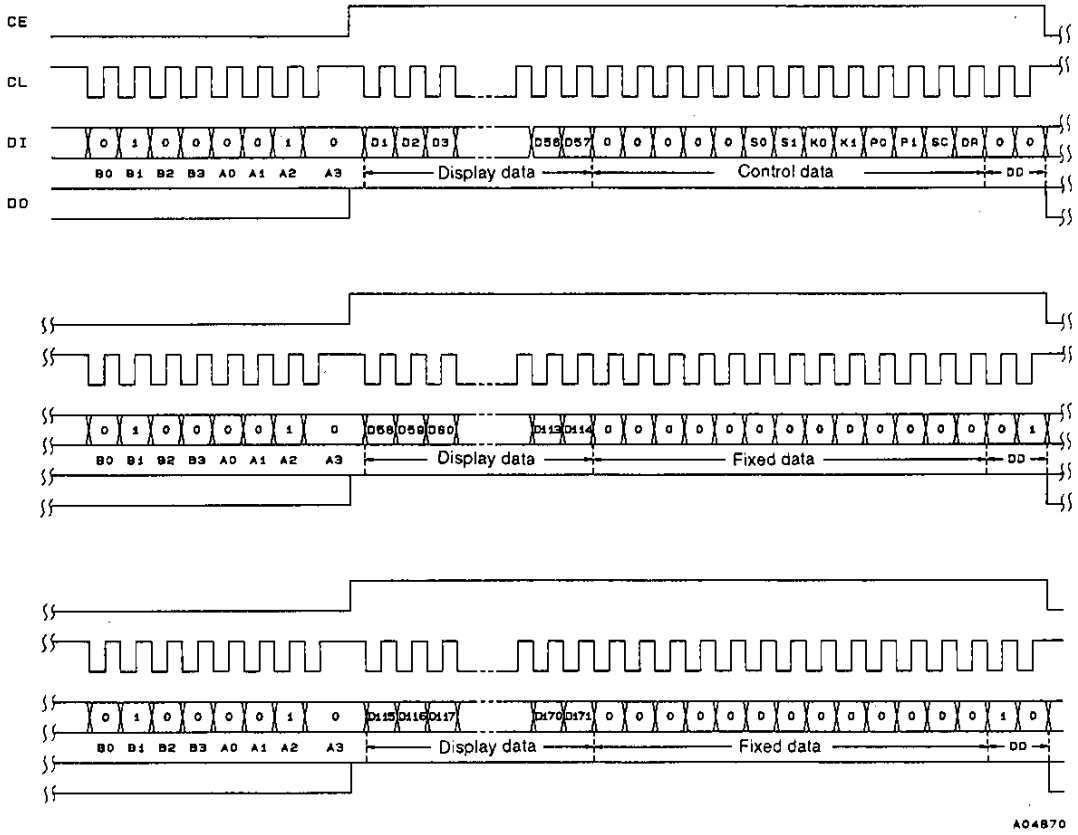
Serial Data Input

1. When CL is stopped at the low level



Note: DD: Direction data

2. When CL is stopped at the high level



Note: DD: Direction data

- CCB address.....42H
- D1 to D171.....Display data
- S0, S1 .....Sleep control data
- K0, K1.....Key scan output/segment output selection data
- P0, P1 .....Segment output port/general-purpose output port selection data
- SC.....Segment on/off control data
- DR .....1/2 bias or 1/3 bias drive selection data

Control Data Functions

1. S0, S1: Sleep control data
   These control data bits switch between normal mode and sleep mode and set the states of the KS1 to KS6 key scan outputs during key scan standby.

Control data		Mode	OSC oscillator	Segment outputs Common outputs	Output pin states during key scan standby					
S0	S1				KS1	KS2	KS3	KS4	KS5	KS6
0	0	Normal	Operating	Operating	H	H	H	H	H	H
0	1	Sleep	Stopped	L	L	L	L	L	L	H
1	0	Sleep	Stopped	L	L	L	L	L	H	H
1	1	Sleep	Stopped	L	H	H	H	H	H	H

Note: This assumes that the KS1/S56 and KS2/S57 output pins are selected for key scan output.

2. K0, K1: Key scan output/segment output selection data
These control data bits switch the functions of the KS1/S56 and KS2/S57 output pins between key scan output and segment output.

Control data		Output pin state		Maximum number of input keys
K0	K1	KS1/S56	KS2/S57	
0	0	KS1	KS2	30
0	1	S56	KS2	25
1	X	S56	S57	20

X: don't care
Note: KSn (n = 1 or 2): Key scan output
Sn (n = 56 or 57): Segment output

3. P0, P1: Segment output port/general-purpose output port selection data
These control data bits switch the functions of the S1/P1 to S4/P4 output pins between the segment output port function and the general-purpose output port function.

Control data		Output pin state			
P0	P1	S1/P1	S2/P2	S3/P3	S4/P4
0	0	S1	S2	S3	S4
0	1	P1	P2	S3	S4
1	0	P1	P2	P3	S4
1	1	P1	P2	P3	P4

Note: Sn (n = 1 to 4): Segment output port
Pn (n = 1 to 4): General-purpose output port

The table below lists the correspondence between the display data and the output pins when these pins are selected to be general-purpose output ports.

Output pin	Corresponding display data
S1/P1	D1
S2/P2	D4
S3/P3	D7
S4/P4	D10

For example, if the S4/P4 output pin is selected to be a general-purpose output port, the S4/P4 output pin will output a high level when the display data D10 is 1, and a low level when D10 is 0.

4. SC: Segment on/off control data
This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

5. DR: 1/2 bias or 1/3 bias drive selection data
This control data bit switches between LCD 1/2-bias or 1/3-bias drive.

DR	Drive scheme
0	1/3 bias drive
1	1/2 bias drive

Display Data and Output Pin Correspondence

Output pin	COM1	COM2	COM3
S1/P1	D1	D2	D3
S2/P2	D4	D5	D6
S3/P3	D7	D8	D9
S4/P4	D10	D11	D12
S5	D13	D14	D15
S6	D16	D17	D18
S7	D19	D20	D21
S8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90

Output pin	COM1	COM2	COM3
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156
S53	D157	D158	D159
S54	D160	D161	D162
S55	D163	D164	D165
KS1/S56	D166	D167	D168
KS2/S57	D169	D170	D171

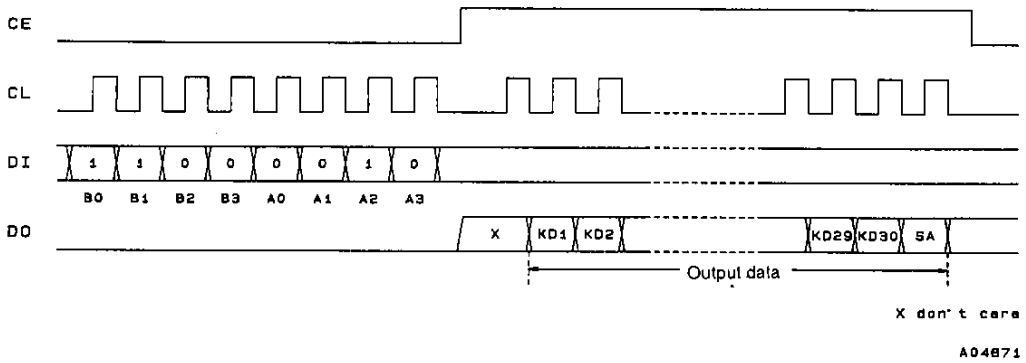
Note: This is for the case where the output pins S1/P1 to S4/P4, KS1/S56 and KS2/S57 are selected for use as segment outputs.

For example, the table below lists the segment output states for the S11 output pin.

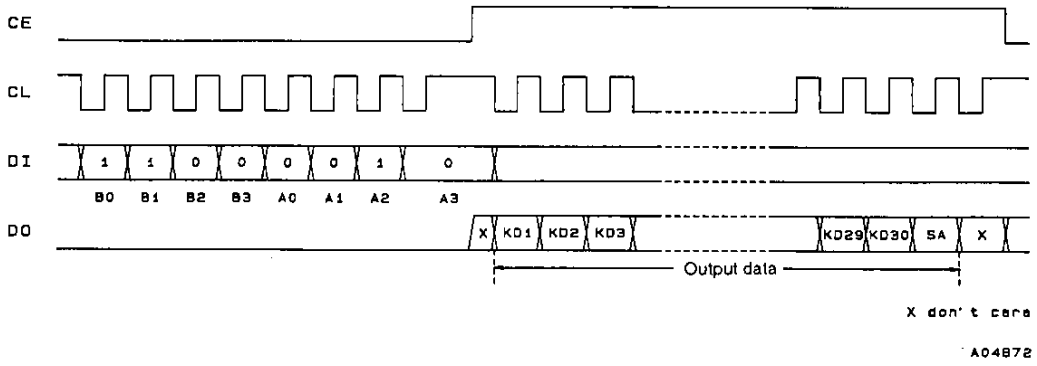
Display data			Output pin (S11) state
D31	D32	D33	
0	0	0	The LCD segments for COM1, COM2 and COM3 are off.
0	0	1	The LCD segment for COM3 is on (lit).
0	1	0	The LCD segment for COM2 is on.
0	1	1	The LCD segments for COM2 and COM3 are on.
1	0	0	The LCD segment for COM1 is on.
1	0	1	The LCD segments for COM1 and COM3 are on.
1	1	0	The LCD segments for COM1 and COM2 are on.
1	1	1	The LCD segments for COM1, COM2 and COM3 are on.

Serial Data Output

1. When CL is stopped at the low level



2. When CL is stopped at the high level



- CCB address.....43H
- KD1 to KD30....Key data
- SA .....Sleep acknowledge data

Note: If a key data read operation is executed when DO is high, the key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

Output Data

1. KD1 to KD30: Key data
   When a key matrix of up to 30 keys is formed using the KS1 to KS6 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

	KI1	KI2	KI3	KI4	KI5
KS1/S56	KD1	KD2	KD3	KD4	KD5
KS2/S57	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

   When the KS1/S56 and KS2/S57 output pins are selected to be segment outputs by control data bits K0 and K1 and a key matrix of up to 20 keys is formed using the KS3 to KS6 output pins and the KI1 to KI5 input pins, the KD1 to KD10 key data bits will be set to 0.

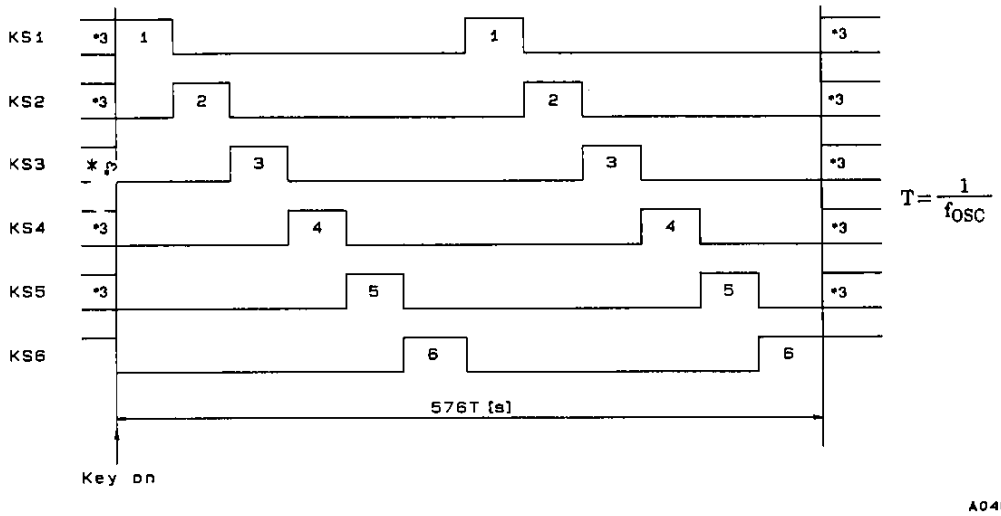
2. SA: Sleep acknowledge data
   This output data bit is set to the state when the key was pressed. Also, while DO will be low in this case, if serial data is input and the mode is set (to normal or sleep mode) during this period, that mode will be set. SA will be 1 in sleep mode and 0 in normal mode.

Sleep Mode Function

Sleep mode is set up by setting either S0 or S1 in the control data to 1. The segment outputs will all go low and the common outputs will also go low, and the oscillator on the OSC pin will stop (although it will be restarted by a key press). This reduces power dissipation. This mode is cleared by sending control data with both S0 and S1 set to 0. However, note that the S1/P1 to S4/P4 outputs can be used as general-purpose output ports according to the state of the P0 and P1 control data bits, even in sleep mode. (See the control data description for details.)

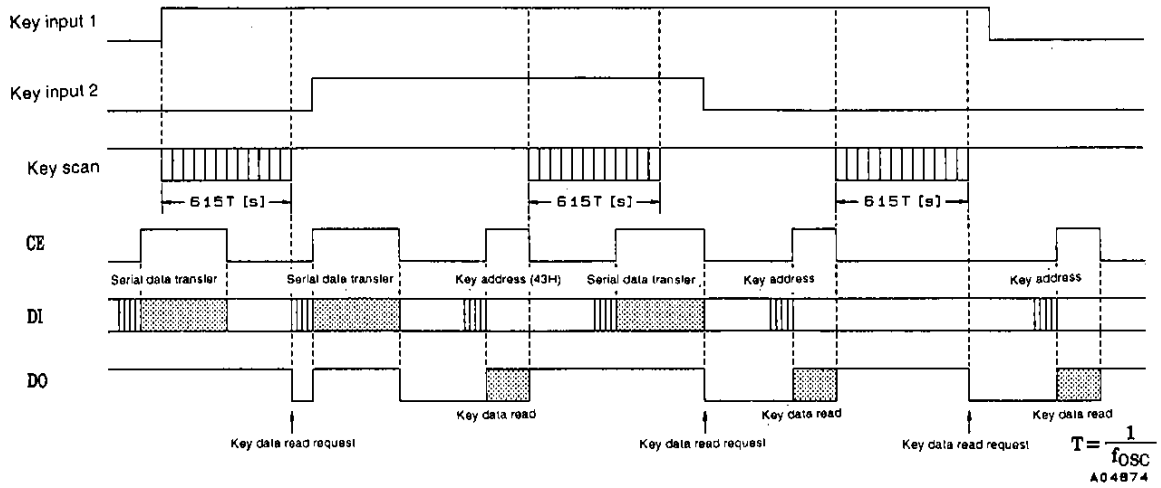
Key Scan Operation Functions

1. Key scan timing
   The key scan period is 288·T (s). To reliably determine the on/off state of the keys, the LC75883E/W scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on DO) 615·T (s) after starting a key scan. If the key data does not agree and a key was pressed at that point, it scans the keys again. Thus the LC75883E/W cannot detect a key press shorter than 615·T (s).



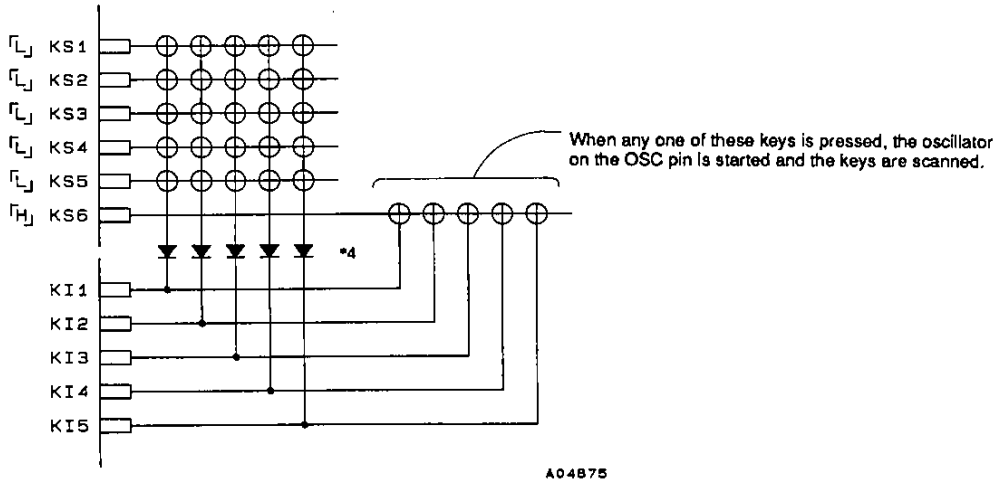
Note: *3. In sleep mode the high/low state of these pins is determined by the S0 and S1 bits in the control data. Key scan output signals are not output from pins that are set low.

2. In normal mode
   - The pins KS1 to KS6 are set high.
   - When a key is pressed a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
   - If a key is pressed for longer than 615·T (s) (where $T = \frac{1}{f_{OSC}}$) the LC75883E/W outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
   - After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75883E/W performs another key scan. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 and 10 kΩ).

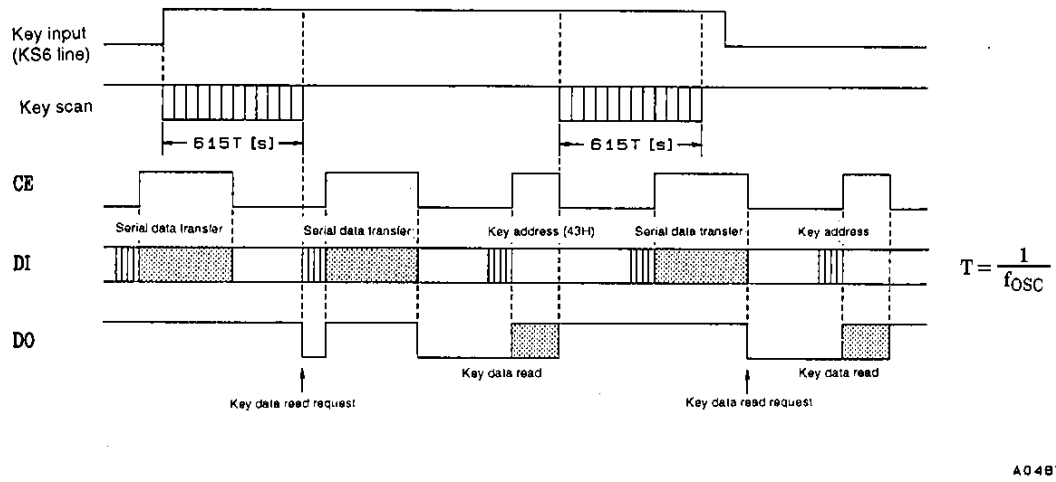


3. In sleep mode
   - The pins KS1 to KS6 are set to high or low by the S0 and S1 bits in the control data. (See the control data description for details.)
   - If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, the oscillator on the OSC pin is started and a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
   - If a key is pressed for longer than 615·T (s) (where $T = \frac{1}{f_{OSC}}$) the LC75883E/W outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
   - After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75883E/W performs another key scan. However, this does not clear sleep mode. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 and 10 kΩ).
   - Sleep mode key scan example

   Example: S0 = 0, S1 = 1 (sleep with only KS6 high)



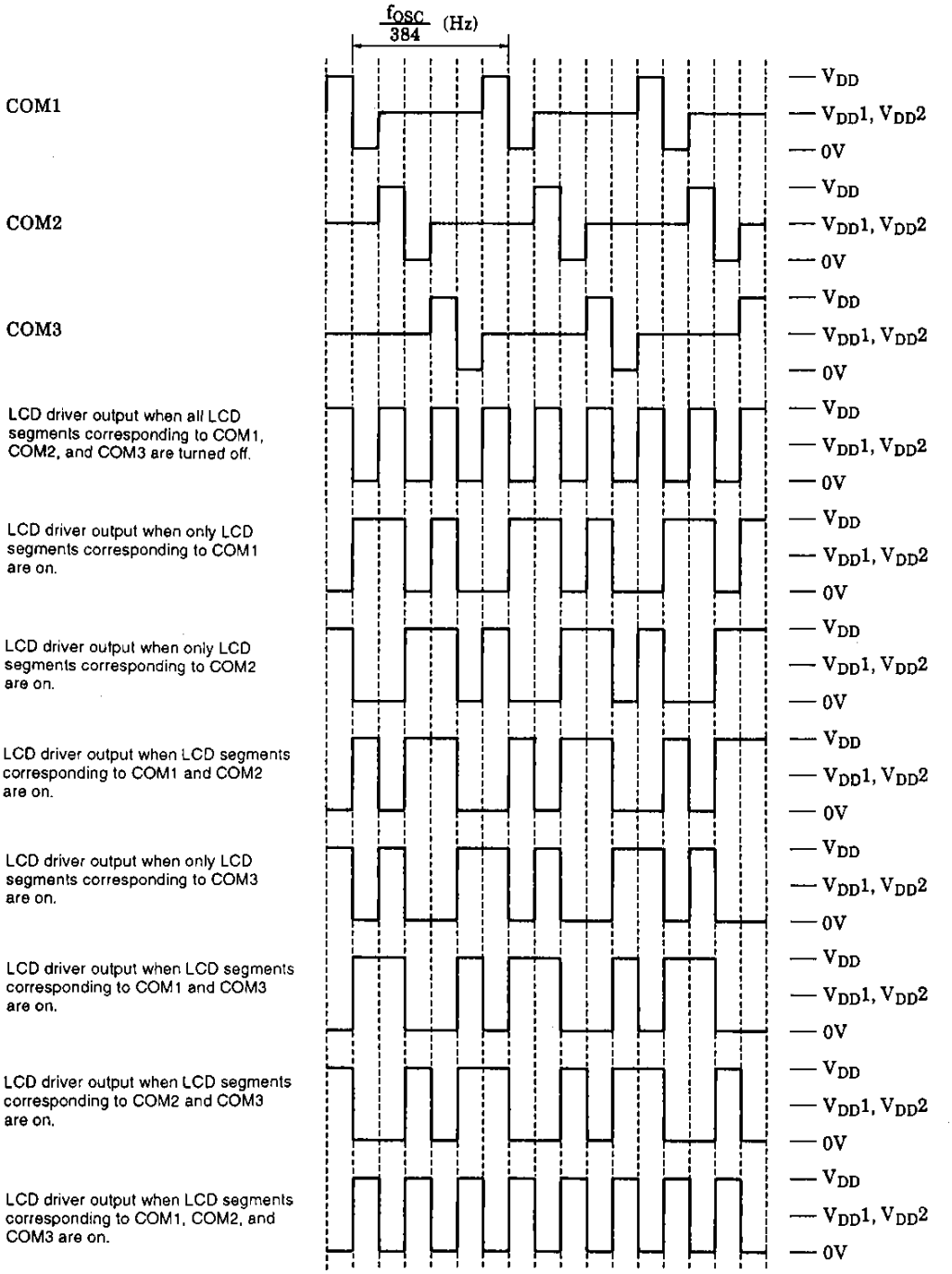
Note: *4. These diodes are required to reliably recognize multiple key presses on the KS6 line when sleep mode state with only KS6 high, as in the above example. That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.



Multiple key presses

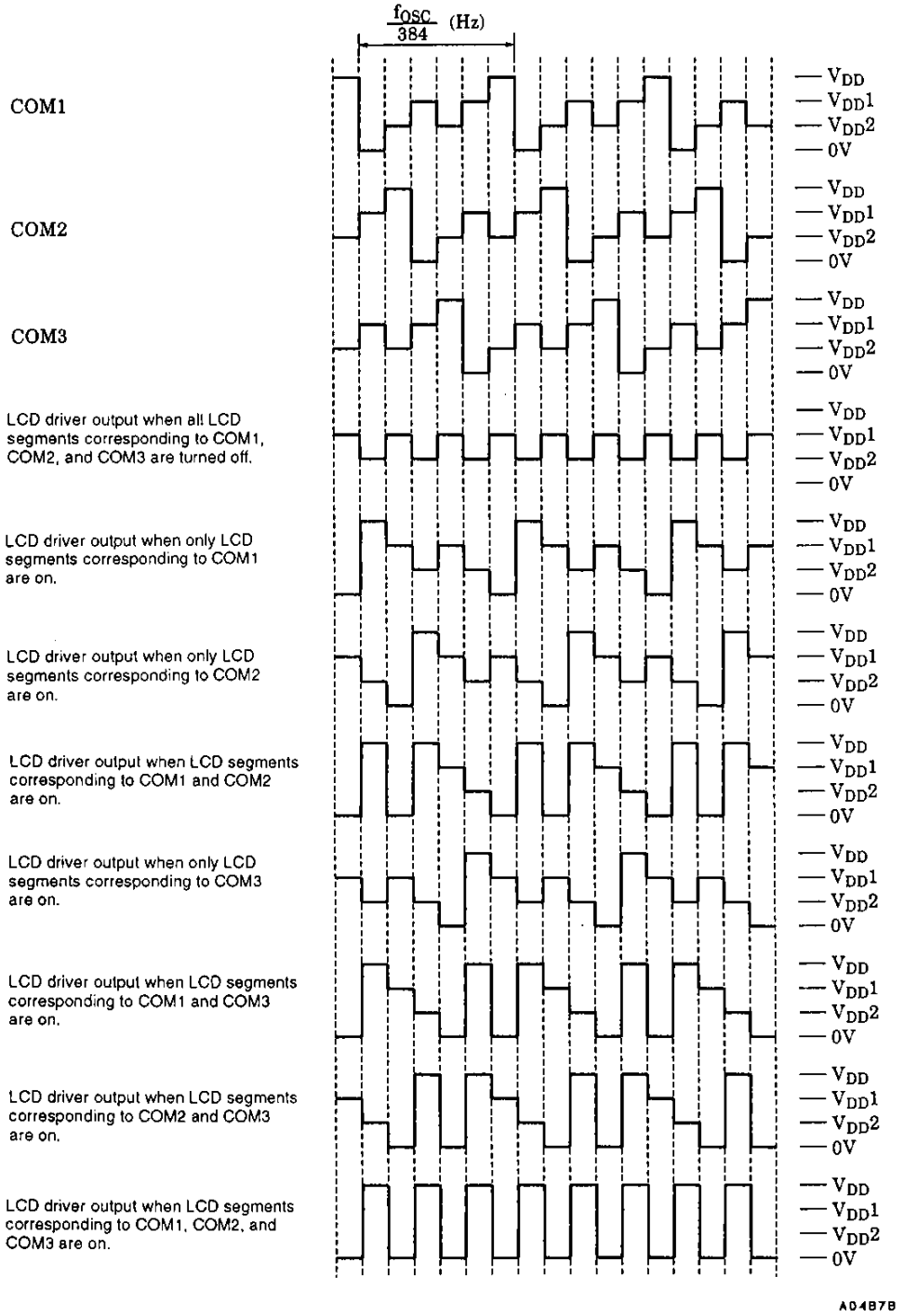
Although the LC75883E/W is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bits and ignore such data.

1/3-Duty - 1/2-Bias Drive Technique



1/3-Duty - 1/2-Bias Waveforms

1/3-Duty - 1/3-Bias Drive Technique



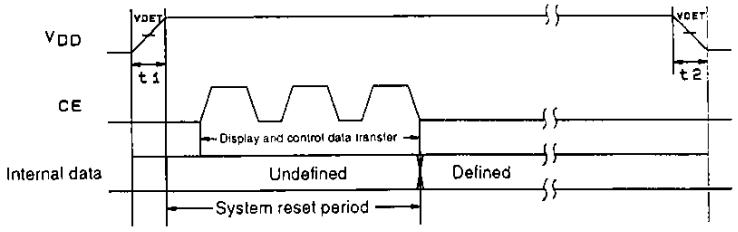
1/3-Duty - 1/3-Bias Waveforms

Voltage Detection Type Reset Circuit (VDET)

This circuit generates an output signal and resets the system when power is first applied and when the voltage drops, i.e., when the power supply voltage is less than or equal to the power down detection voltage VDET, which is 3.0 V, typical. To assure that this function operates reliably, a capacitor must be added to the power supply line so that the power supply voltage V_{DD} rise time when power is first applied and the power supply voltage V_{DD} fall time when the voltage drops are both at least 1 ms. (See Figure 3.)

System Reset

1. Reset methods
   The LC75883E/W supports the two reset methods described below. When a system reset is applied, display is turned off, key scanning is stopped, and all the key data is reset to low. When the reset is cleared, display is turned on and key scanning become possible.
   - Reset at power-on and power-down
     If at least 1 ms is assured as the supply voltage V_{DD} rise time when power is applied, a system reset will be applied by the VDET output signal when the supply voltage is brought up. If at least 1 ms is assured as the supply voltage V_{DD} fall time when power drops, a system reset will be applied in the same manner by the VDET output signal when the supply voltage is lowered. Note that the reset is cleared at the point when all the serial data (the display data D1 to D171 and the control data) has been transferred, i.e., on the fall of the CE signal on the transfer of the last direction data, after all the direction data has been transferred. However, the above operations will be performed regardless of the state (high or low) of the $\overline{RES}$ pin. If $\overline{RES}$ is high, the reset will be cleared at the point the above operations are completed. On the other hand, if $\overline{RES}$ is low, the system will remain in the reset period as long as $\overline{RES}$ is not set high, even if the above operations are completed. (See Figure 3.)



Power supply voltage V_{DD} rise time: t1 ≥ 1 ms
Power supply voltage V_{DD} fall time: t2 ≥ 1 ms

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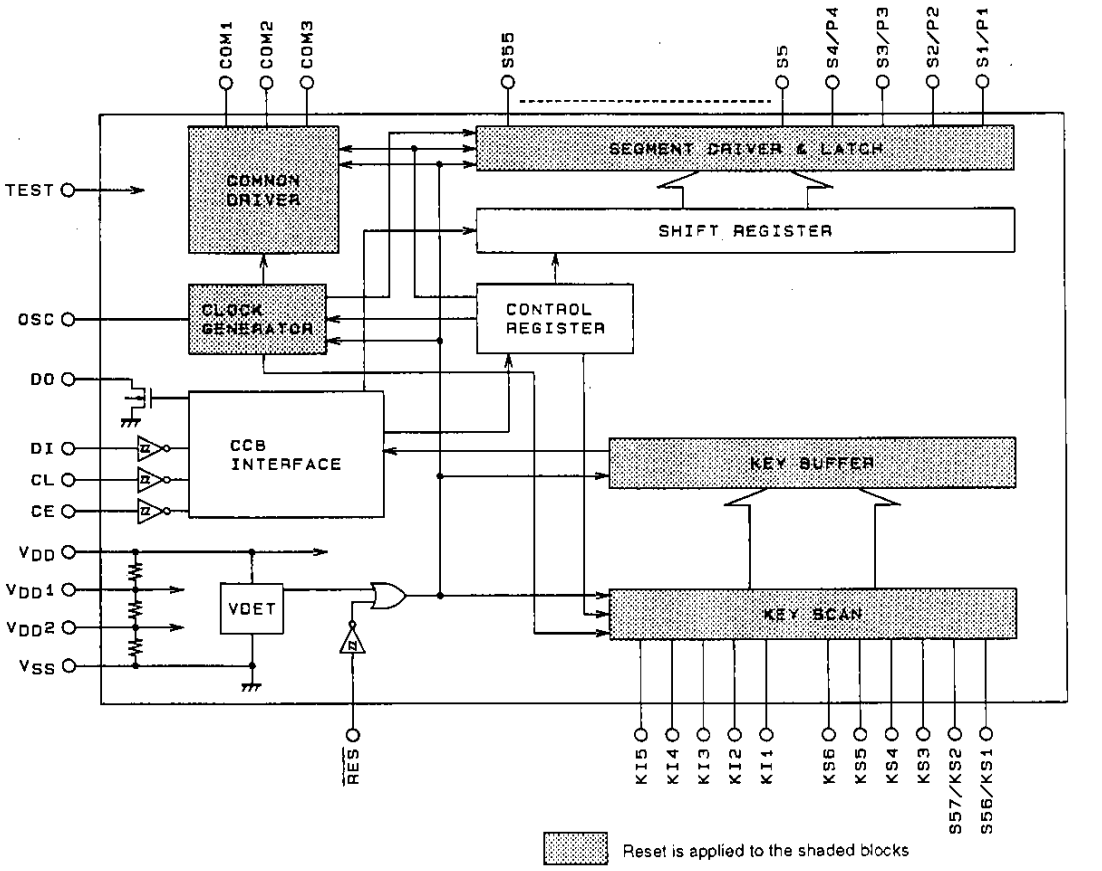
Figure 3

   - Reset when the power-supply voltage is in the allowable operating range (V_{DD} = 4.5 to 6.0 V)
     The system is reset when the $\overline{RES}$ pin is set low, and the reset is cleared by setting $\overline{RES}$ high.

2. LC75883E/W internal block states during the reset period
   - CLOCK GENERATOR
     Reset is applied and the base clock is stopped. However the OSC pin state (normal or sleep mode) is determined after the S0 and S1 control data bits are transferred.
   - COMMON DRIVERS, SEGMENT DRIVERS & LATCH
     Reset is applied and the display is turned off. However, display data can be input to the latch circuit in this state.
   - KEY SCAN
     Reset is applied, the circuit is set to the initial state, and at the same time the key scan operation is disabled.
   - KEY BUFFER
     Reset is applied and all the key data is set to low.
   - CCB INTERFACE, CONTROL REGISTER, SHIFT REGISTER
     Since serial data transfer is possible in the reset state, these circuits are not reset.



3. Output pin states during the reset period

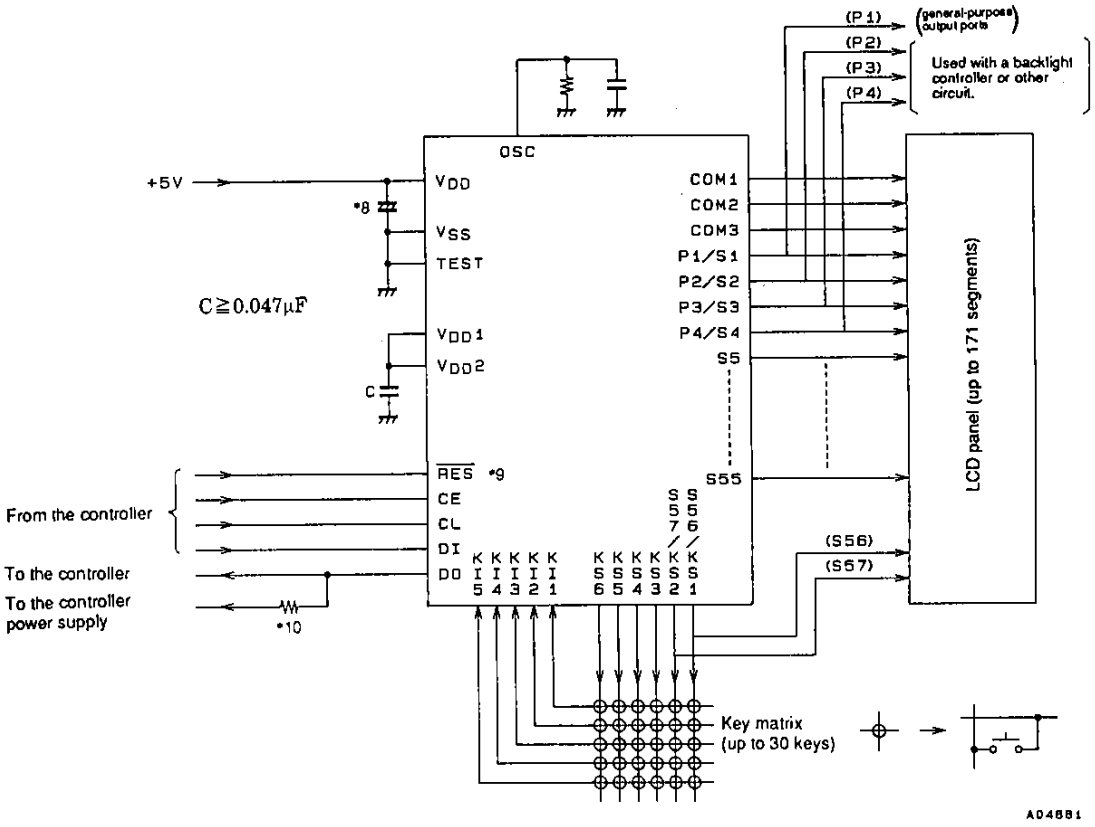
Output pin	State during reset
S1/P1 to S4/P4	L*5
S5 to S55	L
COM1 to COM3	L
KS1/S56, KS2/S57	L*5
KS3 to KS5	X*6
KS6	H
DO	H*7

X: Don't care

Note: *5. These output pins are forcibly set to the segment output function and held low.
*6. When power is first applied, the states of these output pins are undefined until the S0 and S1 control data bits have been transferred.
*7. Since this output pin is an open-drain output, a pull-up resistor of between 1 and 10 kΩ is required. This pin remains high during the reset period even if a key data read operation is performed.

Application Circuit Example 1

1/2 bias (for use with normal panels)



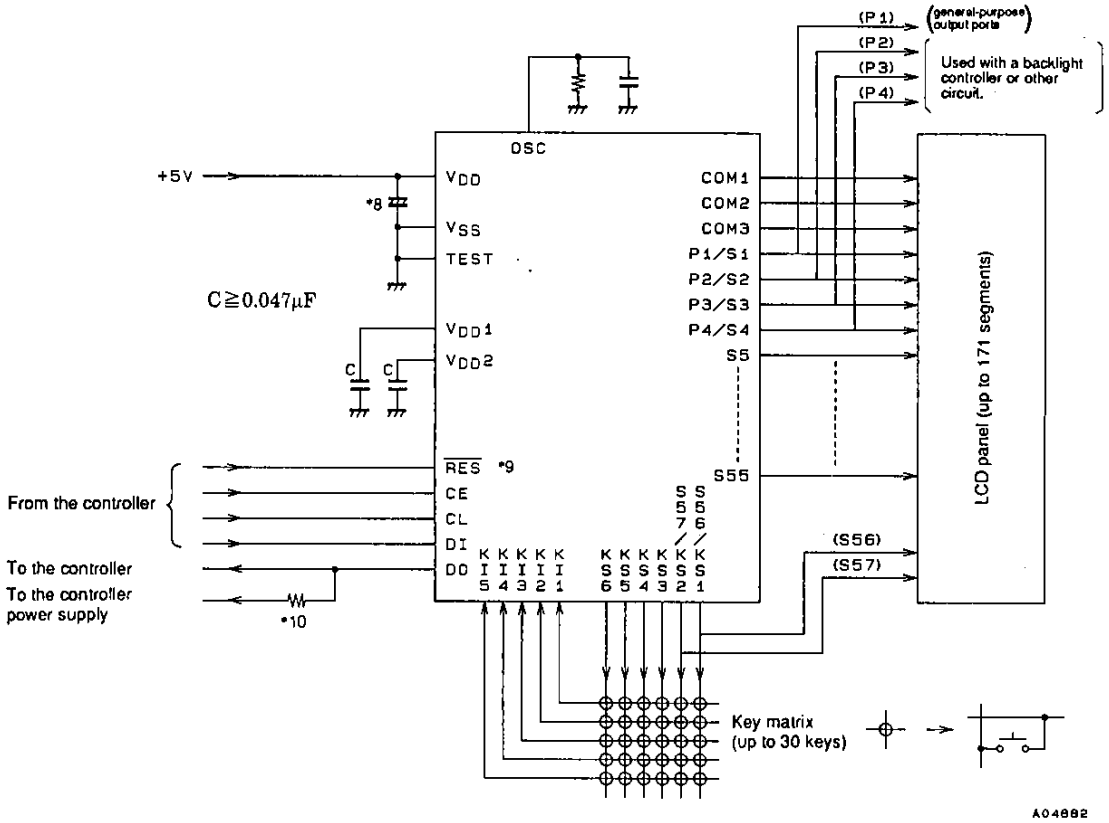
Note: *8. Add a capacitor to the power supply line so that the power supply voltage V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75883E/W is reset by the VDET.

*9. If the $\overline{RES}$ pin is not used for system reset, it must be connected to V_{DD}.

*10. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Application Circuit Example 2

1/3 bias (for use with normal panels)



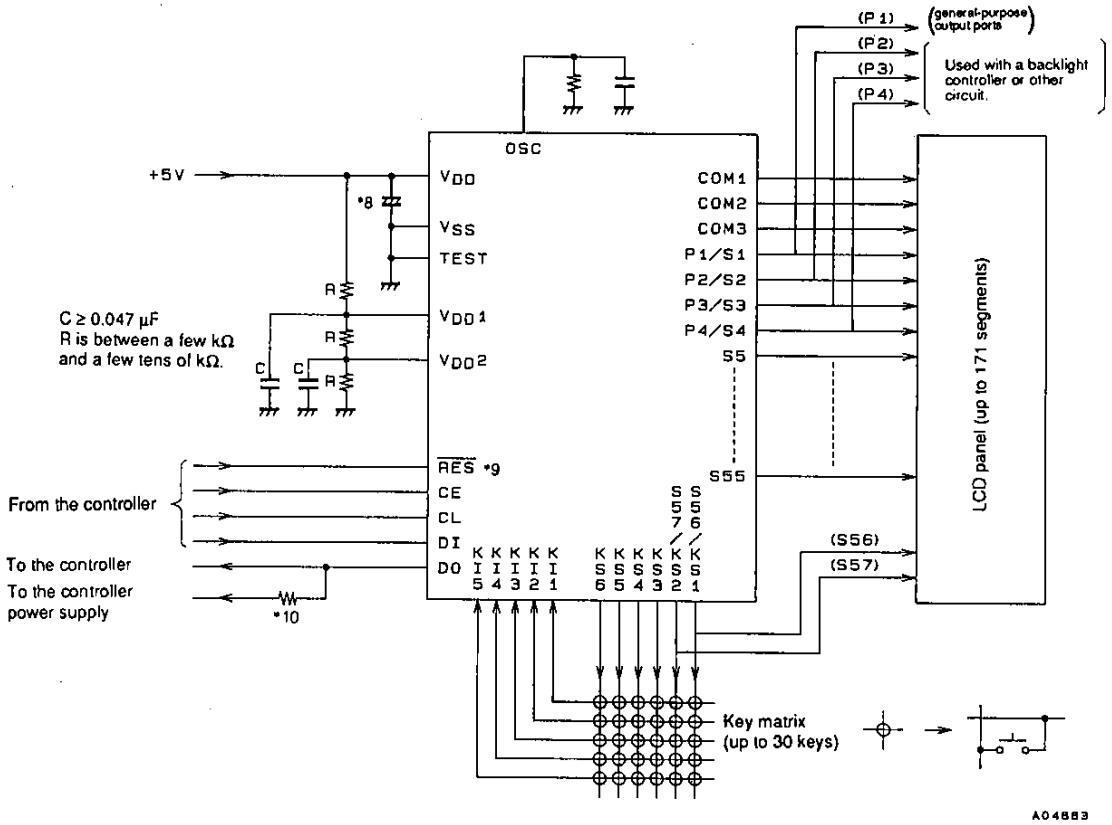
Note: *8. Add a capacitor to the power supply line so that the power supply voltage V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75883E/W is reset by the VDET.

*9. If the $\overline{RES}$ pin is not used for system reset, it must be connected to V_{DD}.

*10. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Application Circuit Example 3

1/3 bias (for use with large panels)



Note:*8.Add a capacitor to the power supply line so that the power supply voltage V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75883E/W is reset by the VDET.

*9. If the $\overline{RES}$ pin is not used for system reset, it must be connected to V_{DD}.

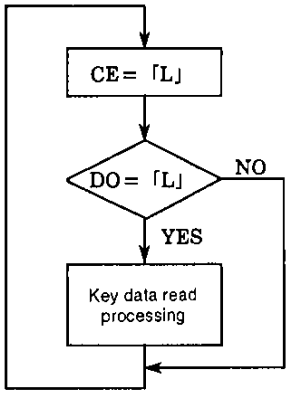
*10. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Notes on transferring display data from the controller

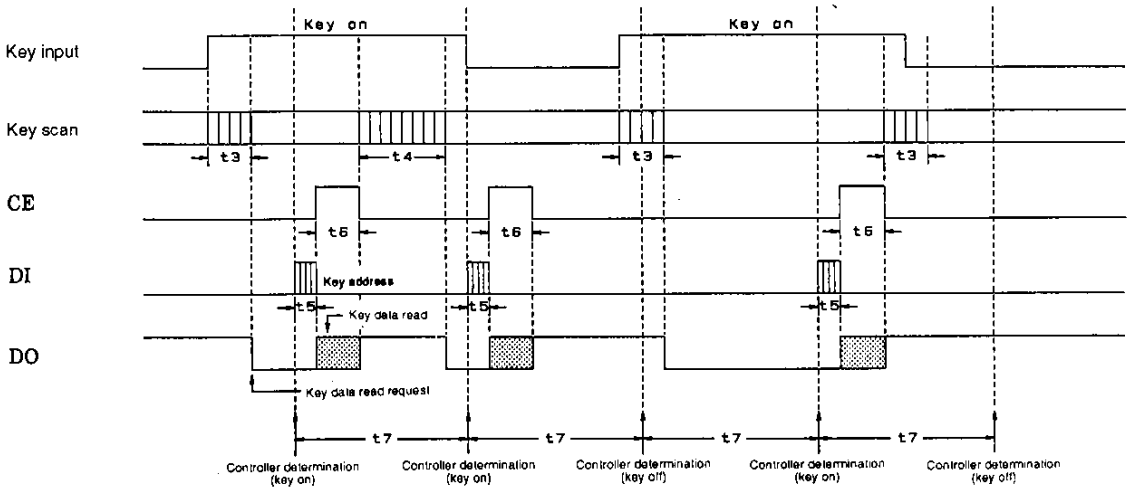
The display data (D1 to D171) is transferred to the LC75883E/W in three operations. All of the display data should be transferred within 30 ms to maintain the quality of the displayed image.

Notes on the controller key data read techniques

1. Timer based key data acquisition
   - Flowchart



   - Timing chart



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t3 .....Key scan execution time when the key data agreed for two key scans. (615·T (s))
t4 .....Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1230·T (s))
t5 .....Key address (43H) transfer time
t6 .....Key data read time

$$T = \frac{1}{f_{OSC}}$$

   - Explanation

In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the DO state when CE is low every t7 period without fail. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation.

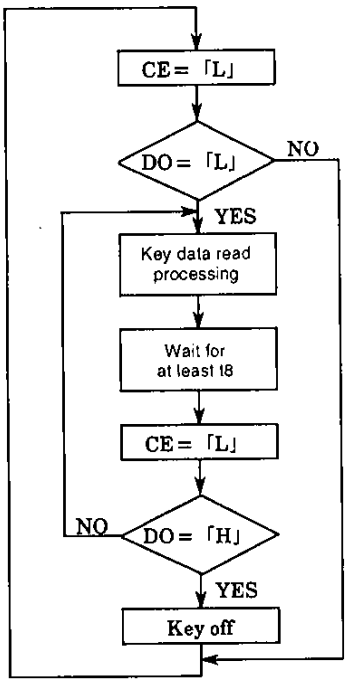
The period t7 in this technique must satisfy the following condition.

$t7 > (t5 + t6 + t4)$

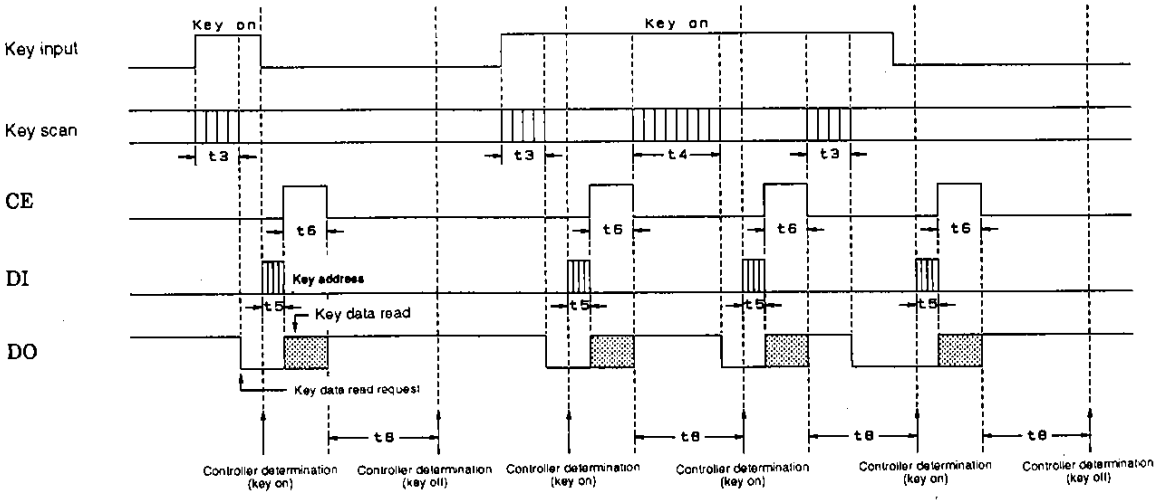
If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

2. Interrupt based key data acquisition

• Flowchart



• Timing chart



t3 .....Key scan execution time when the key data agreed for two key scans. (615·T (s))
t4 .....Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1230·T (s))
t5 .....Key address (43H) transfer time
t6 .....Key data read time

$$T = \frac{1}{f_{OSC}}$$

• Explanation

In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the DO state when CE is low. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t8 has elapsed by checking the DO state when CE is low and reading the key data. The period t8 in this technique must satisfy the following condition.

$t8 > t4$

If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.