Ordering number : ENN 6902

CMOS IC

LC75838E, 75838W

1/8 to 1/10 Duty General-Purpose LCD Display Drivers

Overview

The LC75838E and LC75838W are 1/8 to 1/10 duty general-purpose LCD display drivers used for character and graphics display. These products operate under the control of a microcontroller and can directly drive an LCD with up to 380 segments. They can also control up to 3 general-purpose output ports.

Features

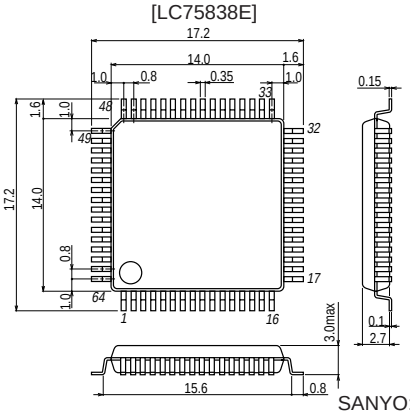
- 1/8duty–1/4bias, 1/9duty–1/4bias, and 1/10duty–1/4bias drive schemes can be controlled from serial data.
  - 1/8duty–1/4bias: up to 320 segments
  - 1/9duty–1/4bias: up to 351 segments
  - 1/10duty–1/4bias: up to 380 segments
- Serial data input supports CCB format communication with the system controller.
- Serial data control of the power-saving mode based backup function and all the segments forced off function.
- Direct display of display data without the use of a decoder provides high generality.
- Built-in display contrast adjustment circuit.
- Up to 3 general-purpose output ports are included.
- Independent LCD driver block power supply V_{LCD}.
- The $\overline{INH}$ pin is provided. This pin turns off the display and forces the general-purpose output ports to the low level.
- RC oscillator circuit

Package Dimensions

unit: mm

3159-QIP64E

[LC75838E]

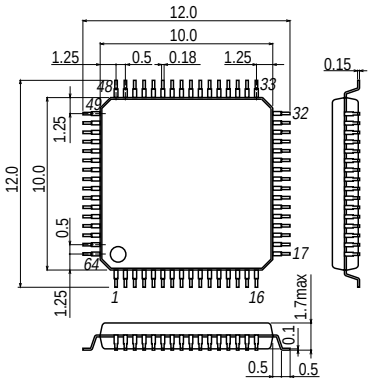


SANYO: QIP64E

unit: mm

3190-SQFP64

[LC75838W]



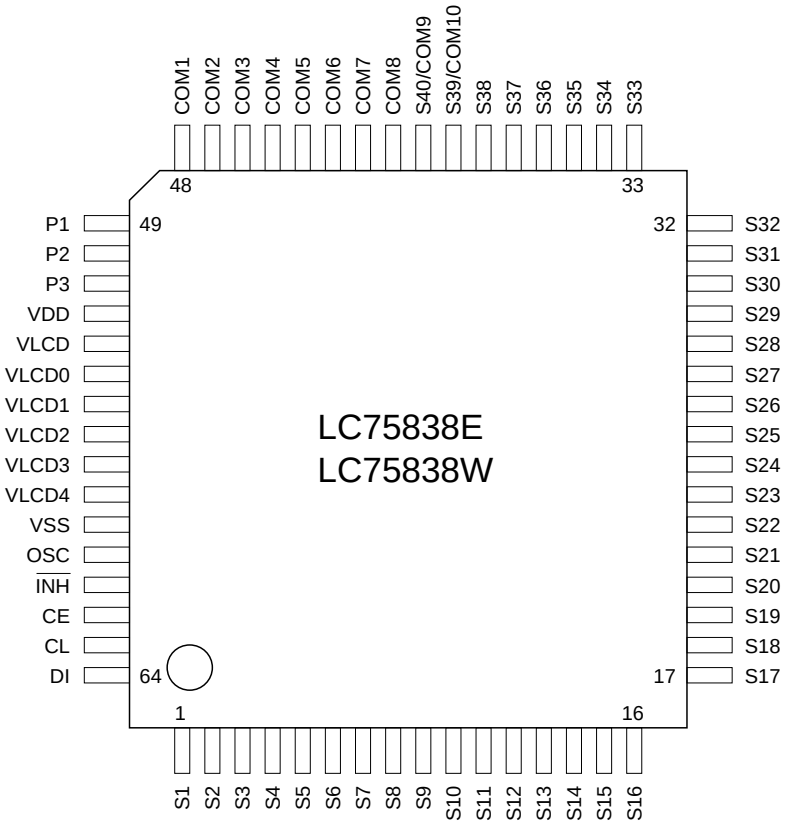
SANYO: SQFP64

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Pin Assignment



Specifications

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
	V_{LCD} max	V_{LCD}	–0.3 to +12.0	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	–0.3 to +7.0	V
	$V_{IN}2$	OSC	–0.3 to V_{DD} +0.3	
	$V_{IN}3$	$V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, $V_{LCD}4$	–0.3 to V_{LCD} +0.3	
Output voltage	$V_{OUT}1$	OSC, P1 to P3	–0.3 to V_{DD} +0.3	V
	$V_{OUT}2$	$V_{LCD}0$, S1 to S40, COM1 to COM10	–0.3 to V_{LCD} +0.3	
Output current	$I_{OUT}1$	S1 to S40	300	µA
	$I_{OUT}2$	COM1 to COM10	3	mA
	$I_{OUT}3$	P1 to P3	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS}=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		6.0	V
	V_{LCD}	V_{LCD}, When the display contrast adjustment circuit is used	7.0		11.0	
		V_{LCD}, When the display contrast adjustment circuit is not used	4.5		11.0	
Output voltage	$V_{LCD}0$	$V_{LCD}0$	$V_{LCD}4$ + 4.5		V_{LCD}	V
Input voltage	$V_{LCD}1$	$V_{LCD}1$		3/4 ($V_{LCD}0$–$V_{LCD}4$)	$V_{LCD}0$	V
	$V_{LCD}2$	$V_{LCD}2$		2/4 ($V_{LCD}0$–$V_{LCD}4$)	$V_{LCD}0$	
	$V_{LCD}3$	$V_{LCD}3$		1/4 ($V_{LCD}0$–$V_{LCD}4$)	$V_{LCD}0$	
	$V_{LCD}4$	$V_{LCD}4$	0		1.5	
Input high level voltage	V_{IH}	CE, CL, DI, $\overline{INH}$	0.8 V_{DD}		6.0	V
Input low level voltage	V_{IL}	CE, CL, DI, $\overline{INH}$	0		0.2 V_{DD}	V
Recommended external resistance	R_{OSC}	OSC		43		kΩ
Recommended external capacitance	C_{OSC}	OSC		680		pF
Guaranteed oscillation range	f_{OSC}	OSC	25	50	100	kHz
Data setup time	t_{ds}	CL, DI :Figure 2	160			ns
Data hold time	t_{dh}	CL, DI :Figure 2	160			ns
CE wait time	t_{cp}	CE, CL :Figure 2	160			ns
CE setup time	t_{cs}	CE, CL :Figure 2	160			ns
CE hold time	t_{ch}	CE, CL :Figure 2	160			ns
High level clock pulse width	tø$_H$	CL :Figure 2	160			ns
Low level clock pulse width	tø$_L$	CL :Figure 2	160			ns
$\overline{INH}$ switching time	t_c	$\overline{INH}$, CE :Figures 3, 4, and 5	10			µs

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$		0.1 V_{DD}		V
Input high level current	I_{IH}	CE, CL, DI, $\overline{INH}$: V_I = 6.0 V			5.0	µA
Input low level current	I_{IL}	CE, CL, DI, $\overline{INH}$: V_I = 0 V	–5.0			µA
Output high level voltage	$V_{OH}1$	S1 to S40: I_O = –20 µA	$V_{LCD}0$ – 0.6			V
	$V_{OH}2$	COM1 to COM10: I_O = –100 µA	$V_{LCD}0$ – 0.6			
	$V_{OH}3$	P1 to P3: I_O = –1 mA	V_{DD} – 1.0			
Output low level voltage	$V_{OL}1$	S1 to S40: I_O = 20 µA			$V_{LCD}4$ + 0.6	V
	$V_{OL}2$	COM1 to COM10: I_O = 100 µA			$V_{LCD}4$ + 0.6	
	$V_{OL}3$	P1 to P3: I_O = 1 mA			1.0	
Output middle level voltage *1	$V_{MID}1$	S1 to S40: I_O = ±20 µA	2/4 ($V_{LCD}0$ – $V_{LCD}4$) –0.6		2/4 ($V_{LCD}0$ – $V_{LCD}4$) +0.6	V
	$V_{MID}2$	COM1 to COM10: I_O = ±100 µA	3/4 ($V_{LCD}0$ – $V_{LCD}4$) –0.6		3/4 ($V_{LCD}0$ – $V_{LCD}4$) +0.6	
	$V_{MID}3$	COM1 to COM10: I_O = ±100 µA	1/4 ($V_{LCD}0$ – $V_{LCD}4$) –0.6		1/4 ($V_{LCD}0$ – $V_{LCD}4$) +0.6	
Oscillator frequency	fosc	OSC: R_{OSC} = 43 kΩ, C_{OSC} = 680 pF	40	50	60	kHz
Current drain	$I_{DD}1$	V_{DD} : Power saving mode			5	µA
	$I_{DD}2$	V_{DD}: V_{DD} = 6.0 V, outputs open, fosc = 50 kHz		200	400	
	$I_{LCD}1$	V_{LCD} : Power saving mode			5	
	$I_{LCD}2$	V_{LCD} : V_{LCD} = 11.0 V Outputs open fosc = 50 kHz When the display contrast adjustment circuit is used.		500	1000	
	$I_{LCD}3$	V_{LCD} : V_{LCD} = 11.0 V Outputs open fosc = 50 kHz When the display contrast adjustment circuit is not used.		250	500	

Note: *1 Excluding the bias voltage generation divider resistor built into $V_{LCD}0$, $V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, and $V_{LCD}4$. (See Figure 1.)

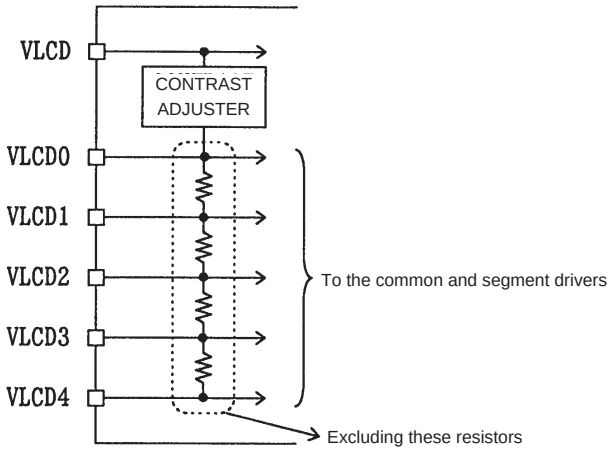
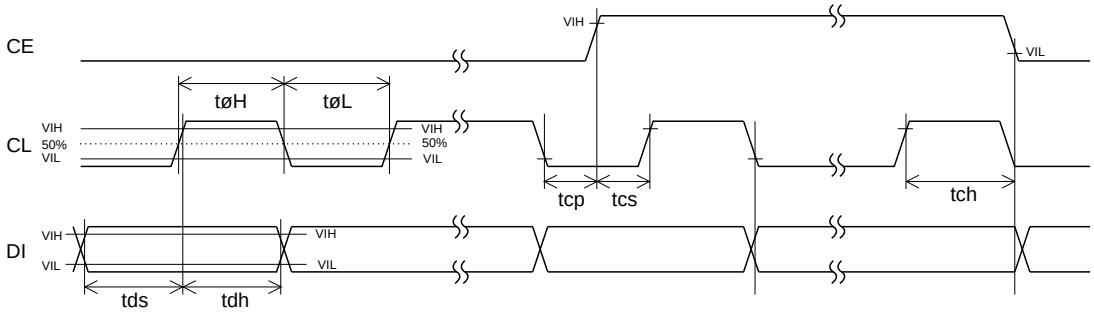


Figure 1

- When CL is stopped at the low level



- When CL is stopped at the high level

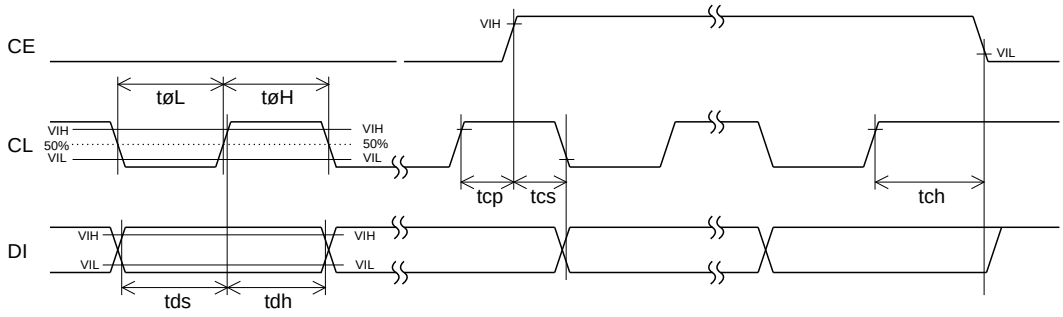
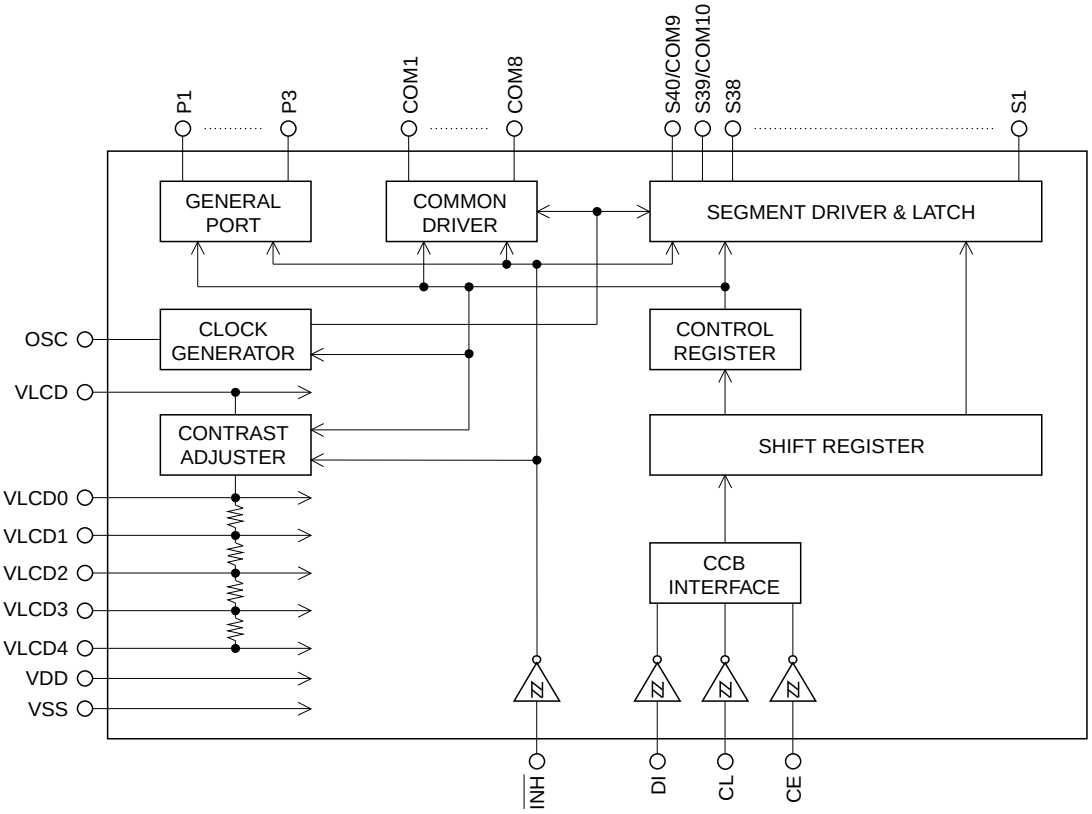


Figure 2

Block Diagram



Pin Functions

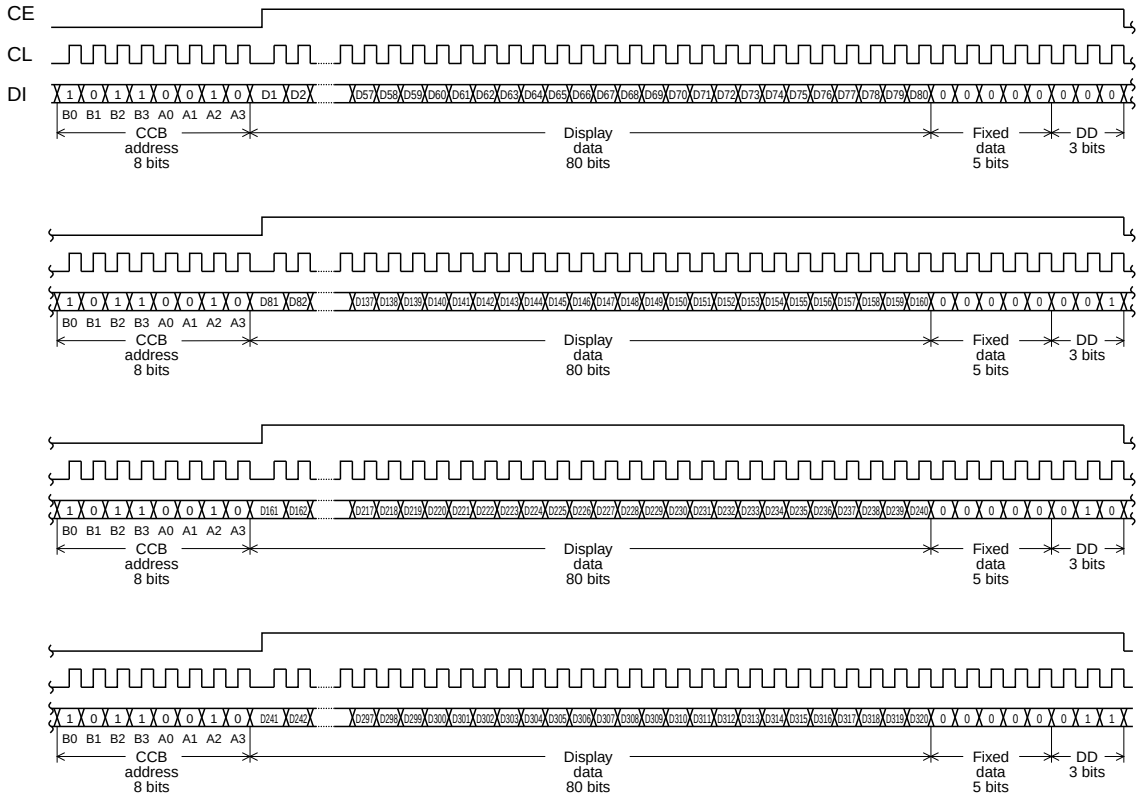
Pin	Pin No.	Function	Active	I/O	Handling when unused
S1 to S38 S39/COM10 S40/COM9	1 to 38 39 40	Segment driver outputs. The S39/COM10 and S40/COM9 pins can be used as common driver outputs under the control data DT1, DT2.	—	○	Open
COM1 to COM8	48 to 41	Common driver outputs.	—	○	Open
P1 to P3	49 to 51	General-purpose output ports.	—	○	Open
OSC	60	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor at this pin.	—	I/O	V_{DD}
CE	62	Serial data transfer inputs. These pins are connected to the microcontroller. CE :Chip enable CL :Synchronization clock DI :Transfer data	H	I	GND
CL	63		↑	I	
DI	64		—	I	
$\overline{INH}$	61	Input that turns the display off and forces the general-purpose output ports low. • When $\overline{INH}$ is low (V_{SS}) • Display off S1 to S38 = "L" ($V_{LCD}4$). S39/COM10, S40/COM9 = "L" ($V_{LCD}4$) COM1 to COM8 = "L" ($V_{LCD}4$). • General-purpose output ports P1 to P3 = low (V_{SS}) • When $\overline{INH}$ is high (V_{DD}) • Display on • The states of the general-purpose output ports can be set by the PC1 to PC3 control data. However, serial data can be transferred when the $\overline{INH}$ pin is low.	L	I	GND
$V_{LCD}0$	54	LCD drive 4/4 bias voltage (high level) supply pin. The level on this pin can be changed by the display contrast adjustment circuit. However, ($V_{LCD}0 - V_{LCD}4$) must be greater than or equal to 4.5 V. Also,external power must not be applied to this pin since the pin circuit includes the display contrast adjustment circuit.	—	O	Open
$V_{LCD}1$	55	LCD drive 3/4 bias voltage (middle level) supply pin. This pin can be used to supply the 3/4 ($V_{LCD}0 - V_{LCD}4$) voltage level externally.	—	I	Open
$V_{LCD}2$	56	LCD drive 2/4 bias voltage (middle level) supply pin. This pin can be used to supply the 2/4 ($V_{LCD}0 - V_{LCD}4$) voltage level externally.	—	I	Open
$V_{LCD}3$	57	LCD drive 1/4 bias voltage (middle level) supply pin. This pin can be used to supply the 1/4 ($V_{LCD}0 - V_{LCD}4$) voltage level externally.	—	I	Open
$V_{LCD}4$	58	LCD drive 0/4 bias voltage (low level) supply pin. Fine adjustment of the display contrast can be implemented by connecting an external variable resistor to this pin. However, ($V_{LCD}0 - V_{LCD}4$) must be greater than or equal to 4.5 V, and $V_{LCD}4$ must be in the range 0 V to 1.5 V, inclusive.	—	I	GND
V_{DD}	52	Logic block power supply connection. Provide a voltage of between 2.7 and 6.0V.	—	—	—
V_{LCD}	53	LCD driver block power supply connection. Provide a voltage of between 7.0 and 11.0 V when the display contrast adjustment circuit is used and provide a voltage of between 4.5 and 11.0 V when the circuit is not used.	—	—	—
V_{SS}	59	Power supply connection. Connect to ground.	—	—	—

Serial Data Transfer Format

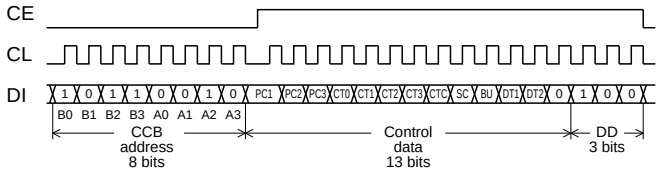
1. 1/8 duty

① When CL is stopped at the low level

• When the display data is transferred.



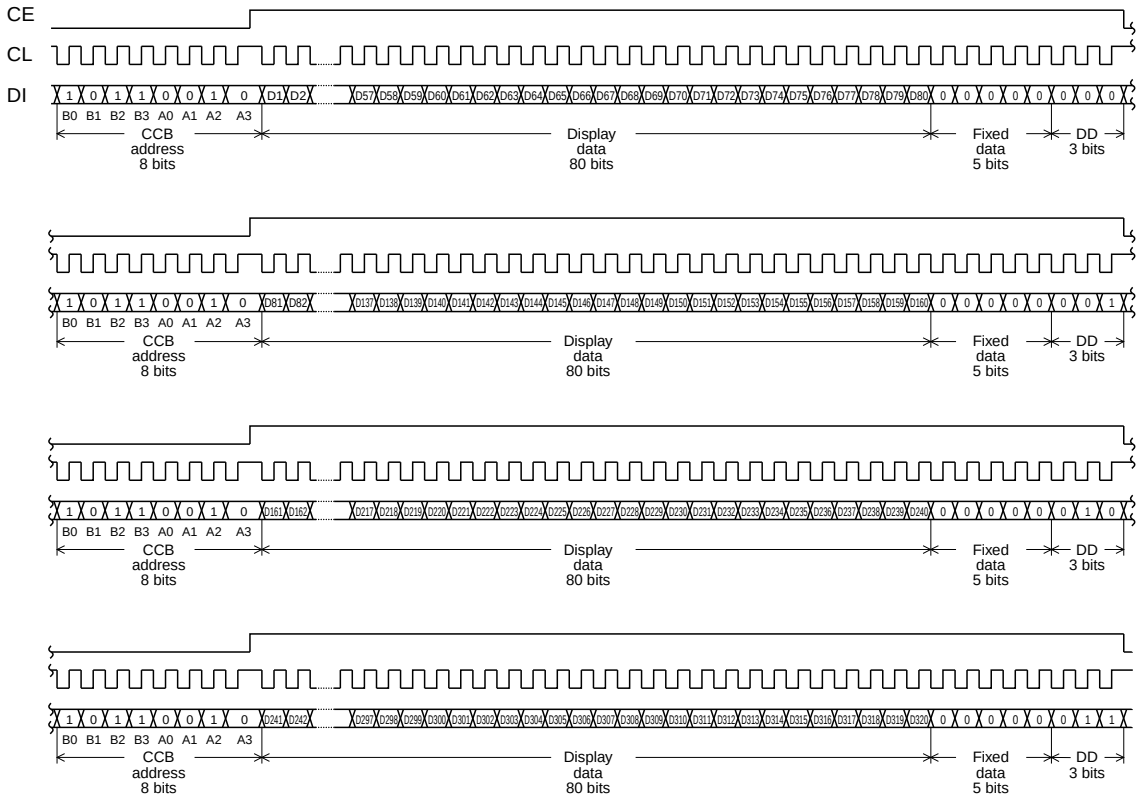
• When the control data is transferred.



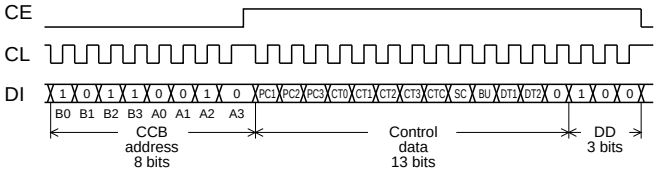
Note: B0 to B3, A0 to A3 ····· CCB address
DD····· Direction data

② When CL is stopped at the high level

• When the display data is transferred.



• When the control data is transferred.



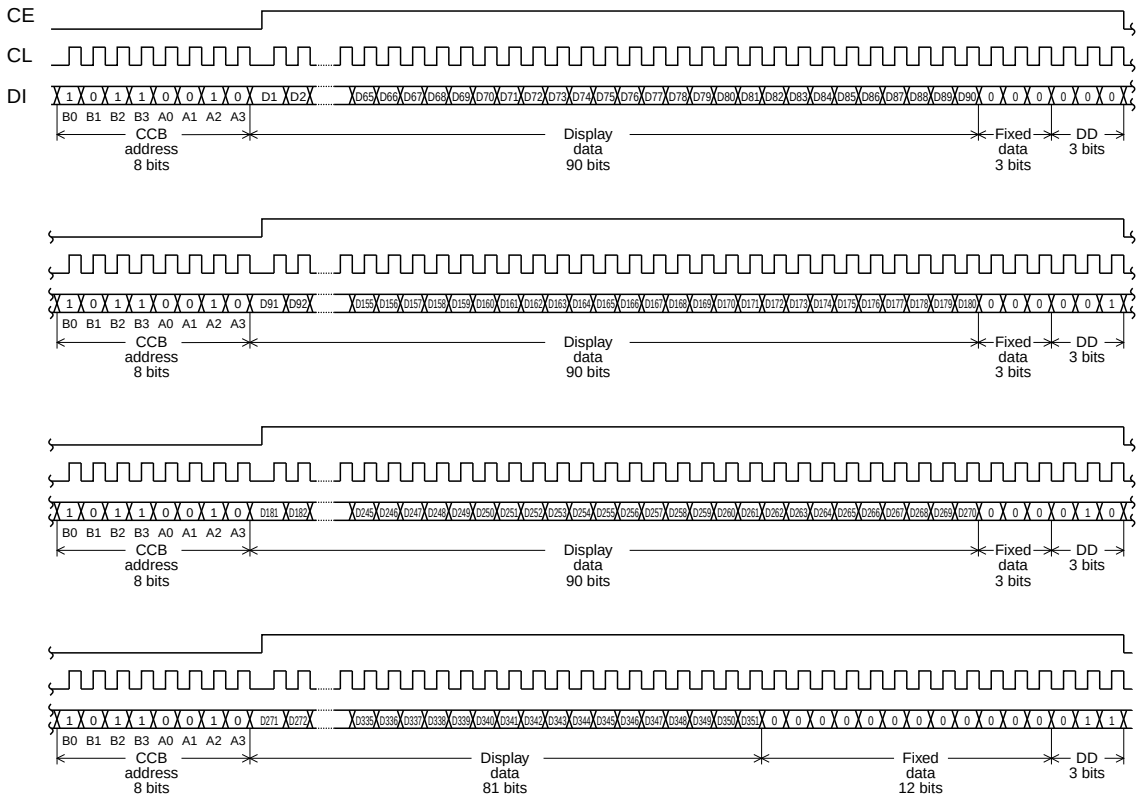
Note: B0 to B3, A0 to A3 ····· CCB address
DD····· Direction data

• CCB address: 4DH
• D1 to D320: ..... Display data
• PC1 to PC3: ..... General-purpose output port state setting data
• CT0 to CT3, CTC: Display contrast setting data
• SC: ..... Segment on/off control data
• BU: ..... Normal mode/power saving mode control data
• DT1, DT2:..... Display technique setting data

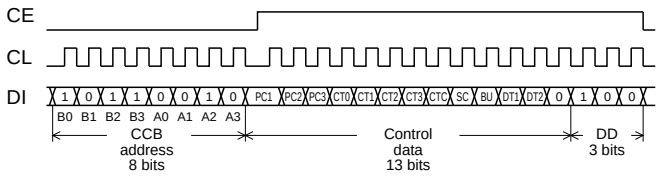
2. 1/9 duty

① When CL is stopped at the low level

• When the display data is transferred.



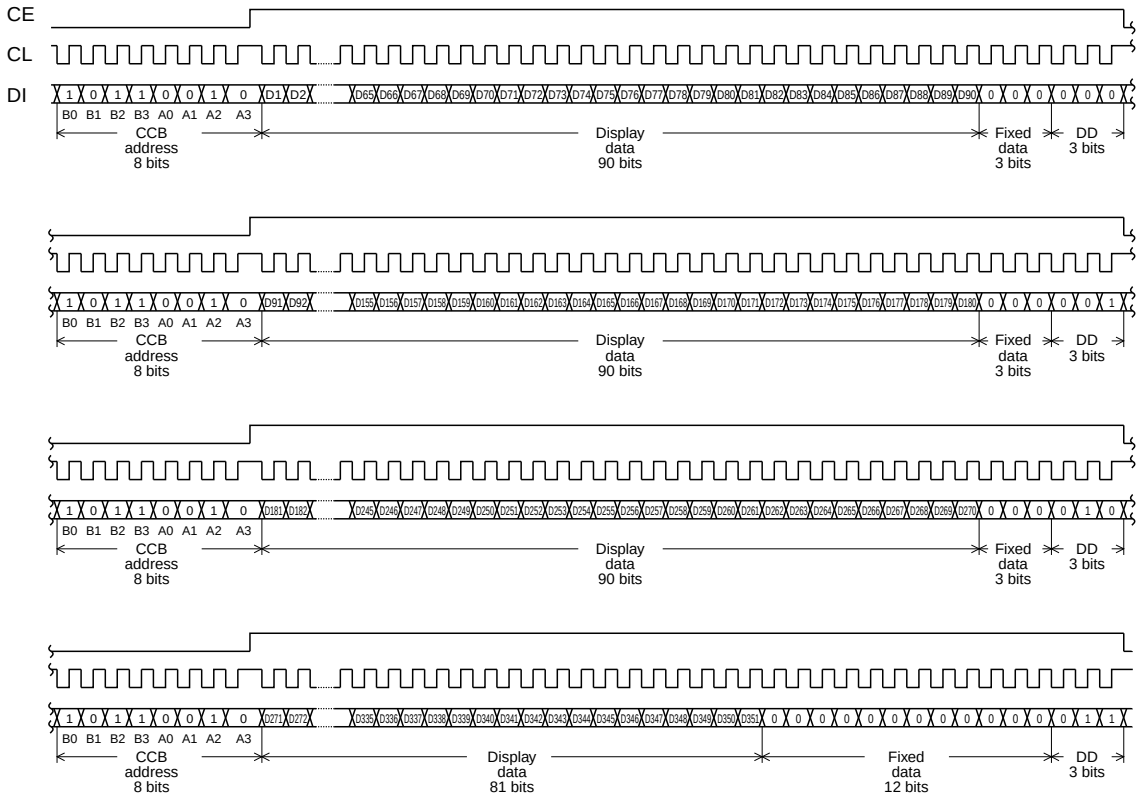
• When the control data is transferred.



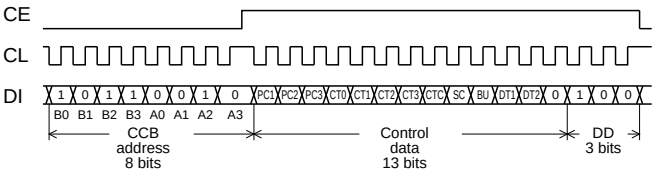
Note: B0 to B3, A0 to A3 ····· CCB address
DD····· Direction data

② When CL is stopped at the high level

• When the display data is transferred.



• When the control data is transferred.



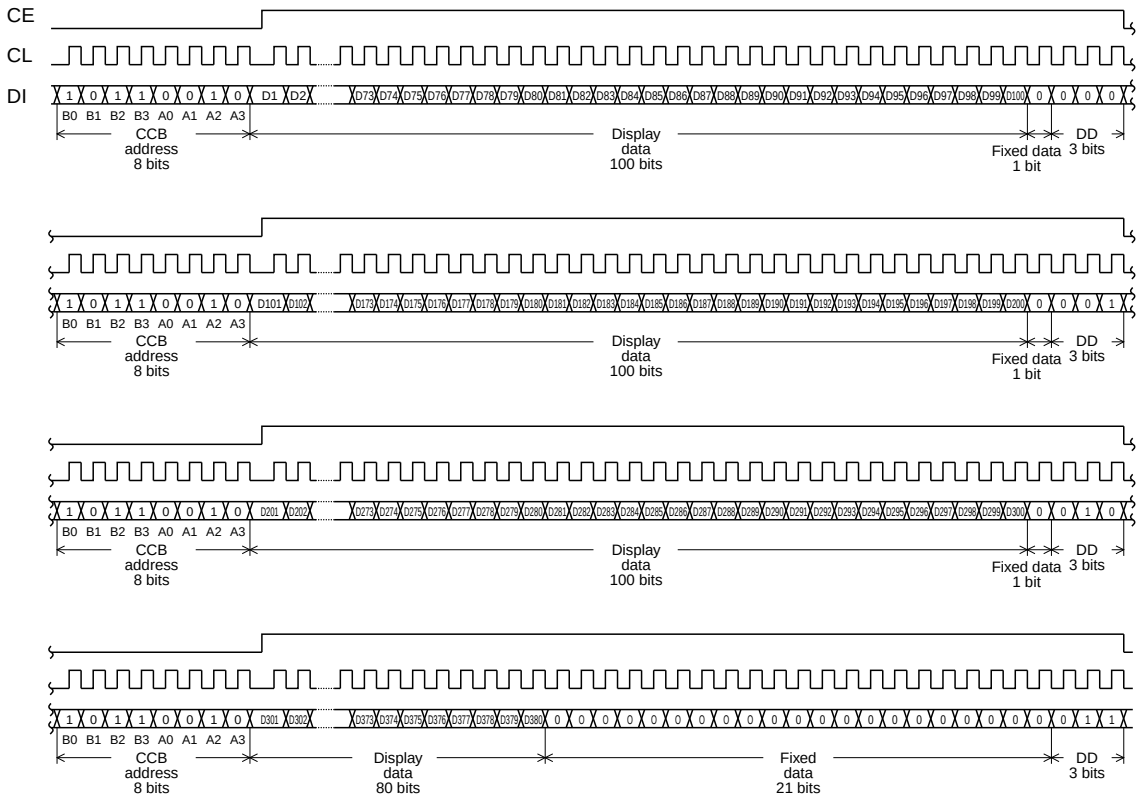
Note: B0 to B3, A0 to A3 ····· CCB address
DD····· Direction data

• CCB address: 4DH
• D1 to D351: ..... Display data
• PC1 to PC3: ..... General-purpose output port state setting data
• CT0 to CT3, CTC: Display contrast setting data
• SC: ..... Segment on/off control data
• BU: ..... Normal mode/power saving mode control data
• DT1, DT2: ..... Display technique setting data

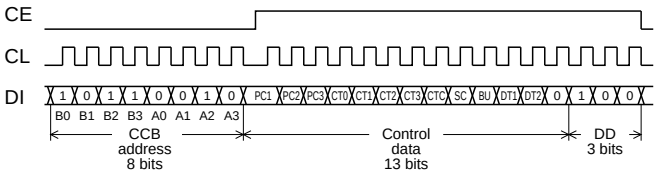
3. 1/10 duty

① When CL is stopped at the low level

• When the display data is transferred.



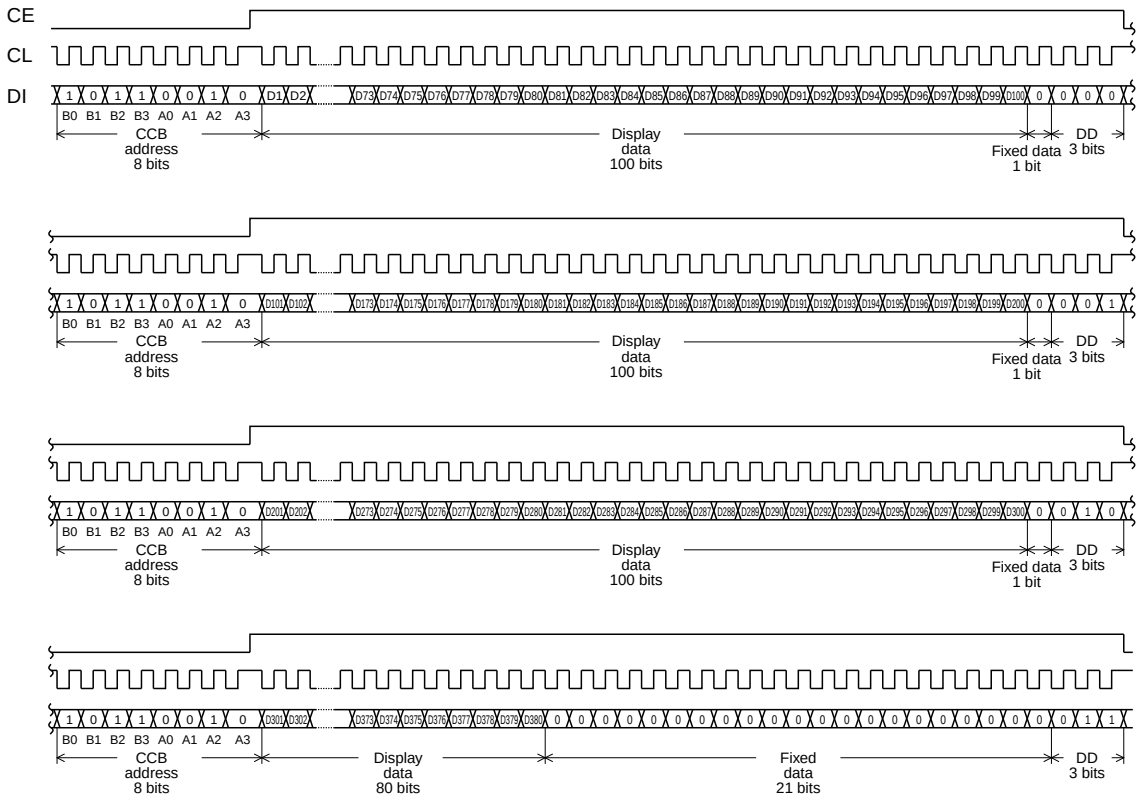
• When the control data is transferred.



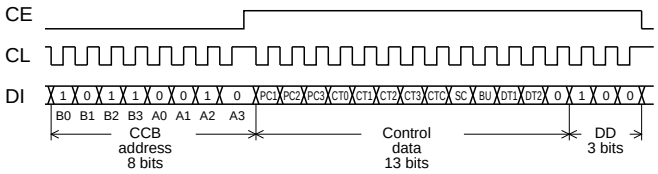
Note: B0 to B3, A0 to A3 ····· CCB address
DD ····· Direction data

② When CL is stopped at the high level

• When the display data is transferred.



• When the control data is transferred.



Note: B0 to B3, A0 to A3 ····· CCB address
DD····· Direction data

• CCB address: 4DH
• D1 to D380: ..... Display data
• PC1 to PC3: ..... General-purpose output port state setting data
• CT0 to CT3, CTC: Display contrast setting data
• SC: ..... Segment on/off control data
• BU: ..... Normal mode/power saving mode control data
• DT1, DT2: ..... Display technique setting data

Control Data Functions

1. PC1 to PC3: General-purpose output port state setting data
   These control data bits set the states of the general-purpose output ports P1 to P3.

Output pin	P1	P2	P3
General-purpose output port state setting data	PC1	PC2	PC3

For example, if PC1 and PC2 are set to 1, and PC3 is set to 0, then the output pins P1 and P2 will output high levels (V_{DD}) and the output pin P3 will output low level (V_{SS}).

2. CT0 to CT3, CTC: Display contrast setting data
   These control data bits set the display contrast.
   CT0 to CT3: Display contrast setting (11 steps)

CT0	CT1	CT2	CT3	LCD drive 4/4 bias voltage supply $V_{LCD}0$ level
0	0	0	0	0.94 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 2)
1	0	0	0	0.91 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 3)
0	1	0	0	0.88 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 4)
1	1	0	0	0.85 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 5)
0	0	1	0	0.82 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 6)
1	0	1	0	0.79 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 7)
0	1	1	0	0.76 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 8)
1	1	1	0	0.73 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 9)
0	0	0	1	0.70 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 10)
1	0	0	1	0.67 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 11)
0	1	0	1	0.64 V_{LCD} = V_{LCD} – (0.03 V_{LCD} × 12)

CTC: Display contrast adjustment circuit state setting

CTC	Display contrast adjustment circuit state
0	The display contrast adjustment circuit is disabled, and the $V_{LCD}0$ pin level is forced to the V_{LCD} level.
1	The display contrast adjustment circuit operates and the display contrast is adjusted.

Note that although the display contrast can be adjusted by operating the built-in display contrast adjustment circuit, it is also possible to apply fine adjustments to the contrast by connecting an external variable resistor to the $V_{LCD}4$ pin and modifying the $V_{LCD}4$ pin voltage. However, the following conditions must be met: ($V_{LCD}0 - V_{LCD}4$) ≥ 4.5 V, and 1.5 V ≥ $V_{LCD}4$ ≥ 0 V.

3. SC: Segment on/off control data
   This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

4. BU: Normal mode/power saving mode control data
   This control data bit controls the normal mode and power saving mode.

BU	Mode
0	Normal mode
1	Power saving mode The common and segment pins go to the $V_{LCD}4$ level and the oscillator on the OSC pin is stopped. Note that the states of the general-purpose output ports P1 to P3 are set by PC1 to PC3 in the control data during power saving mode as well as normal mode.

5. DT1, DT2: Display technique setting data
   This control data bits set the display technique.

DT1	DT2	Display technique	Output pins	
			S40/COM9	S39/COM10
0	0	1/8 duty 1/4 bias drive	S40	S39
1	0	1/9 duty 1/4 bias drive	COM9	S39
0	1	1/10 duty 1/4 bias drive	COM9	COM10

Notes: Sn (n = 39, 40): Segment outputs
COMn (n = 9 or 10): Common outputs

Display Data and Output Pin Correspondence

• 1/8 duty

Output Pin	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8
S1	D1	D2	D3	D4	D5	D6	D7	D8
S2	D9	D10	D11	D12	D13	D14	D15	D16
S3	D17	D18	D19	D20	D21	D22	D23	D24
S4	D25	D26	D27	D28	D29	D30	D31	D32
S5	D33	D34	D35	D36	D37	D38	D39	D40
S6	D41	D42	D43	D44	D45	D46	D47	D48
S7	D49	D50	D51	D52	D53	D54	D55	D56
S8	D57	D58	D59	D60	D61	D62	D63	D64
S9	D65	D66	D67	D68	D69	D70	D71	D72
S10	D73	D74	D75	D76	D77	D78	D79	D80
S11	D81	D82	D83	D84	D85	D86	D87	D88
S12	D89	D90	D91	D92	D93	D94	D95	D96
S13	D97	D98	D99	D100	D101	D102	D103	D104
S14	D105	D106	D107	D108	D109	D110	D111	D112
S15	D113	D114	D115	D116	D117	D118	D119	D120
S16	D121	D122	D123	D124	D125	D126	D127	D128
S17	D129	D130	D131	D132	D133	D134	D135	D136
S18	D137	D138	D139	D140	D141	D142	D143	D144
S19	D145	D146	D147	D148	D149	D150	D151	D152
S20	D153	D154	D155	D156	D157	D158	D159	D160
S21	D161	D162	D163	D164	D165	D166	D167	D168
S22	D169	D170	D171	D172	D173	D174	D175	D176
S23	D177	D178	D179	D180	D181	D182	D183	D184
S24	D185	D186	D187	D188	D189	D190	D191	D192
S25	D193	D194	D195	D196	D197	D198	D199	D200
S26	D201	D202	D203	D204	D205	D206	D207	D208
S27	D209	D210	D211	D212	D213	D214	D215	D216
S28	D217	D218	D219	D220	D221	D222	D223	D224
S29	D225	D226	D227	D228	D229	D230	D231	D232
S30	D233	D234	D235	D236	D237	D238	D239	D240
S31	D241	D242	D243	D244	D245	D246	D247	D248
S32	D249	D250	D251	D252	D253	D254	D255	D256
S33	D257	D258	D259	D260	D261	D262	D263	D264
S34	D265	D266	D267	D268	D269	D270	D271	D272
S35	D273	D274	D275	D276	D277	D278	D279	D280
S36	D281	D282	D283	D284	D285	D286	D287	D288
S37	D289	D290	D291	D292	D293	D294	D295	D296
S38	D297	D298	D299	D300	D301	D302	D303	D304
S39/COM10	D305	D306	D307	D308	D309	D310	D311	D312
S40/COM9	D313	D314	D315	D316	D317	D318	D319	D320

Note: Applies when the S39/COM10 and S40/COM9 output pins are set to their segment output function.

For example, the table below lists the segment output states for the S11 output pin.

Display data								Output pin state (S11)
D81	D82	D83	D84	D85	D86	D87	D88	
0	0	0	0	0	0	0	0	The LCD segments for COM1 to COM8 are off
1	0	0	0	0	0	0	0	The LCD segment for COM1 is on
0	1	0	0	0	0	0	0	The LCD segment for COM2 is on
0	0	1	0	0	0	0	0	The LCD segment for COM3 is on
0	0	0	1	0	0	0	0	The LCD segment for COM4 is on
0	0	0	0	1	0	0	0	The LCD segment for COM5 is on
0	0	0	0	0	1	0	0	The LCD segment for COM6 is on
0	0	0	0	0	0	1	0	The LCD segment for COM7 is on
0	0	0	0	0	0	0	1	The LCD segment for COM8 is on
1	1	1	1	1	1	1	1	The LCD segments for COM1 to COM8 are on

• 1/9 duty

Output Pin	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8	COM9
S1	D1	D2	D3	D4	D5	D6	D7	D8	D9
S2	D10	D11	D12	D13	D14	D15	D16	D17	D18
S3	D19	D20	D21	D22	D23	D24	D25	D26	D27
S4	D28	D29	D30	D31	D32	D33	D34	D35	D36
S5	D37	D38	D39	D40	D41	D42	D43	D44	D45
S6	D46	D47	D48	D49	D50	D51	D52	D53	D54
S7	D55	D56	D57	D58	D59	D60	D61	D62	D63
S8	D64	D65	D66	D67	D68	D69	D70	D71	D72
S9	D73	D74	D75	D76	D77	D78	D79	D80	D81
S10	D82	D83	D84	D85	D86	D87	D88	D89	D90
S11	D91	D92	D93	D94	D95	D96	D97	D98	D99
S12	D100	D101	D102	D103	D104	D105	D106	D107	D108
S13	D109	D110	D111	D112	D113	D114	D115	D116	D117
S14	D118	D119	D120	D121	D122	D123	D124	D125	D126
S15	D127	D128	D129	D130	D131	D132	D133	D134	D135
S16	D136	D137	D138	D139	D140	D141	D142	D143	D144
S17	D145	D146	D147	D148	D149	D150	D151	D152	D153
S18	D154	D155	D156	D157	D158	D159	D160	D161	D162
S19	D163	D164	D165	D166	D167	D168	D169	D170	D171
S20	D172	D173	D174	D175	D176	D177	D178	D179	D180
S21	D181	D182	D183	D184	D185	D186	D187	D188	D189
S22	D190	D191	D192	D193	D194	D195	D196	D197	D198
S23	D199	D200	D201	D202	D203	D204	D205	D206	D207
S24	D208	D209	D210	D211	D212	D213	D214	D215	D216
S25	D217	D218	D219	D220	D221	D222	D223	D224	D225
S26	D226	D227	D228	D229	D230	D231	D232	D233	D234
S27	D235	D236	D237	D238	D239	D240	D241	D242	D243
S28	D244	D245	D246	D247	D248	D249	D250	D251	D252
S29	D253	D254	D255	D256	D257	D258	D259	D260	D261
S30	D262	D263	D264	D265	D266	D267	D268	D269	D270
S31	D271	D272	D273	D274	D275	D276	D277	D278	D279
S32	D280	D281	D282	D283	D284	D285	D286	D287	D288
S33	D289	D290	D291	D292	D293	D294	D295	D296	D297
S34	D298	D299	D300	D301	D302	D303	D304	D305	D306
S35	D307	D308	D309	D310	D311	D312	D313	D314	D315
S36	D316	D317	D318	D319	D320	D321	D322	D323	D324
S37	D325	D326	D327	D328	D329	D330	D331	D332	D333
S38	D334	D335	D336	D337	D338	D339	D340	D341	D342
S39/COM10	D343	D344	D345	D346	D347	D348	D349	D350	D351

Note: Applies when the S39/COM10 output pin is set to its segment output function.

For example, the table below lists the segment output states for the S11 output pin.

Display data									Output pin state (S11)
D91	D92	D93	D94	D95	D96	D97	D98	D99	
0	0	0	0	0	0	0	0	0	The LCD segments for COM1 to COM9 are off
1	0	0	0	0	0	0	0	0	The LCD segment for COM1 is on
0	1	0	0	0	0	0	0	0	The LCD segment for COM2 is on
0	0	1	0	0	0	0	0	0	The LCD segment for COM3 is on
0	0	0	1	0	0	0	0	0	The LCD segment for COM4 is on
0	0	0	0	1	0	0	0	0	The LCD segment for COM5 is on
0	0	0	0	0	1	0	0	0	The LCD segment for COM6 is on
0	0	0	0	0	0	1	0	0	The LCD segment for COM7 is on
0	0	0	0	0	0	0	1	0	The LCD segment for COM8 is on
0	0	0	0	0	0	0	0	1	The LCD segment for COM9 is on
1	1	1	1	1	1	1	1	1	The LCD segments for COM1 to COM9 are on

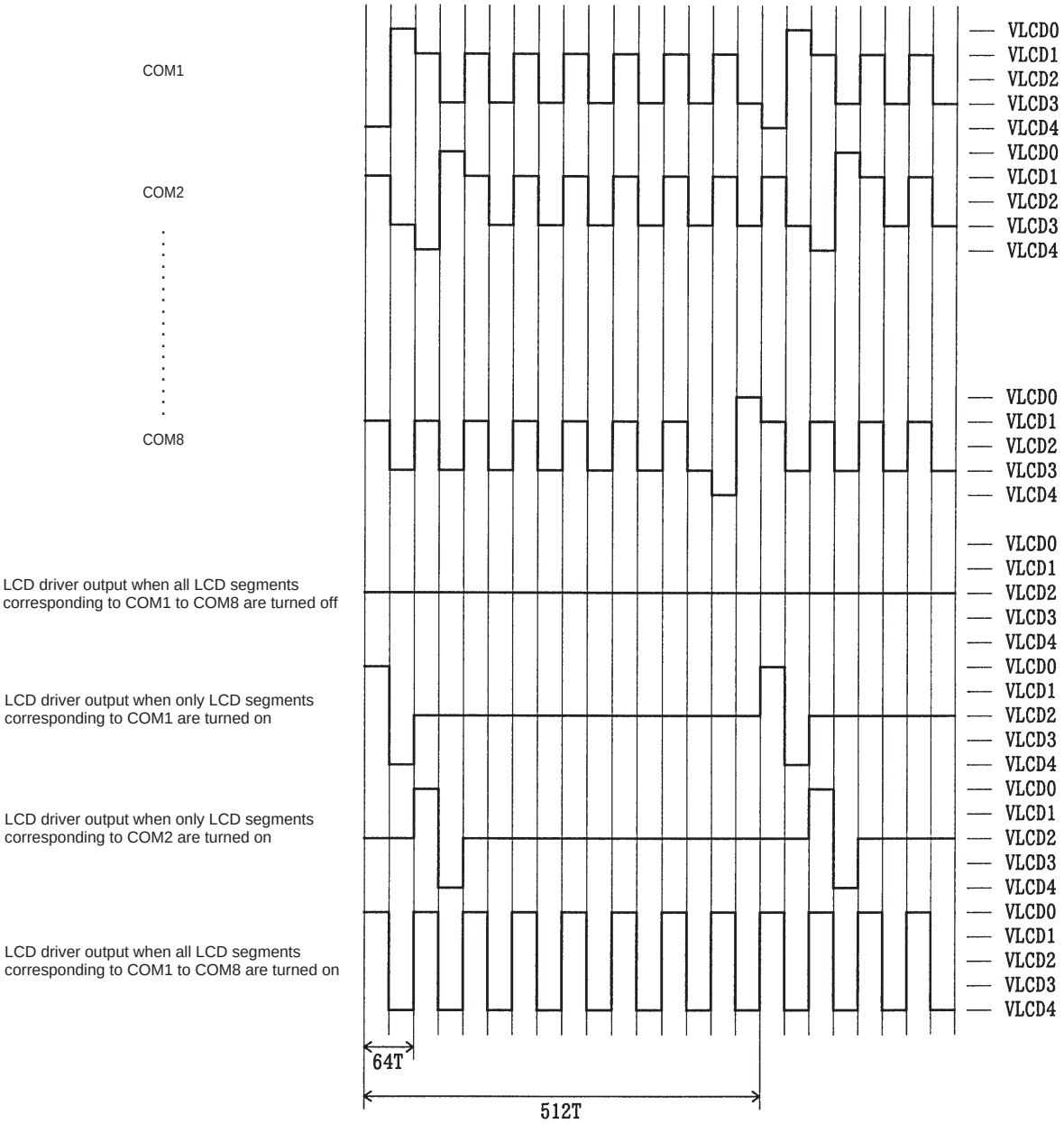
• 1/10 duty

Output Pin	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8	COM9	COM10
S1	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
S2	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20
S3	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30
S4	D31	D32	D33	D34	D35	D36	D37	D38	D39	D40
S5	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50
S6	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60
S7	D61	D62	D63	D64	D65	D66	D67	D68	D69	D70
S8	D71	D72	D73	D74	D75	D76	D77	D78	D79	D80
S9	D81	D82	D83	D84	D85	D86	D87	D88	D89	D90
S10	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100
S11	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110
S12	D111	D112	D113	D114	D115	D116	D117	D118	D119	D120
S13	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130
S14	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140
S15	D141	D142	D143	D144	D145	D146	D147	D148	D149	D150
S16	D151	D152	D153	D154	D155	D156	D157	D158	D159	D160
S17	D161	D162	D163	D164	D165	D166	D167	D168	D169	D170
S18	D171	D172	D173	D174	D175	D176	D177	D178	D179	D180
S19	D181	D182	D183	D184	D185	D186	D187	D188	D189	D190
S20	D191	D192	D193	D194	D195	D196	D197	D198	D199	D200
S21	D201	D202	D203	D204	D205	D206	D207	D208	D209	D210
S22	D211	D212	D213	D214	D215	D216	D217	D218	D219	D220
S23	D221	D222	D223	D224	D225	D226	D227	D228	D229	D230
S24	D231	D232	D233	D234	D235	D236	D237	D238	D239	D240
S25	D241	D242	D243	D244	D245	D246	D247	D248	D249	D250
S26	D251	D252	D253	D254	D255	D256	D257	D258	D259	D260
S27	D261	D262	D263	D264	D265	D266	D267	D268	D269	D270
S28	D271	D272	D273	D274	D275	D276	D277	D278	D279	D280
S29	D281	D282	D283	D284	D285	D286	D287	D288	D289	D290
S30	D291	D292	D293	D294	D295	D296	D297	D298	D299	D300
S31	D301	D302	D303	D304	D305	D306	D307	D308	D309	D310
S32	D311	D312	D313	D314	D315	D316	D317	D318	D319	D320
S33	D321	D322	D323	D324	D325	D326	D327	D328	D329	D330
S34	D331	D332	D333	D334	D335	D336	D337	D338	D339	D340
S35	D341	D342	D343	D344	D345	D346	D347	D348	D349	D350
S36	D351	D352	D353	D354	D355	D356	D357	D358	D359	D360
S37	D361	D362	D363	D364	D365	D366	D367	D368	D369	D370
S38	D371	D372	D373	D374	D375	D376	D377	D378	D379	D380

For example, the table below lists the segment output states for the S11 output pin.

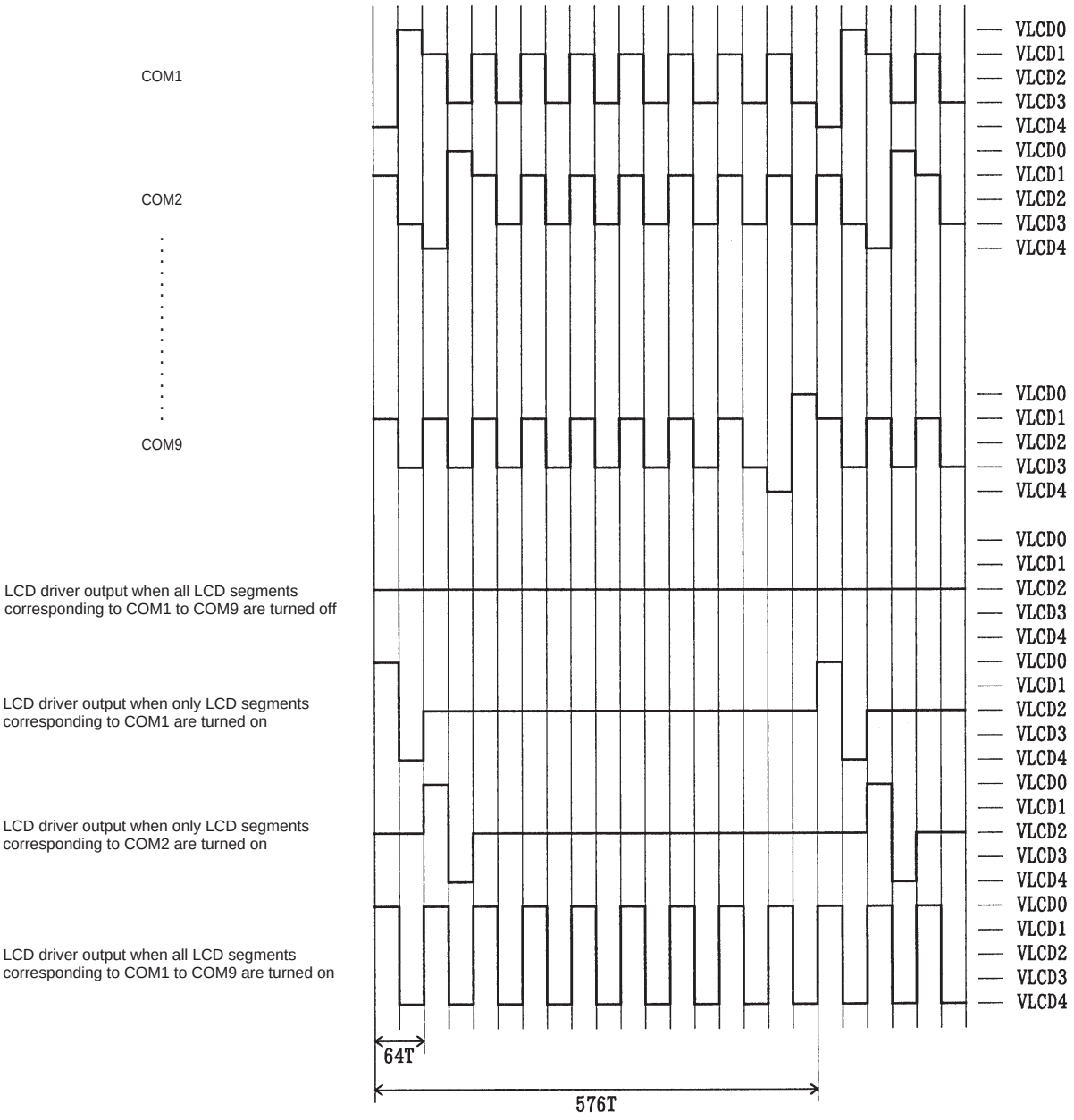
Display data										Output pin state (S11)
D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	
0	0	0	0	0	0	0	0	0	0	The LCD segments for COM1 to COM10 are off
1	0	0	0	0	0	0	0	0	0	The LCD segment for COM1 is on
0	1	0	0	0	0	0	0	0	0	The LCD segment for COM2 is on
0	0	1	0	0	0	0	0	0	0	The LCD segment for COM3 is on
0	0	0	1	0	0	0	0	0	0	The LCD segment for COM4 is on
0	0	0	0	1	0	0	0	0	0	The LCD segment for COM5 is on
0	0	0	0	0	1	0	0	0	0	The LCD segment for COM6 is on
0	0	0	0	0	0	1	0	0	0	The LCD segment for COM7 is on
0	0	0	0	0	0	0	1	0	0	The LCD segment for COM8 is on
0	0	0	0	0	0	0	0	1	0	The LCD segment for COM9 is on
0	0	0	0	0	0	0	0	0	1	The LCD segment for COM10 is on
1	1	1	1	1	1	1	1	1	1	The LCD segments for COM1 to COM10 are on

1/8 Duty, 1/4 Bias Drive Technique



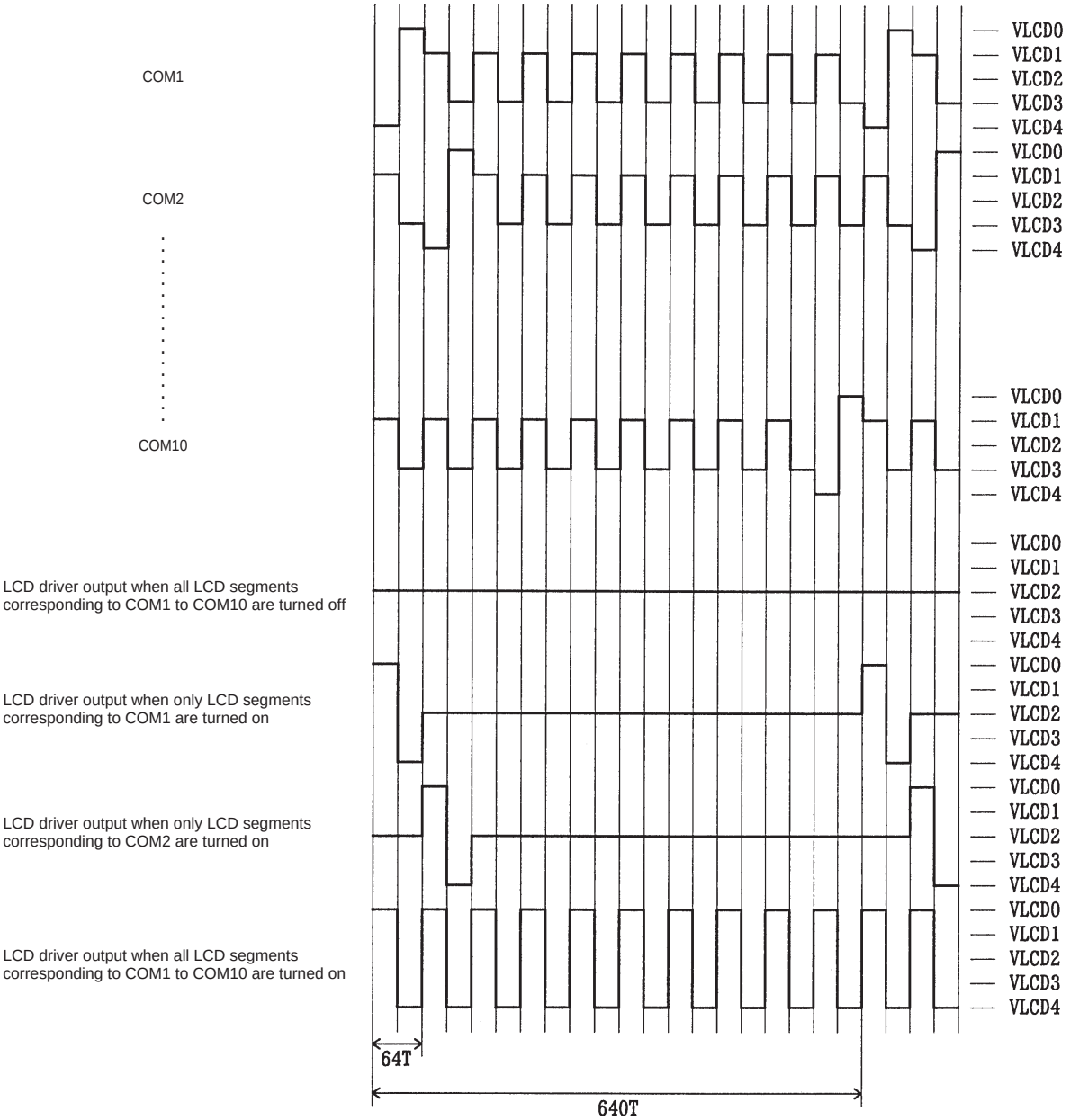
$$T = \frac{1}{fosc}$$

1/9 Duty, 1/4 Bias Drive Technique



$$T = \frac{1}{fosc}$$

1/10 Duty, 1/4 Bias Drive Technique



$$T = \frac{1}{fosc}$$

The $\overline{INH}$ Pin and Display Control

Since the IC internal data (the display data and the control data) is undefined when power is first applied, applications should set the $\overline{INH}$ pin low at the same time as power is applied to turn off the display (This sets the S1 to S38, S39/COM10, S40/COM9, and COM1 to COM8 to the $V_{LCD}4$ level and the P1 to P3 to the V_{SS} level.) and during this period send serial data from the controller. The controller should then set the $\overline{INH}$ pin high after the data transfer has completed. This procedure prevents meaningless displays at power on. (See figures 3, 4, and 5.)

Power Supply Sequence

The following sequences must be observed when power is turned on and off. (See figures 3, 4, and 5.)

- Power on :Logic block power supply(V_{DD}) on → LCD driver block power supply(V_{LCD}) on
- Power off:LCD driver block power supply(V_{LCD}) off → Logic block power supply(V_{DD}) off

However, if the logic and LCD driver blocks use a shared power supply, then the power supplies can be turned on and off at the same time.

- 1/8 duty

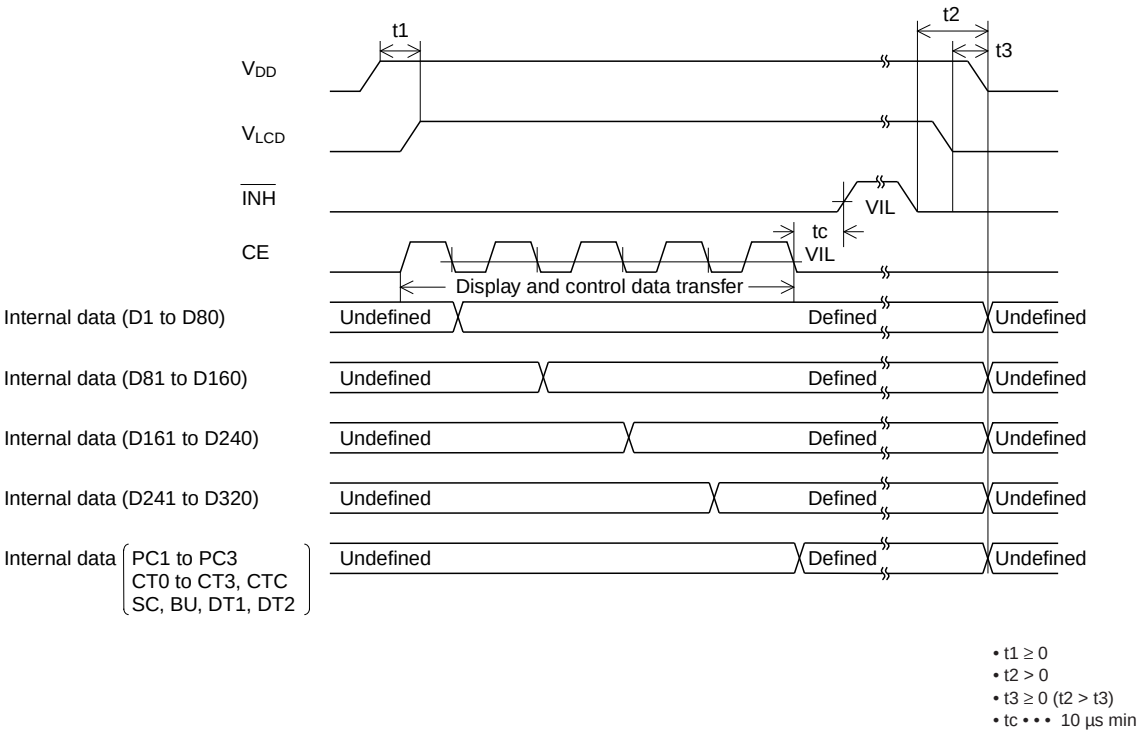


Figure 3

• 1/9 duty

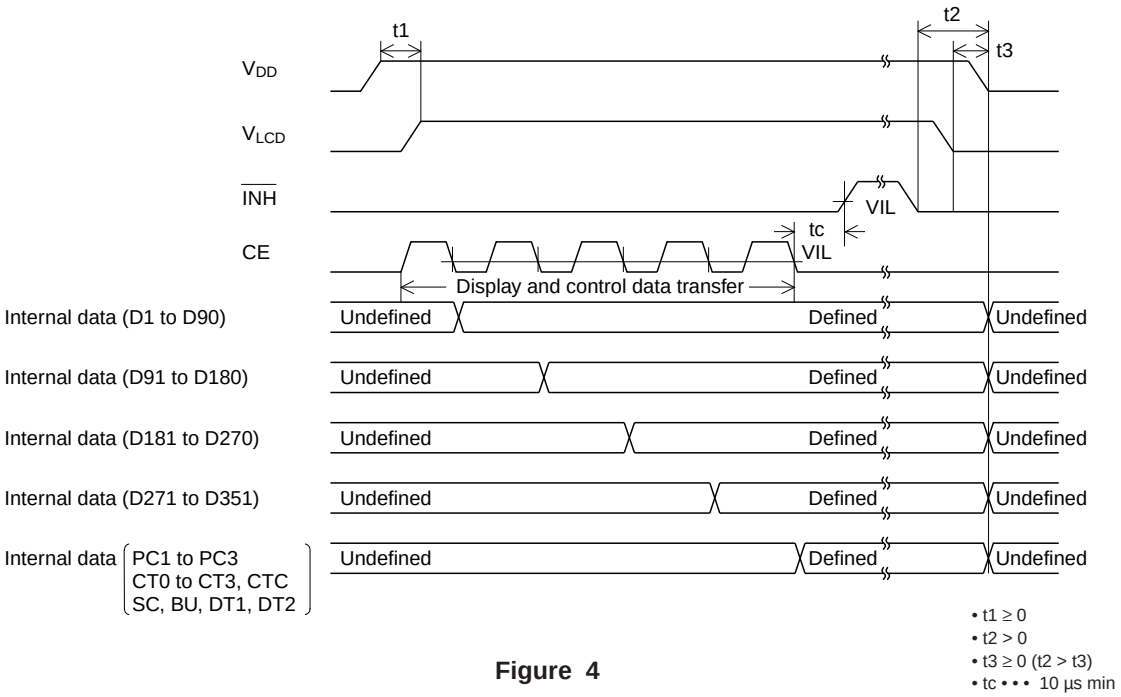


Figure 4

• 1/10 duty

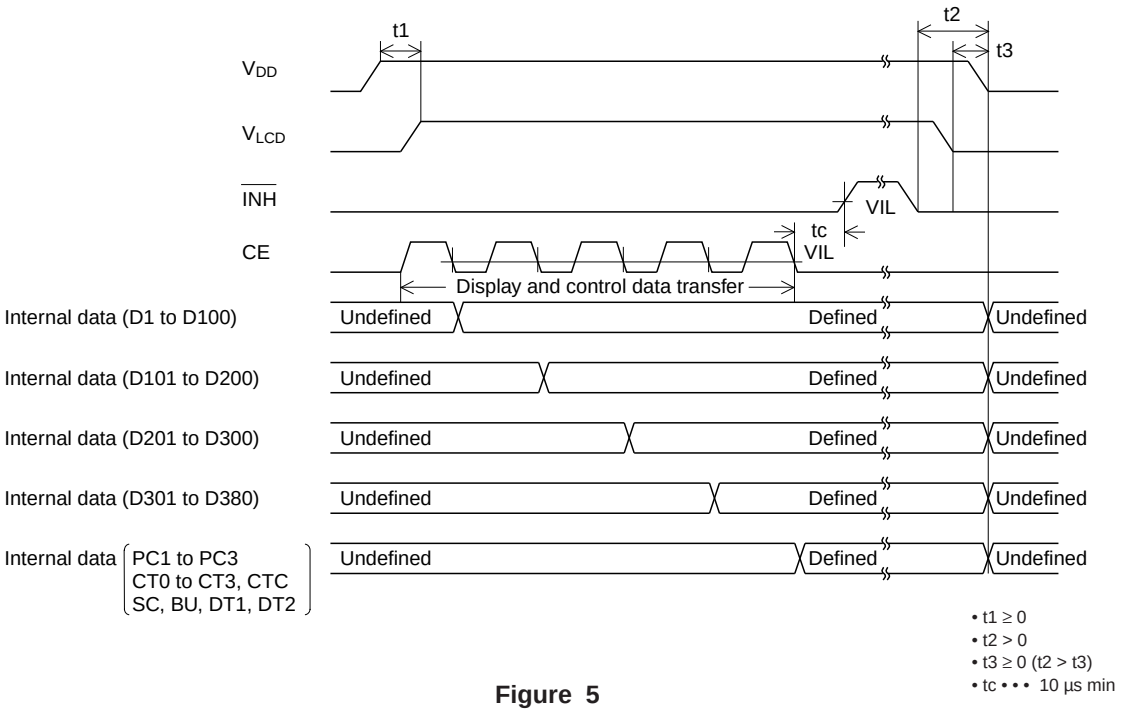


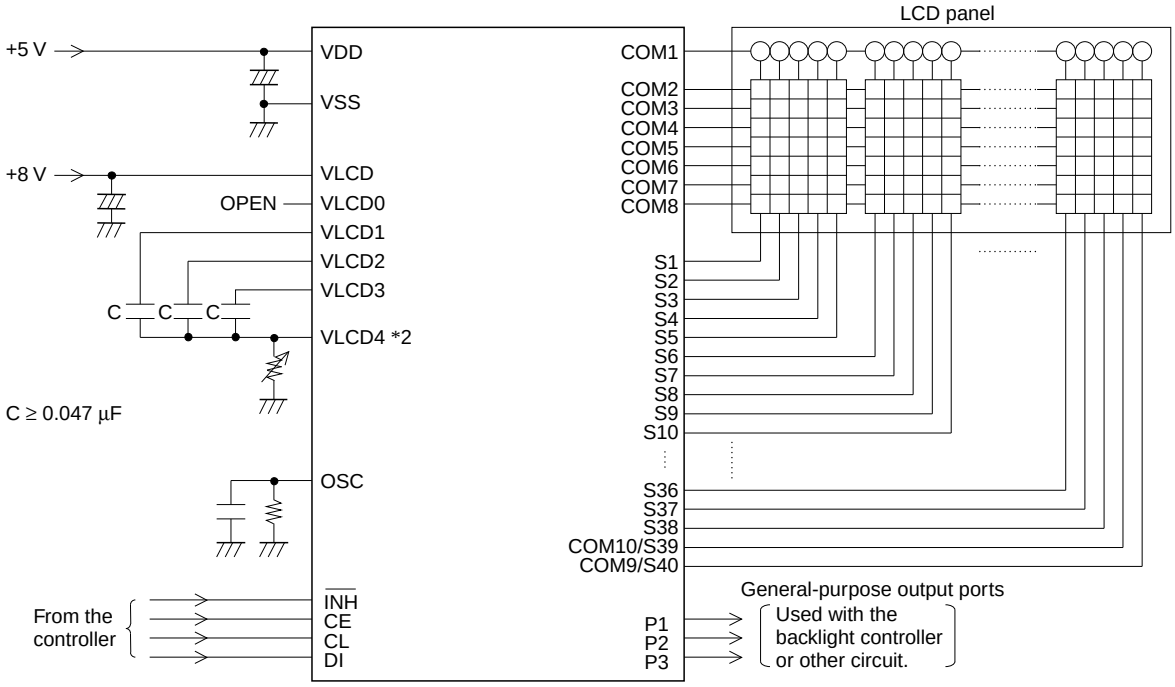
Figure 5

Notes on Transferring Display Data from the Controller

The display data is transferred to the LC75838E/W in four operations. All of the display data should be transferred within 30 ms to maintain the quality of the displayed image.

Sample Application Circuit 1

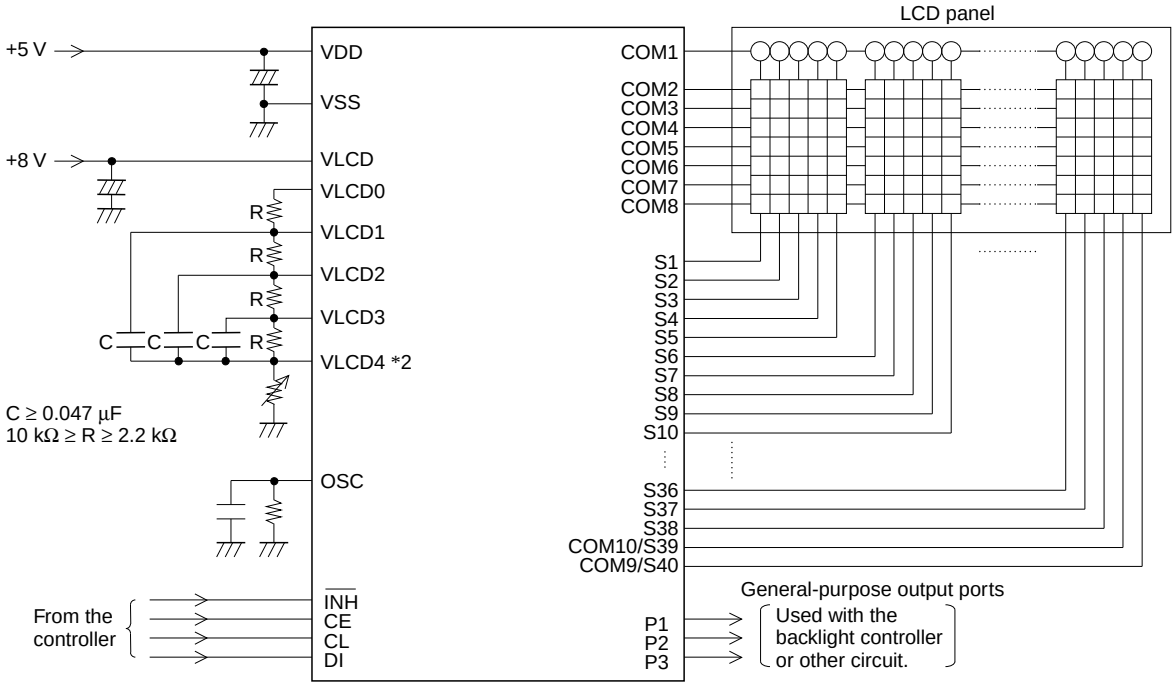
1/8 duty, 1/4 bias drive technique (for use with normal panels)



Note: *2. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

Sample Application Circuit 2

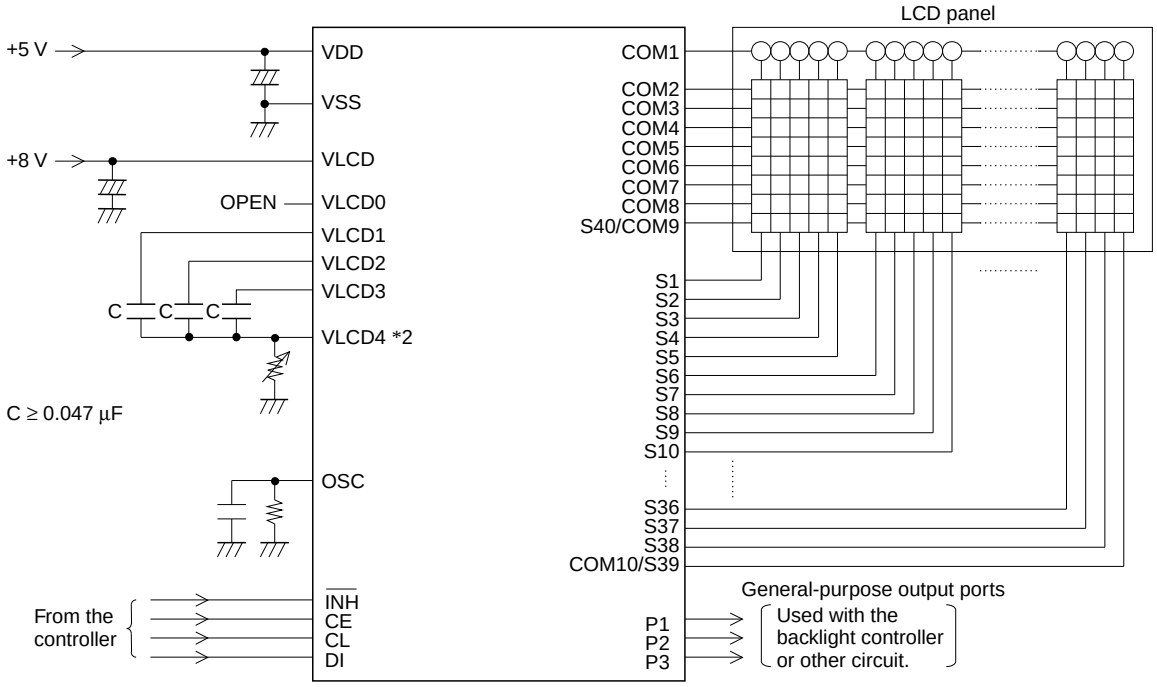
1/8 duty, 1/4 bias drive technique (for use with large panels)



Note: *2. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

Sample Application Circuit 3

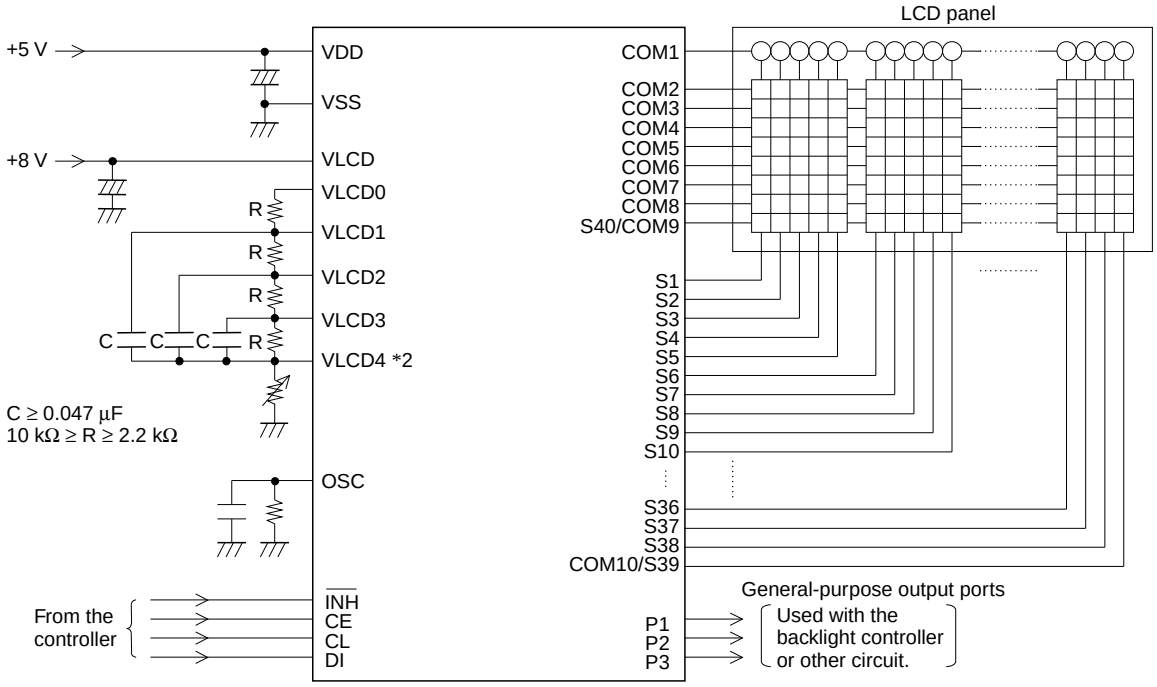
1/9 duty, 1/4 bias drive technique (for use with normal panels)



Note: *2. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

Sample Application Circuit 4

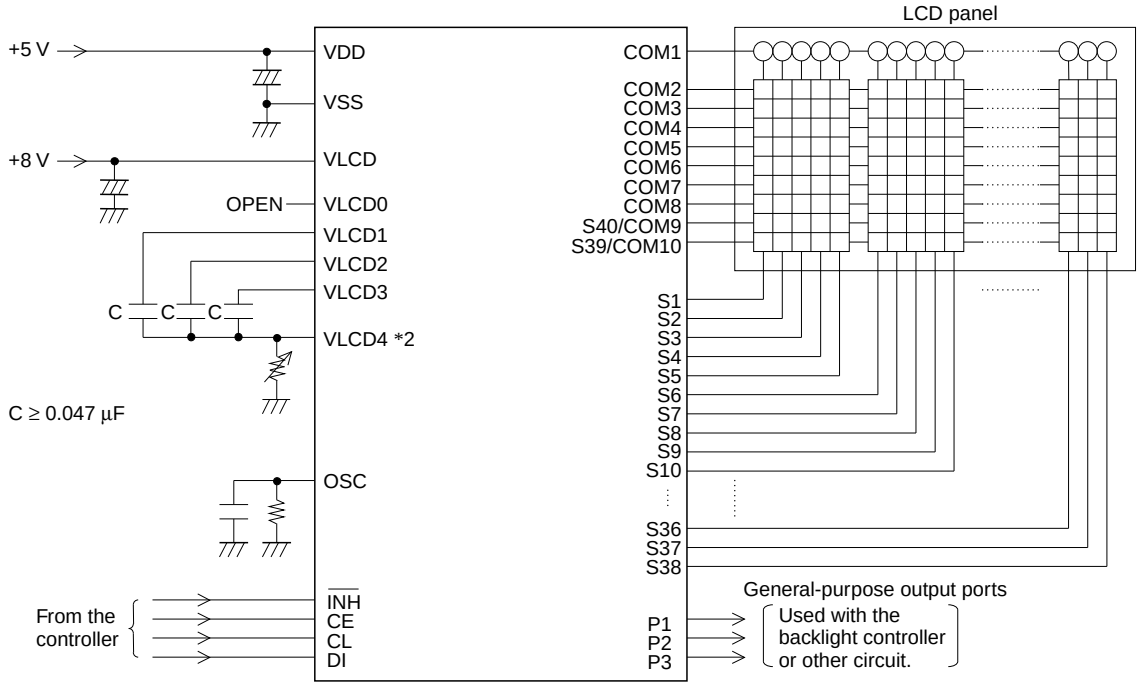
1/9 duty, 1/4 bias drive technique (for use with large panels)



Note: *2. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

Sample Application Circuit 5

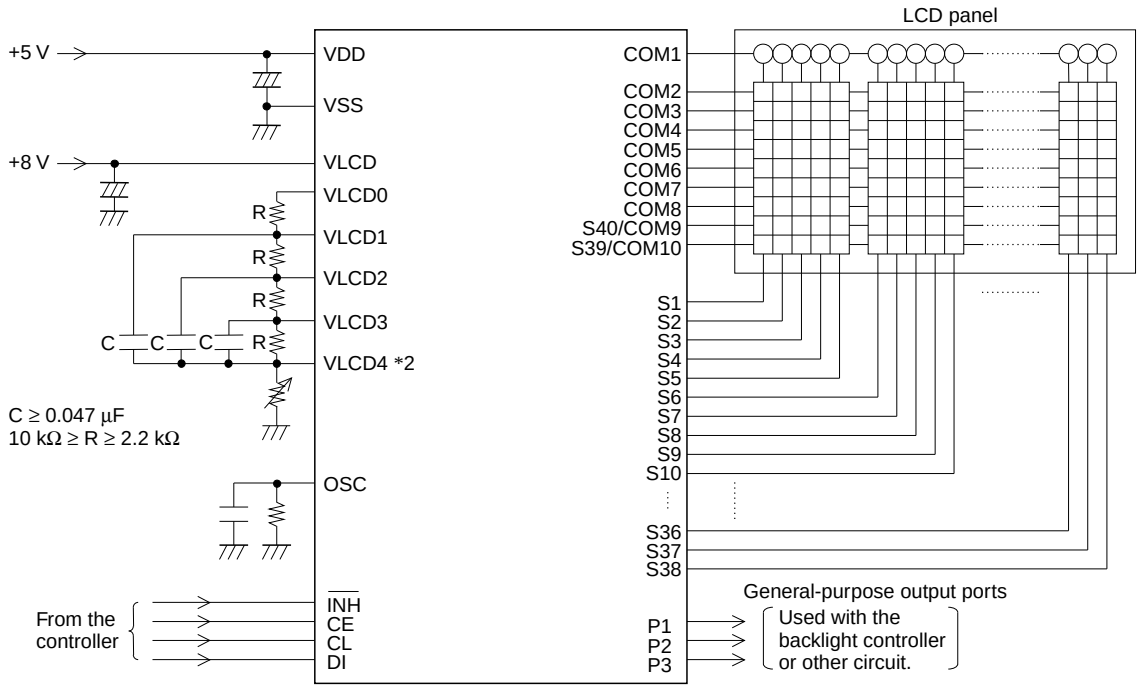
1/10 duty, 1/4 bias drive technique (for use with normal panels)



Note: *2. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

Sample Application Circuit 6

1/10 duty, 1/4 bias drive technique (for use with large panels)



Note: *2. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.