Ordering number : ENA0573

SANYO Semiconductors
DATA SHEET

LC7940KD
LC7941KDR

CMOS IC
Dot-Matrix LCD Drivers

Overview

The LC7940KD and LC7941KDR are segment driver LSIs for driving large, dot-matrix LCD displays. They read 4-bit parallel or serial input, display data from a controller into an 80-bit latch, and then generate LCD drive signals corresponding to that data. The LC7940KD and LC7941KDR feature mirror-image pin assignments, allowing them to be used together to increase component density. They are designed to be used with the LC7942KD (QIP80D) common driver to drive large LCD panels.

Features

- 80 built-in LCD display drive circuits
- 1/8 to 1/128 display duty cycle
- Serial or 4-bit parallel data input
- Chip disable for low power dissipation for large-sized panels
- Bias supply voltage can be supplied externally
- Operating supply voltage and ambient temperature
  V_{DD} (logic block): 2.7 to 5.5V/-20 to +85°C
  V_{DD}-V_{EE} (LCD block): 8 to 20V/-20 to +85°C
- CMOS process
- Package: QIP100D(LC7940KD)/QIP100DR(LC7941KDR)

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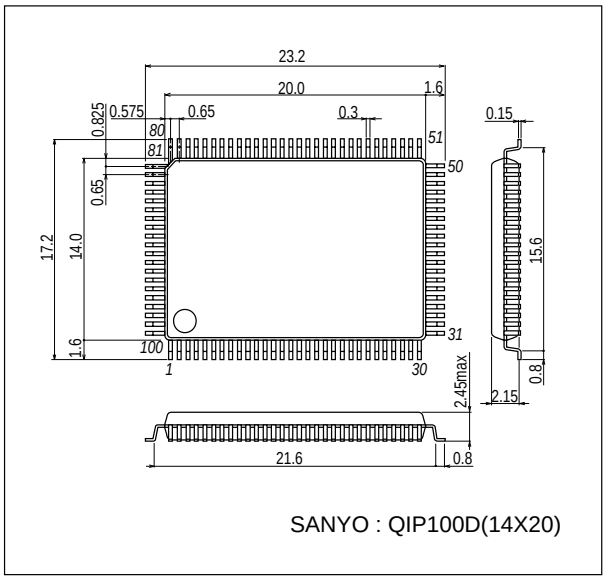
N2206HKIM B8-8529 No.A0573-1/13

Package Dimensions

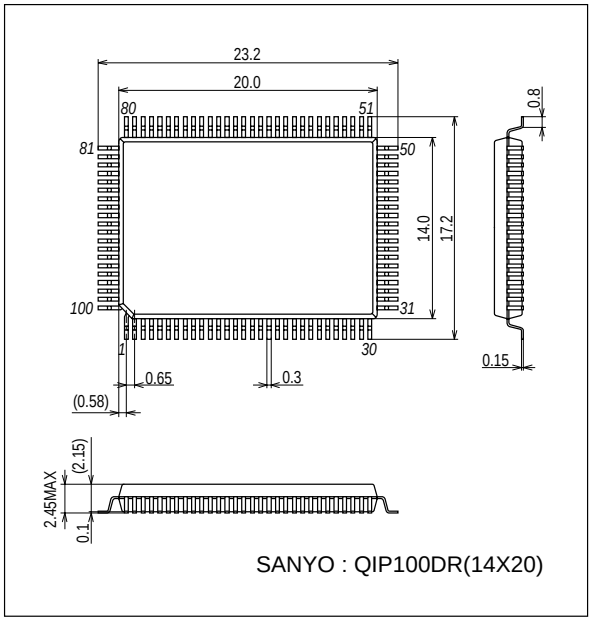
unit: mm (typ)
3180 [LC7940KD]



SANYO : QIP100D(14X20)

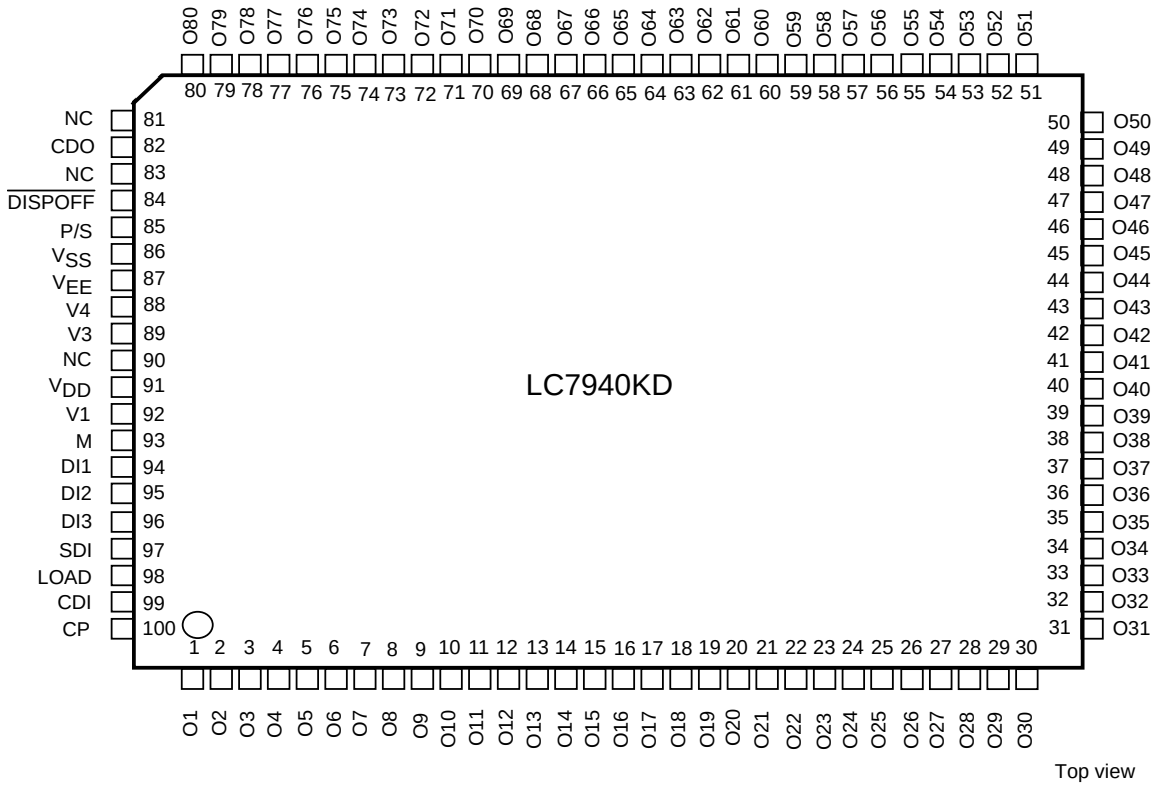
Package Dimensions

unit: mm (typ)
3329 [LC7941KDR]

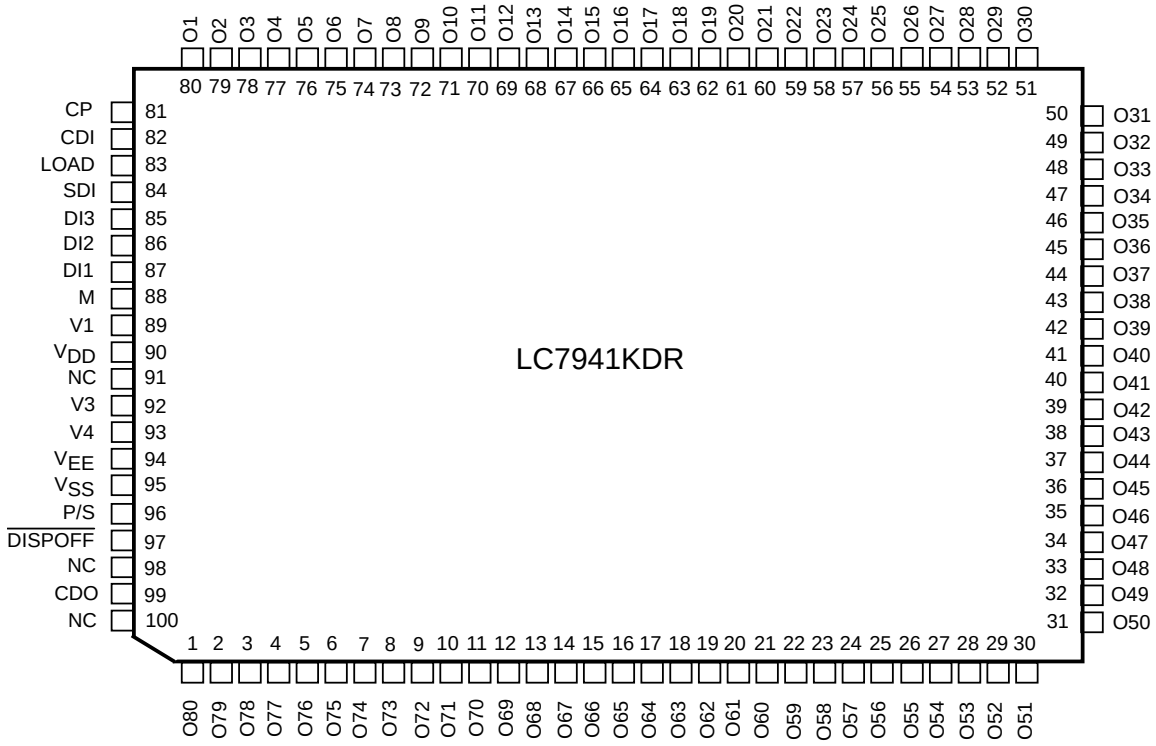


SANYO : QIP100DR(14X20)

Pin Assignment

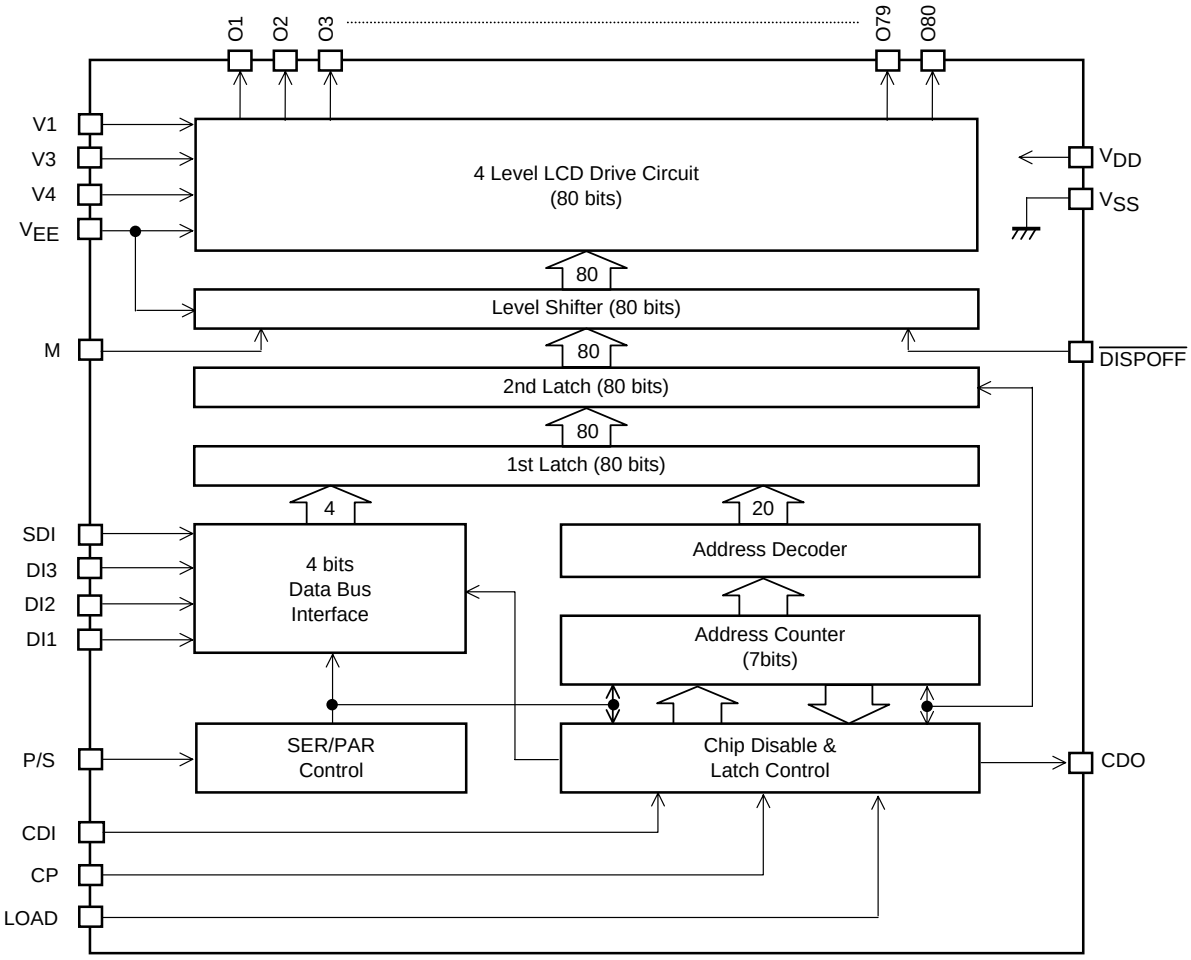


Top view



Top view

Block Diagram



Pin Function

<table>
<tr><th colspan="2">Pin No</th><th rowspan="2">Symbol</th><th rowspan="2">I/O</th><th rowspan="2">Function</th></tr>
<tr><th>LC7940KD</th><th>LC7941KDR</th></tr>
<tr><td>91</td><td>90</td><td>V_{DD}</td><td rowspan="3">Supply</td><td rowspan="3">LCD panel drive voltage supplies
V_{DD}-V_{SS} is the logic supply.
V_{DD}-V_{EE} is the LCD supply.</td></tr>
<tr><td>86</td><td>95</td><td>V_{SS}</td></tr>
<tr><td>87</td><td>94</td><td>V_{EE}</td></tr>
<tr><td>92</td><td>89</td><td>V1</td><td rowspan="3">Supply</td><td rowspan="3">LCD panel drive voltage supplies
V1 and V_{EE} are selected levels.
V3 and V4 are not-selected levels.</td></tr>
<tr><td>89</td><td>92</td><td>V3</td></tr>
<tr><td>88</td><td>93</td><td>V4</td></tr>
<tr><td>100</td><td>81</td><td>CP</td><td>I</td><td>Display data input clock (falling edge trigger).</td></tr>
<tr><td>99</td><td>82</td><td>CDI</td><td>I</td><td>Chip disable.
Data is read in When LOW, and not read in When HIGH.</td></tr>
<tr><td>98</td><td>83</td><td>LOAD</td><td>I</td><td>Display data latch clock (falling edge trigger).
On the falling edge, the LCD drive signals set by the display data are output.</td></tr>
<tr><td>97</td><td>84</td><td>SDI</td><td>I</td><td>Serial data input.</td></tr>
<tr><td>96</td><td>85</td><td>DI3</td><td>I</td><td rowspan="3">4-bit parallel data input pins.
<table><tr><th>Data input</th><th colspan="3">LCD driver output</th></tr><tr><td>SDI</td><td>O4</td><td>O8</td><td rowspan="4">→</td><td>O80</td></tr><tr><td>DI3</td><td>O3</td><td>O7</td><td>O79</td></tr><tr><td>DI2</td><td>O2</td><td>O6</td><td>O78</td></tr><tr><td>DI1</td><td>O1</td><td>O5</td><td>O77</td></tr></table>In serial data input mode, DI1 to DI3 should all be tied HIGH or LOW.</td></tr>
<tr><td>95</td><td>86</td><td>DI2</td><td>I</td></tr>
<tr><td>94</td><td>87</td><td>DI1</td><td>I</td></tr>
<tr><td>93</td><td>88</td><td>M</td><td>I</td><td>LCD panel drive voltage output alternation control signal.</td></tr>
<tr><td>85</td><td>96</td><td>P/S</td><td>I</td><td>Data input mode select. 4-bit parallel input when HIGH, and serial input when LOW.</td></tr>
<tr><td>82</td><td>99</td><td>CDO</td><td>O</td><td>Cascade connection pin for extension segment drivers.
Data is read out when HIGH. Goes LOW after data is read out.
Connected to the CDI input of the next chip.</td></tr>
<tr><td>1 to 80</td><td>80 to 1</td><td>O1 to O80</td><td>O</td><td>LCD drive outputs.
The output drive level is determined by the display data, M signal and $\overline{\text{DISPOFF}}$ input as shown below.
<table><tr><th>M</th><th>Q</th><th>$\overline{\text{DISPOFF}}$</th><th>Output</th></tr><tr><td>L</td><td>L</td><td>H</td><td>V3</td></tr><tr><td>L</td><td>H</td><td>H</td><td>V1</td></tr><tr><td>H</td><td>L</td><td>H</td><td>V4</td></tr><tr><td>H</td><td>H</td><td>H</td><td>V_{EE}</td></tr><tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr></table>Note* don’t care (tied HIGH or LOW)</td></tr>
<tr><td>84</td><td>97</td><td>$\overline{\text{DISPOFF}}$</td><td>I</td><td>O1 to O80 output control input pin.
When LOW, V1 is output on the O1 to O80 outputs.
See the truth table.</td></tr>
<tr><td>81</td><td>91</td><td>NC</td><td rowspan="3">-</td><td rowspan="3">No connection.</td></tr>
<tr><td>83</td><td>98</td><td>NC</td></tr>
<tr><td>90</td><td>100</td><td>NC</td></tr>
</table>

Specifications

Absolute Maximum Ratings at Ta=25±2°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage (logic)	V_{DD} max	-	-0.3 to +7.0	V
Maximum supply voltage (LCD)	V_{DD}-V_{EE} max	*1	0 to 22	V
Maximum input voltage	V_I max	-	-0.3 to V_{DD} +0.3	V
Operating temperature range	Topr	-	-20 to +85	°C
Storage temperature range	Tstg	-	-40 to +125	°C

Note *1 The following relations between elements should be maintained:
$V_{DD} \geq V1 > V3 > V4 > V_{EE}$, V_{DD}-V3≤7V, V4-V_{EE}≤7V

Allowable Operating Ranges at Ta = -20 to 85°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage (logic)	V_{DD}	-	2.7	-	5.5	V
Supply voltage (LCD)	V_{DD}-V_{EE}	*2, 3	8	-	20	V
Input high level voltage	V_{IH}	CP, CDI, DI1 to DI3, M, SDI, P/S, $\overline{\text{DISPOFF}}$, and LOAD	0.8V_{DD}	-	-	V
Input low level voltage	V_{IL}	CP, CDI, DI1 to DI3, M, SDI, P/S, $\overline{\text{DISPOFF}}$, and LOAD	-	-	0.2V_{DD}	V
CP Shift clock frequency	f_{CP}	CP	-	-	3.3	MHz
CP pulse width	t_{WC}	CP	100	-	-	ns
LOAD pulse width	t_{WL}	LOAD	100	-	-	ns
DIn and SDI to CP setup time	t_{SETUP}	DIn and SDI to CP	80	-	-	ns
DIn and SDI to CP hold time	t_{HOLD}	DIn and SDI to CP	80	-	-	ns
CP to LOAD time	t_{CL1}	CP to LOAD	0	-	-	ns
	t_{CL2}	CP to LOAD	100	-	-	ns
LOAD to CP time	t_{LC}	LOAD to CP	100	-	-	ns
CP rise time	t_R	CP	-	-	50	ns
CP fall time	t_F	CP	-	-	50	ns
LOAD rise time	t_{RL}	LOAD	-	-	50	ns
LOAD fall time	t_{FL}	LOAD	-	-	50	ns

Note *2 The following relations between elements should be maintained:
$V_{DD} \geq V1 > V3 > V4 > V_{EE}$, V_{DD}-V3≤7V, V4-V_{EE}≤7V

*3 When the power is turned on, either the logic system power must be turned on before the LCD drive system power or else they must both be turned on at the same time. When the power is turned off, either the LCD drive system power must be turned off before the logic system power, or else both must be turned off at the same time.

Electrical Characteristics at Ta = 25±2°C, V_{DD} = 2.7 to 5.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level current	I_{IH}	V_{IN} = V_{DD}: LOAD, CP, CDI, P/S, DI1 to DI3, SDI, M, and $\overline{DISPOFF}$	-	-	1	μA
Input low level current	I_{IL}	V_{IN} = V_{SS}: LOAD, CP, CDI, P/S, DI1 to DI3, SDI, M, and $\overline{DISPOFF}$	-1	-	-	μA
Output high level voltage	V_{OH}	I_{OH} = -400μA: CDO	V_{DD}-0.4	-	-	V
Output low level voltage	V_{OL}	I_{OL} = 400μA: CDO	-	-	0.4	V
Driver on resistance	R_{ON}	V_{DD}-V_{EE} = 18V, $\|V_{DE}$-$V_o\|$ = 0.25V *4	-	0.7	2	kΩ
Standby current drain	I_{ST}	CDI = V_{DD}, V_{DD}-V_{EE} = 18V, CP = 3.3MHz, Output unloaded: V_{SS}	-	-	200	μA
Operating current drain	I_{SS} *5	V_{DD}-V_{EE} = 18V, CP = 3.3MHz, LOAD = 5.156kHz M = 52Hz: V_{SS}	-	-	1.0	mA
	I_{EE} *6	V_{DD}-V_{EE} = 18V, CP = 3.3MHz, LOAD = 5.156kHz M = 52Hz: V_{EE}	-	-	0.1	mA

Note *4 V_{DE} = one of V1, V3, V4 or V_{EE}. V1 = V_{DD}, V3 = 9/11(V_{DD}-V_{EE}), V4 = 2/11(V_{DD}-V_{EE})

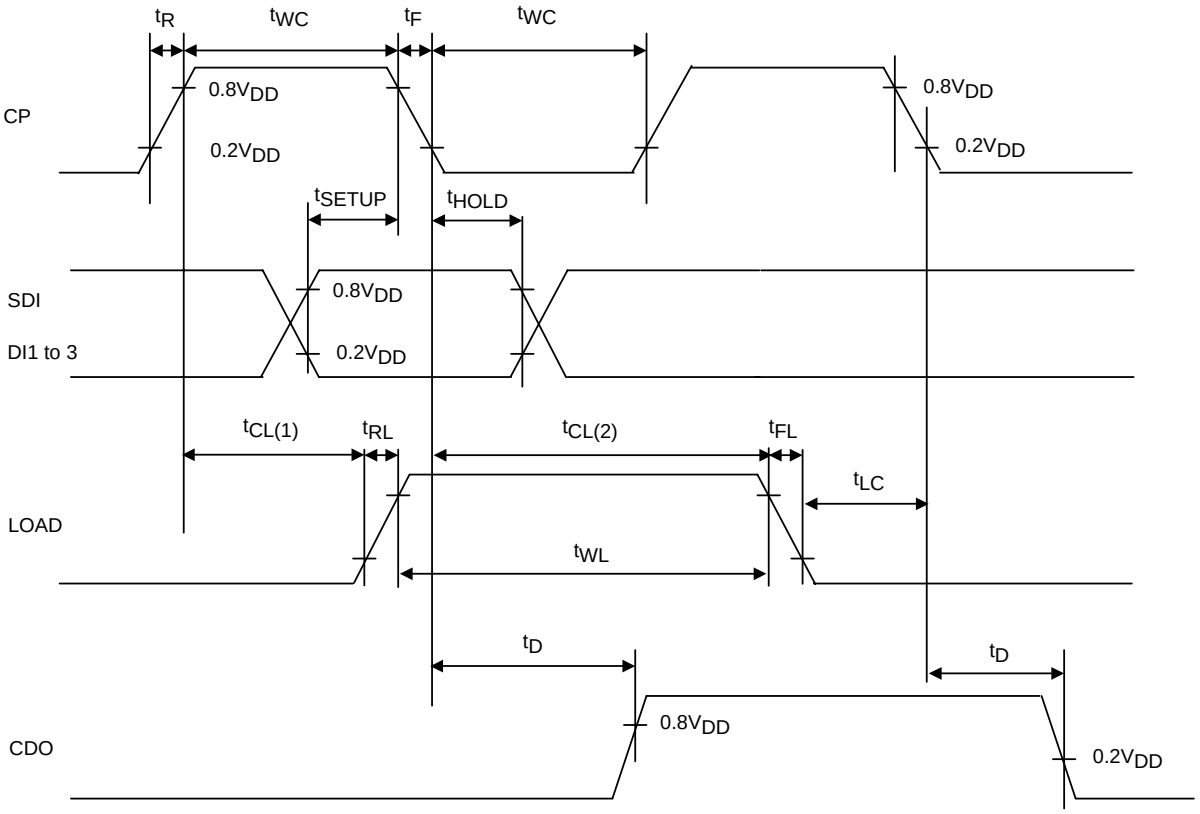
*5 I_{SS} is the current flowing from V_{DD}-V_{SS}.

*6 I_{EE} is the current flowing from V_{DD}-V_{EE}

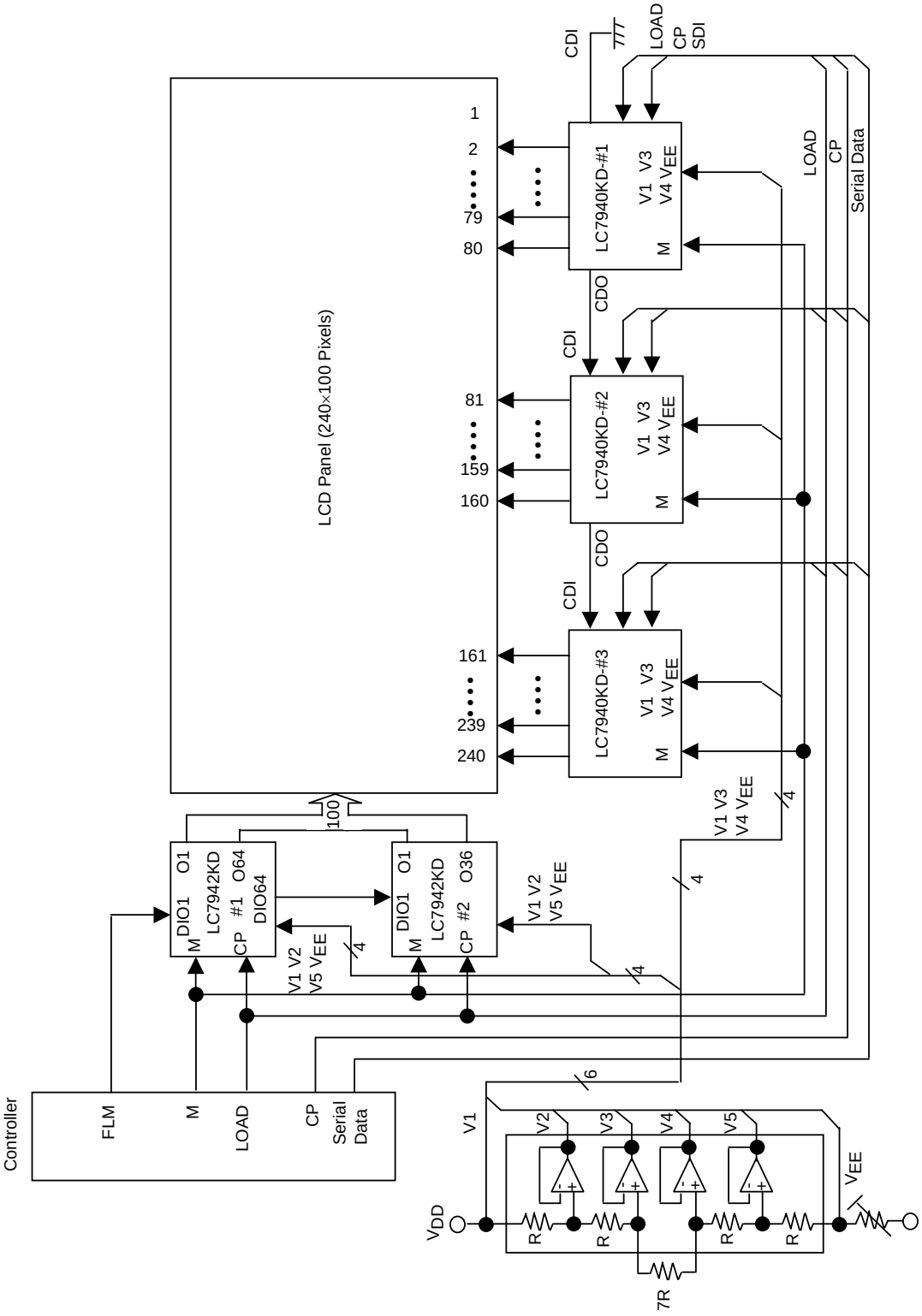
Switching Characteristics at Ta = 25±2°C, V_{SS} = 0V, V_{DD} = 2.7 to 5.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output delay time	t_D	CL=30pF: CDO	-	-	200	ns

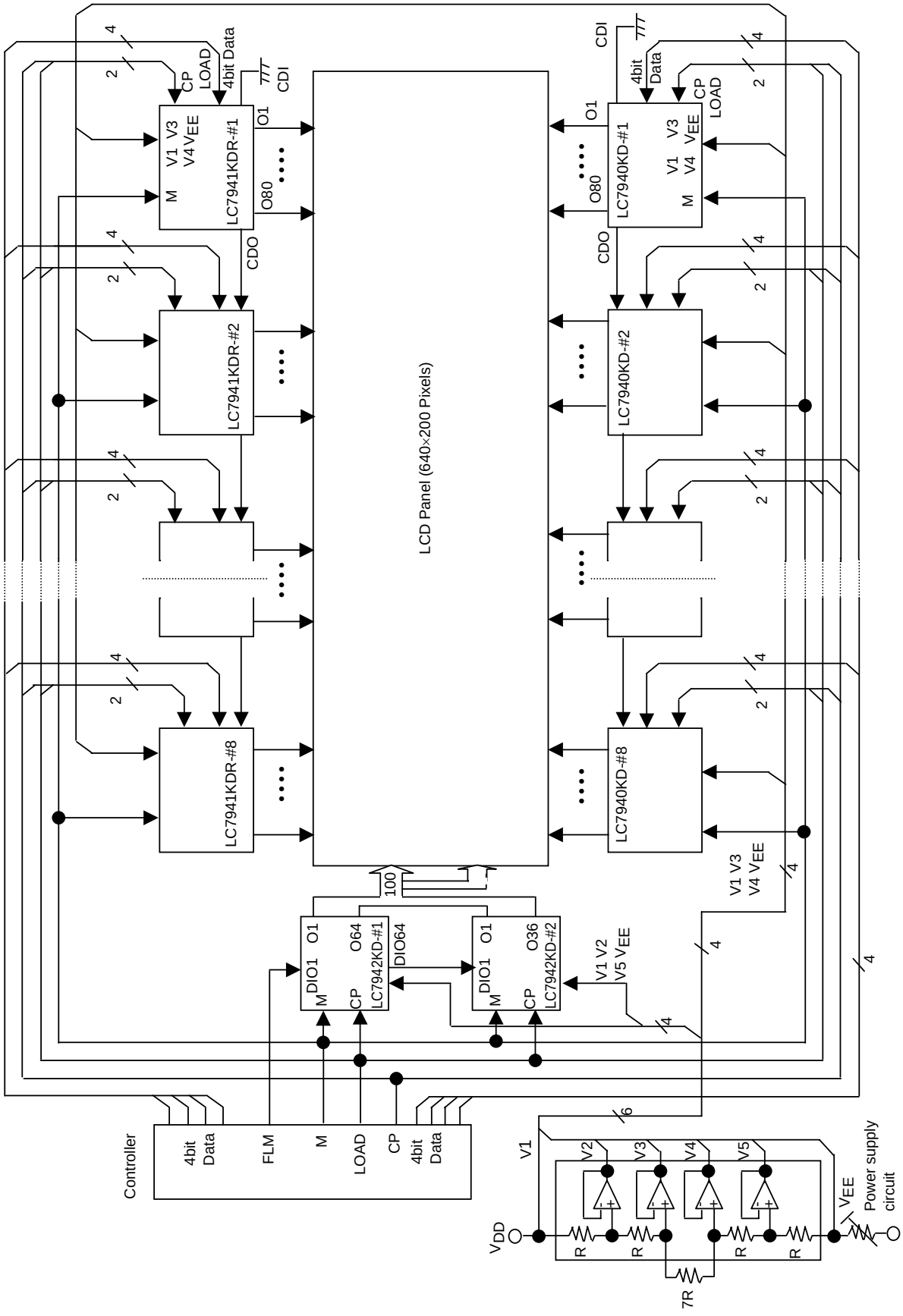
Switching Characteristics Diagram



Application Notes LCD Panel1



Application Notes LCD Panel2

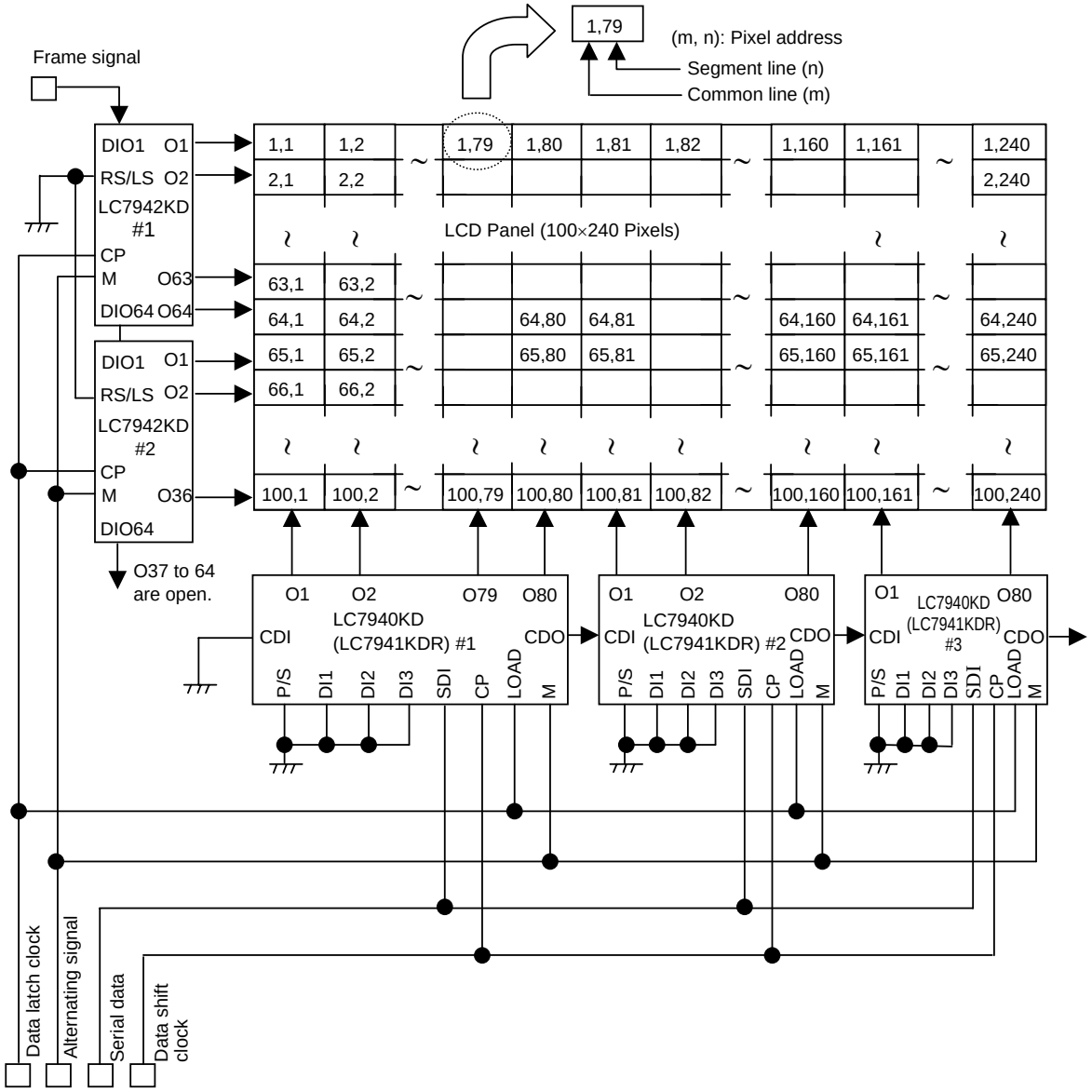


100×240-Pixel LCD Panel Application

A100×240-Pixel LCD Panel requires the following drivers.

- 3×LC7940KD (or LC7941KDR) drivers
- 2×LC7942KD drivers

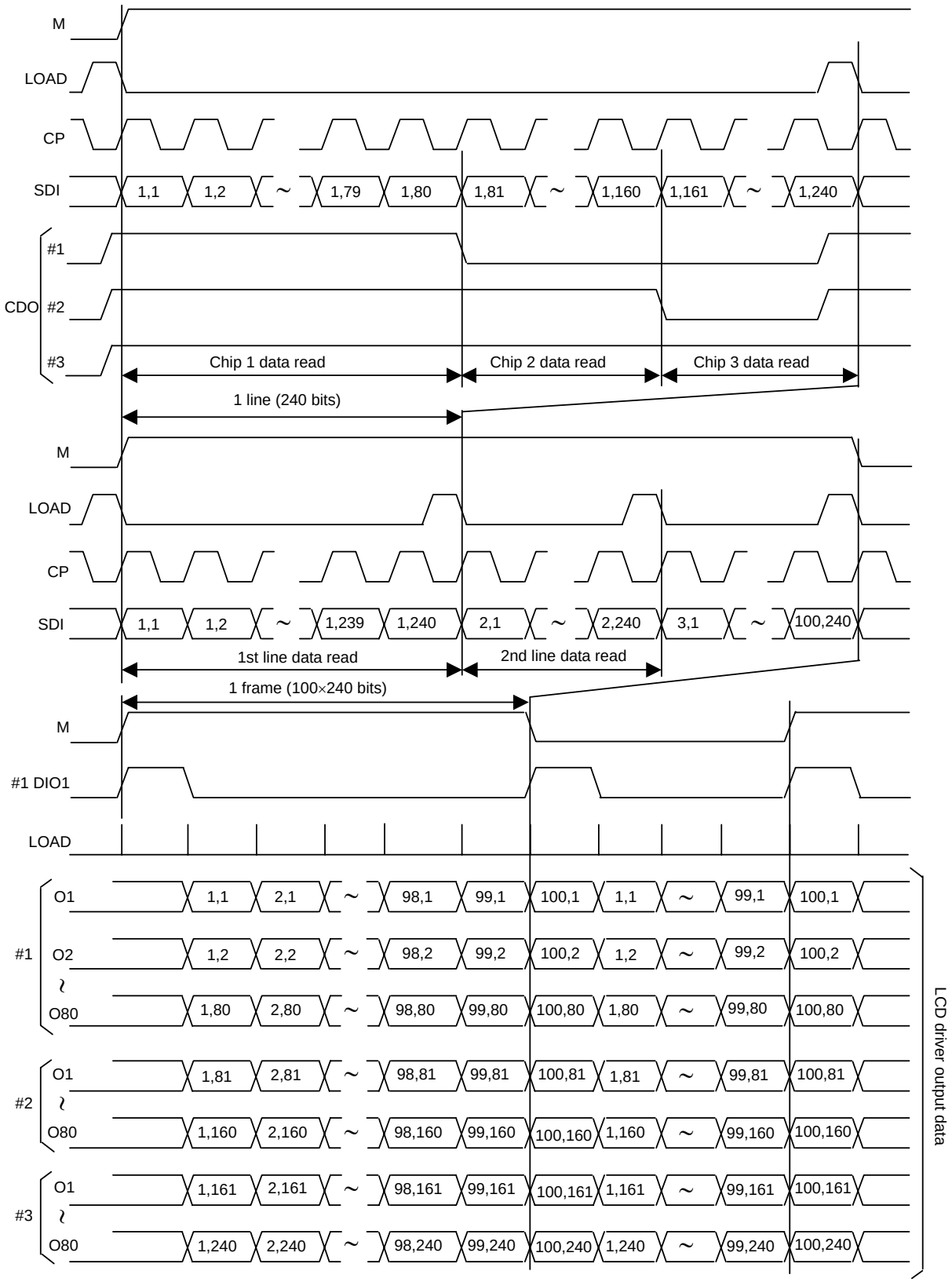
An example using 1/100 duty cycle is shown below.



(1) The LC7942KD chips are cascaded by connecting DIO64 on chip 1 to DIO1 on chip 2.
For a 100-bit shift register, O37 to O64 on chip 2 are left open.

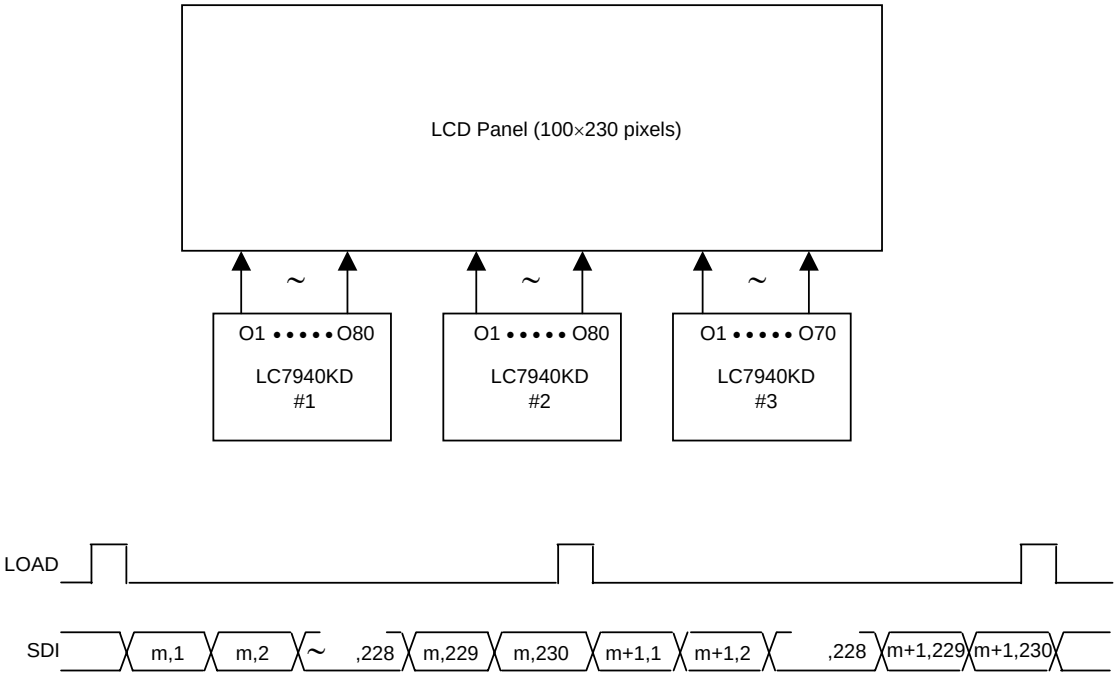
(2) The LC7940KD (or LC7941KDR) chips are cascaded by connecting CDO on chip 1 to CDI on chip 2, and CDO on chip 2 to CDI on chip 3. CDI on chip 1 is tied to GND, and CDO on chop 3 is not used. This configulation allows the input of 240-bit serial data.

100×240-pixel LCD Panel Timing Diagram

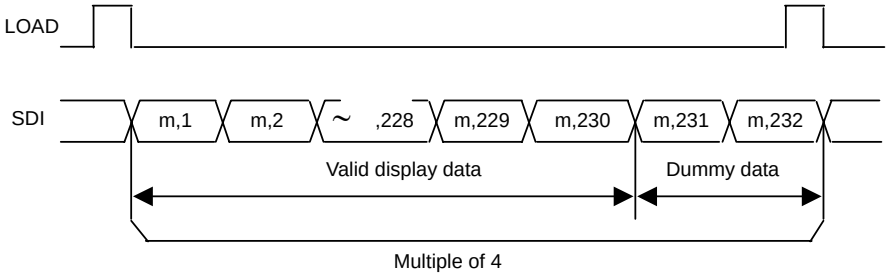


Segment Data Not Multiples of 4

Example.



If this timing data is sent, data elements (m, 229), (m, 230), (m+1, 229),(m+1, 230)… will not appear in the output (O69 and O70 on chip 3). This is because the LC7940KD (or LC7941KDR) converts serial/parallel data in 4-bit units, which also decrease power dissipation.
For data that is not a multiple of 4, like 230, the following scheme is used.



In this case, (m, 231) is output on O71 on chip 3, and (m, 232) on O72 on chip 3. However, these outputs are not connected to the panel and are, therefore, invalid.