SONY

CXL1506M/N

CMOS-CCD 1H/2H Delay Line for PAL

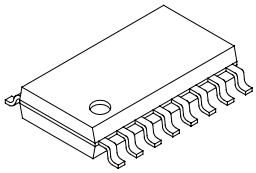
For the availability of this product, please contact the sales office.

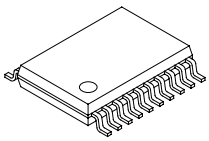
Description

The CXL1506M/N is a CMOS-CCD delay line developed for video signal processing. Usage in conjunction with an external low pass filter provides 1H and 2H delay signals simultaneously (For PAL signals).

CXL1506M
16 pin SOP (Plastic)

CXL1506N
20 pin SSOP (Plastic)





Features

- Single power supply (5V)
- Low power consumption
- Built-in peripheral circuits
- Built-in tripling PLL circuit
- For PAL signals
- 1 input and 2 outputs
  (Outputs for both 1H and 2H delays)

Block Diagram **CXL1506M**
CXL1506N

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation			
	P_D CXL1506M	400	mW
	CXL1506N	300	mW

Recommended Operating Voltage (Ta = 25°C)

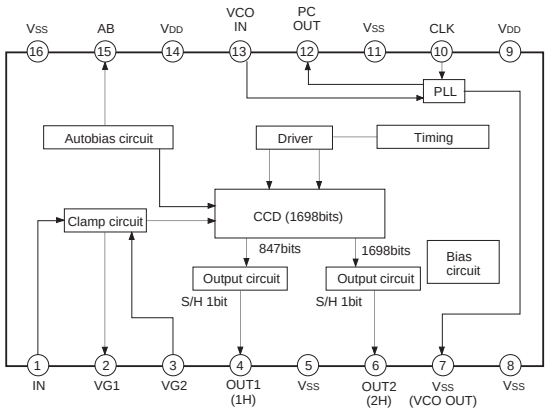
	V_{DD}	5 ± 0.25	V

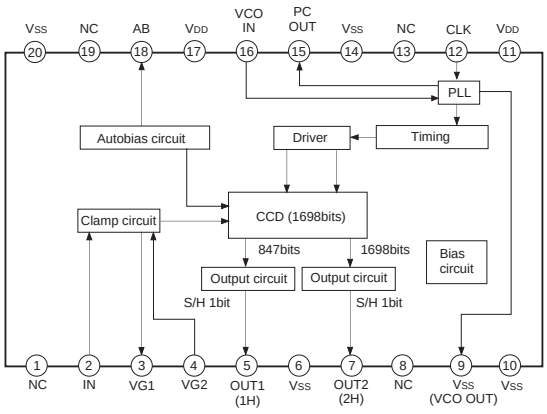
Recommended Clock Conditions (Ta = 25°C)

• Input clock amplitude	V_{CLK}	0.2 to 1.0Vp-p (0.4Vp-p Typ.)	
• Input clock frequency	f_{CLK}	4.433619	MHz
• Input clock waveform	sine wave		

Input Signal Amplitude

	V_{SIG}	575 (Max.) mVp-p (at internal clamp condition)	





E89X22C78-PS

Pin Description (CXL1506M)

Pin No.	Symbol	I/O	Description	Impedance [Ω]
1	IN	I	Signal input (Non-inverted signal)	> 10kΩ (at no clamp)
2	VG1	O	Gate bias 1 DC output	
3 (Note)	VG2	I	Gate bias 2 DC input	
4	OUT1	O	1H signal output (Inverted signal)	40 to 500Ω
5	V_{SS}	—	GND	
6	OUT2	O	2H signal output (Inverted signal)	40 to 500Ω
7	V_{SS} (VCO OUT)	(O)	GND or VCO output (3fsc)	
8	V_{SS}	—	GND	
9	V_{DD}	—	Power supply (5V)	
10	CLK	I	Clock input (fsc)	> 10kΩ
11	V_{SS}	—	GND	
12	PC OUT	O	Phase comparator output	
13	VCO IN	I	VCO input	
14	V_{DD}	—	Power supply (5V)	
15	AB	O	Autobias DC output	600 to 200kΩ
16	V_{SS}	—	GND	

Note) Description of VG2

Control of input signal clamp condition

0V … Sync tip clamp condition

5V … Center bias condition

The input signal is biased to approx. 2.1V by means of the IC internal resistance (approx. 10kΩ). In this mode the input signal is limited to the APL 50% and the maximum input signal amplitude is at 200mVp-p.

Pin Description (CXL1506N)

Pin No.	Symbol	I/O	Description	Impedance [Ω]
1	NC	—	—	
2	IN	I	Signal input (Non-inverted signal)	> 10kΩ (at no clamp)
3	VG1	O	Gate bias 1 DC output	
4 (Note)	VG2	I	Gate bias 2 DC input	
5	OUT1	O	1H signal output (Inverted signal)	40 to 500Ω
6	V_{SS}	—	GND	
7	OUT2	O	2H signal output (Inverted signal)	40 to 500Ω
8	NC	—	—	
9	V_{SS} (VCO OUT)	(O)	GND or VCO output (3fsc)	
10	V_{SS}	—	GND	
11	V_{DD}	—	Power supply (5V)	
12	CLK	I	Clock input (fsc)	> 10kΩ
13	NC	—	—	
14	V_{SS}	—	GND	
15	PC OUT	O	Phase comparator output	
16	VCO IN	I	VCO input	
17	V_{DD}	—	Power supply (5V)	
18	AB	O	Autobias DC output	600 to 200kΩ
19	NC	—	—	
20	V_{SS}	—	GND	

Note) Description of VG2

Control of input signal clamp condition

0V … Sync tip clamp condition

5V … Center bias condition

The input signal is biased to approx. 2.1V by means of the IC internal resistance (approx. 10kΩ). In this mode the input signal is limited to the APL 50% and the maximum input signal amplitude is at 200mVp-p.

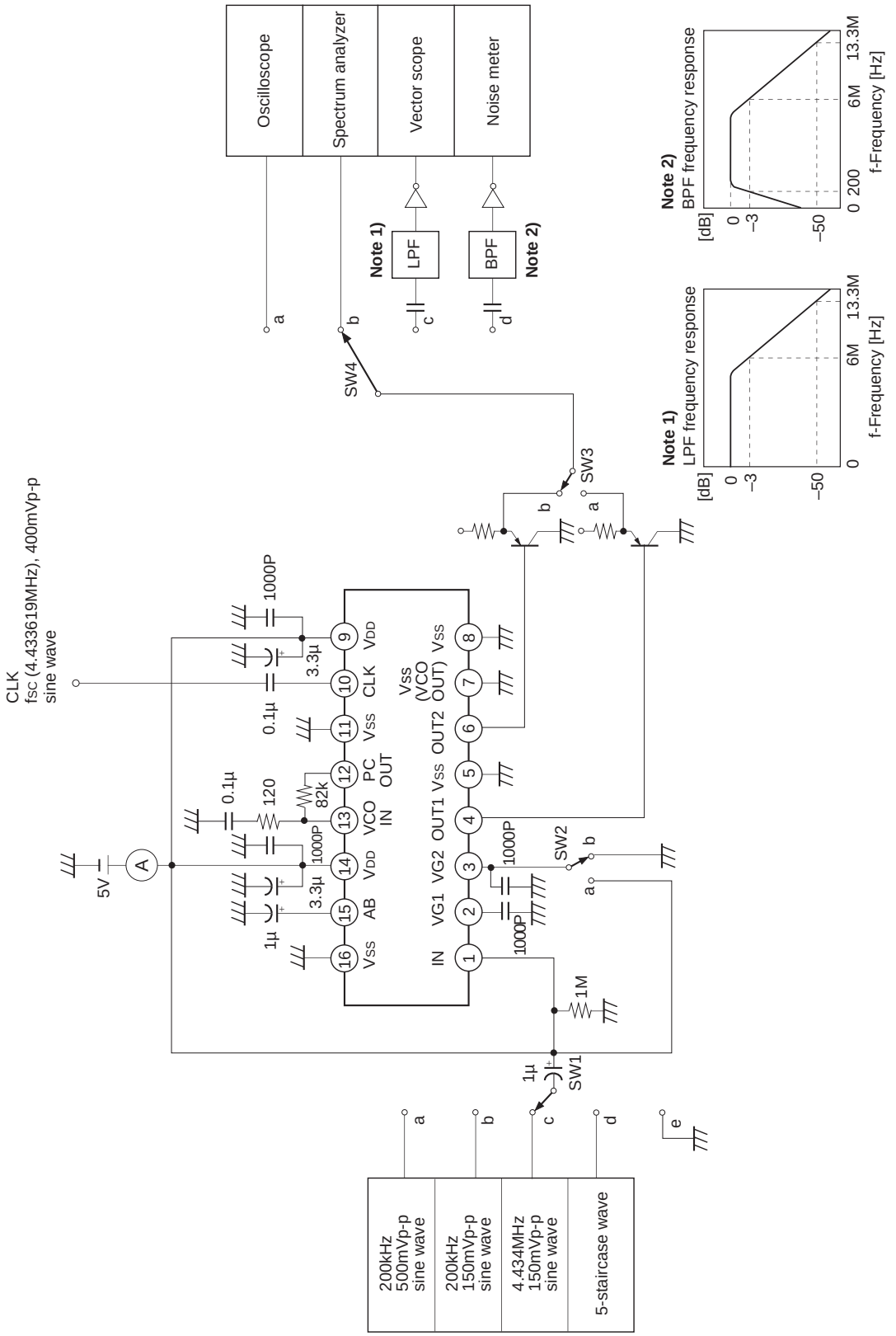
Electrical Characteristics

(Ta = 25°C, V_{DD} = 5V, f_{CLK} = 4.433619MHz, V_{CLK} = 400mVp-p sine wave)

See Electrical Characteristics Test Circuit.

Item	Symbol	Test conditions (Note 1)	SW conditions				Min.	Typ.	Max.	Unit	Note
			1	2	3	4					
Supply current	I_{DD}	—	a	b	a	a	17	27	37	mA	2
Low frequency gain	GL1	200kHz 500mVp-p sine wave	a	b	a	b	–2	0	2	dB	3
	GL2		a	b	b	b	–2	0	2		
Frequency response	fR1	200kHz ↔ 4.434MHz 150mVp-p sine wave	b ↔ c	a	a	b	–2.7	–1.7	–0.7	dB	4
	fR2		b ↔ c	a	b	b	–2.8	–1.8	–0.8		
Differential gain	DG1	5 staircase wave	d	b	a	c	—	5	7	%	5
	DG2		d	b	b	c	—	5	7		
Differential phase	DP1	5 staircase wave	d	b	a	c	—	5	7	degree	5
	DP2		d	b	b	c	—	5	7		
S/N ratio	SN1	No signal input	e	b	a	d	52	56	—	dB	6
	SN2		e	b	b	d	52	56	—		
S/H pulse coupling	CP1	No signal input	e	b	a	a	—	—	350	mVp-p	7
	CP2		e	b	b	a	—	—	350		

Electrical Characteristics Test Circuit (CXL1506M)



* When using CXL1506N, change the connection terminal only.
(See the block diagram and pin configuration. For NC pins, ground them.)

Notes)

1) By switching SW2, input condition turns out as follows.

SW2 condition	Input condition
a	Center bias condition (approx. 2.1V) Approx. 2.1V bias is applied internally to the input signal
b	Sync tip and clamp conditions

2) This is the IC supply current value during clock and signal input.

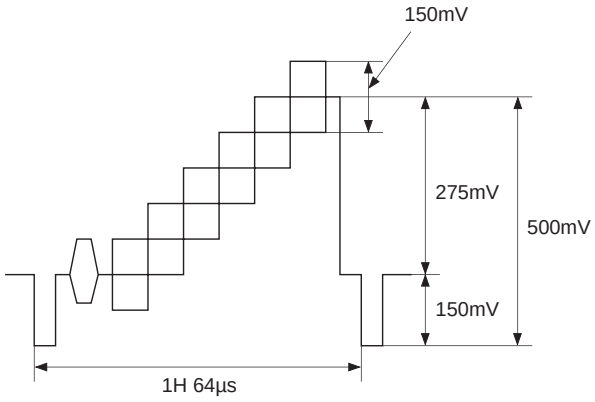
3) GL is the output gain of pin OUT when a 500mVp-p, 200kHz sine wave is fed to pin IN.

$$GL = 20 \log \frac{\text{pin OUT output voltage [mVp-p]}}{500 \text{ [mVp-p]}} \text{ [dB]}$$

4) Indicates the dissipation at 4.434MHz in relation to 200kHz. From the output voltage at pin OUT when a 150mVp-p, 200kHz sine wave is fed to pin IN, and from the output voltage at pin OUT when a 150mVp-p, 4.434MHz sine wave is fed to same, calculation is made according to the following formula.

$$fR = 20 \log \frac{\text{pin OUT output voltage (4.434MHz) [mVp-p]}}{\text{pin OUT output voltage (200kHz) [mVp-p]}} \text{ [dB]}$$

5) The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the following figure is fed, are tested with a vector scope:



6) The noise level of the output signal at no-input signal is tested with a video noise meter in the Sub Carrier Trap mode at BPF 100kHz to 5MHz. (Vn [Vrms])
The signal component is determined either by testing the output voltage (the same testing system as for noise level) at the input of 350mVp-p, 200kHz, or by utilizing values from GL to calculate according to the following formula. (Vs [Vp-p])

(Example of Vs calculation)

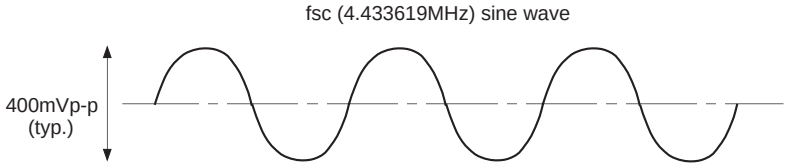
$$Vs = 0.35 \times 10^{\frac{GL}{20}}$$

(Example of SN ratio calculation)

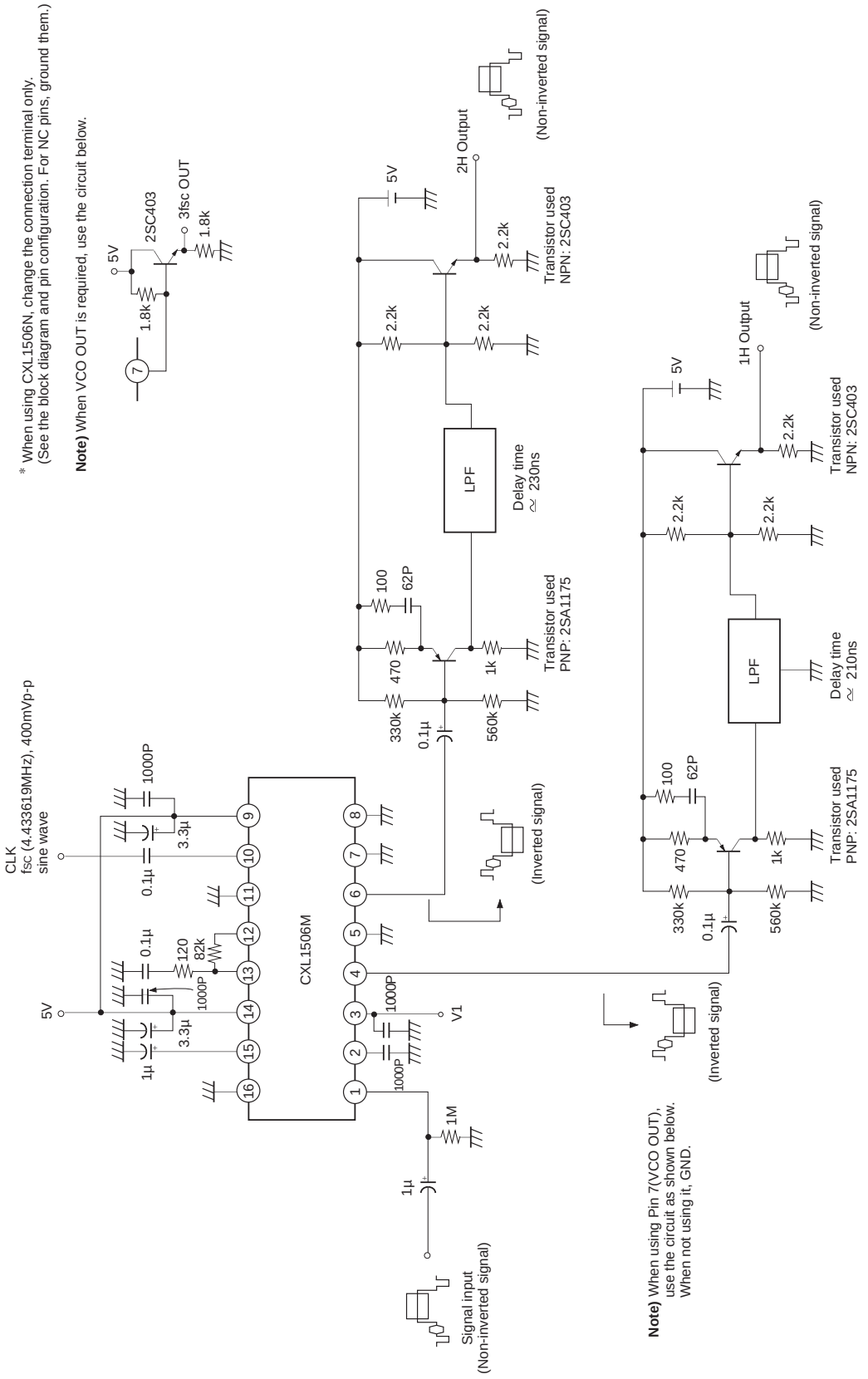
$$SN = 20 \log \frac{Vn \text{ (noise component) [Vrms]}}{Vs \text{ (signal component) [Vp-p]}} \text{ [dB]}$$

7) The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested.

Clock



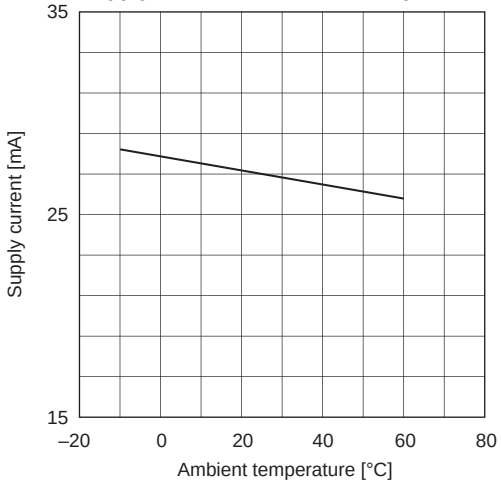
Application Circuit (CXL1506M)



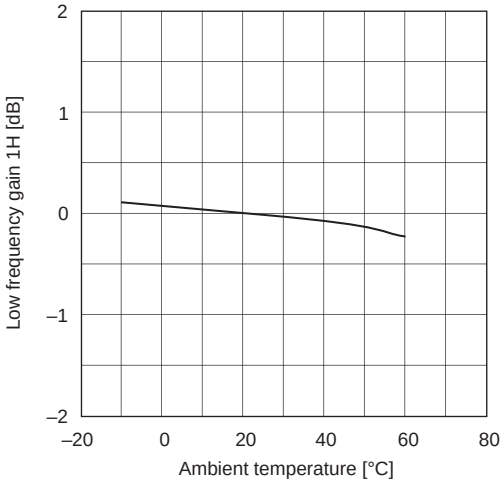
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

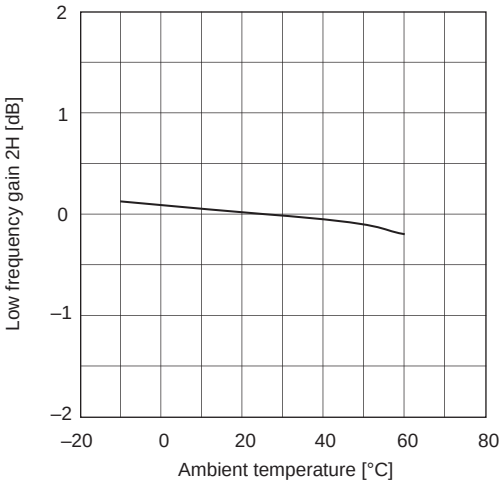
Supply current vs. Ambient temperature



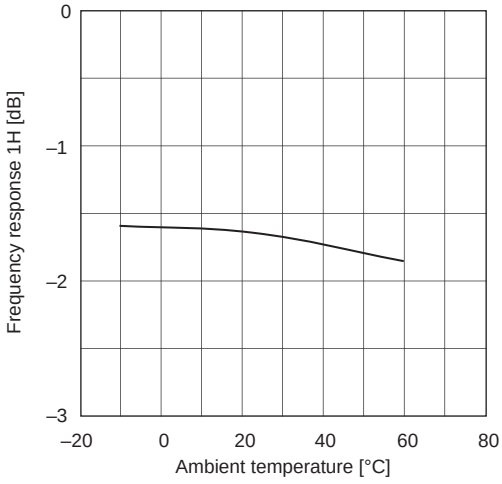
Low frequency gain (1H) vs. Ambient temperature



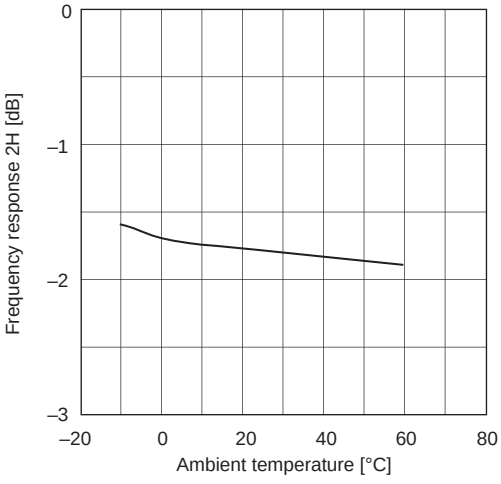
Low frequency gain (2H) vs. Ambient temperature



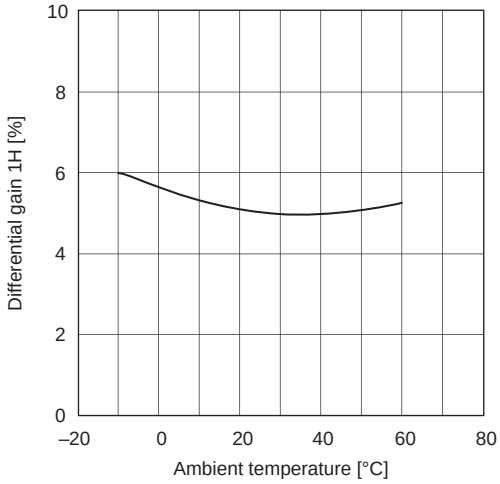
Frequency response (1H) vs. Ambient temperature



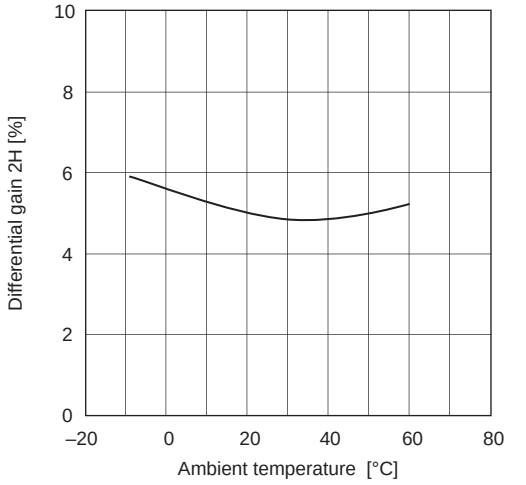
Frequency response (2H) vs. Ambient temperature



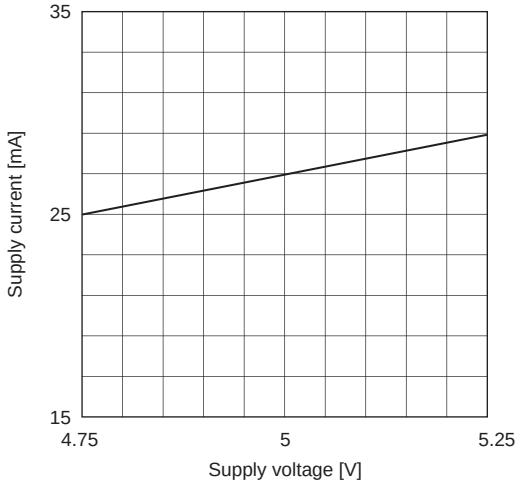
Differential gain (1H) vs. Ambient temperature



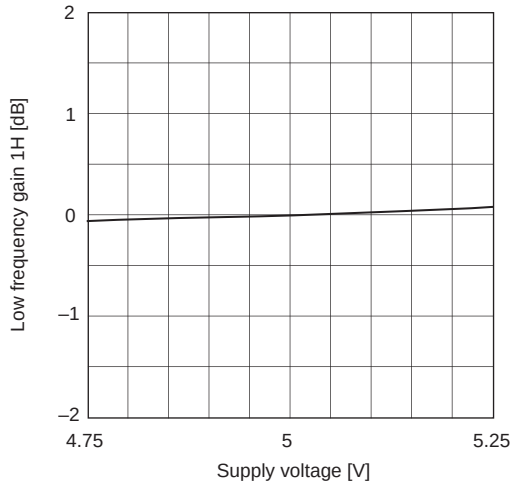
Differential gain (2H) vs. Ambient temperature



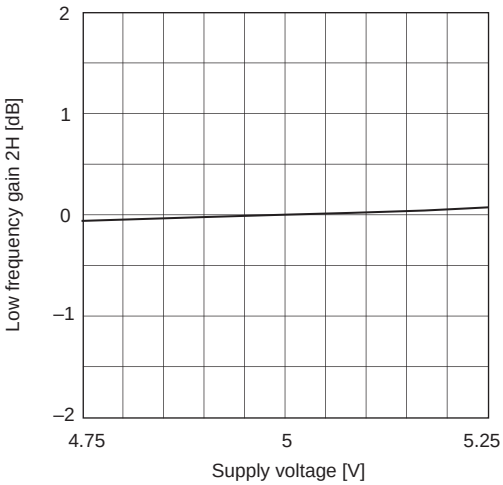
Supply current vs. Supply voltage



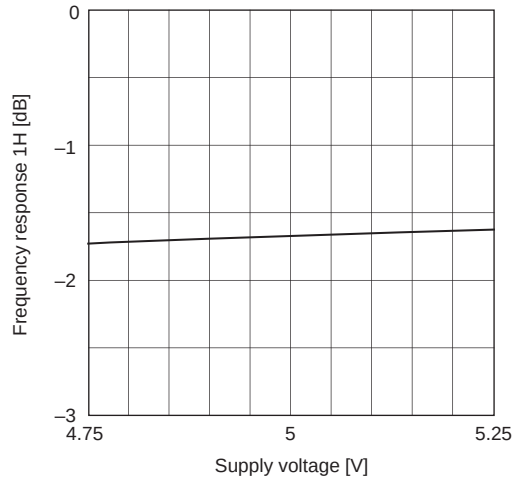
Low frequency gain (1H) vs. Supply voltage



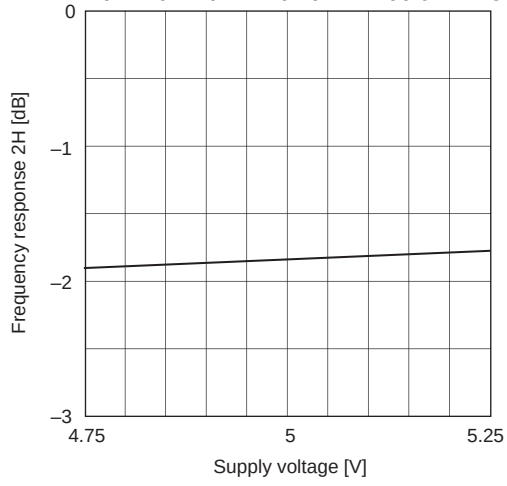
Low frequency gain (2H) vs. Supply voltage



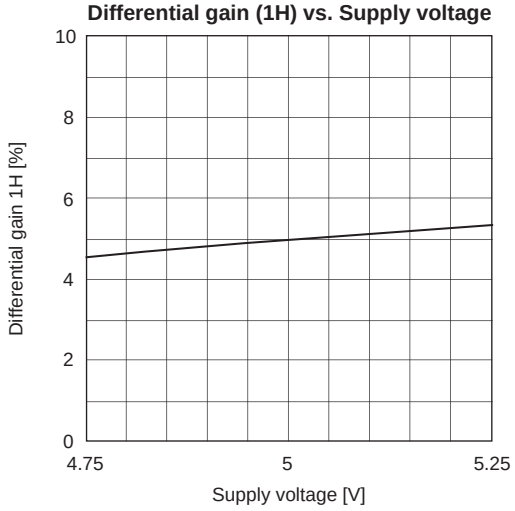
Frequency response (1H) vs. Supply voltage



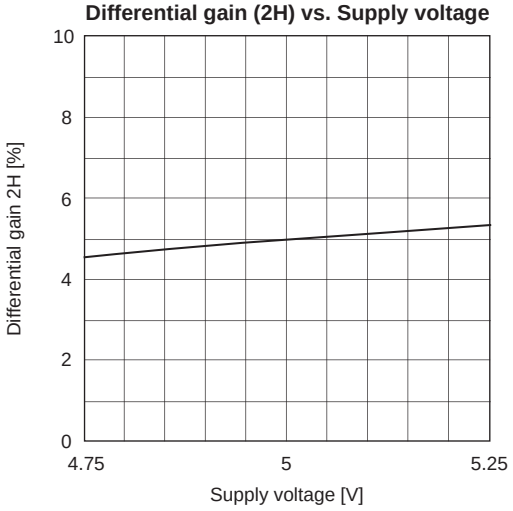
Frequency response (2H) vs. Supply voltage



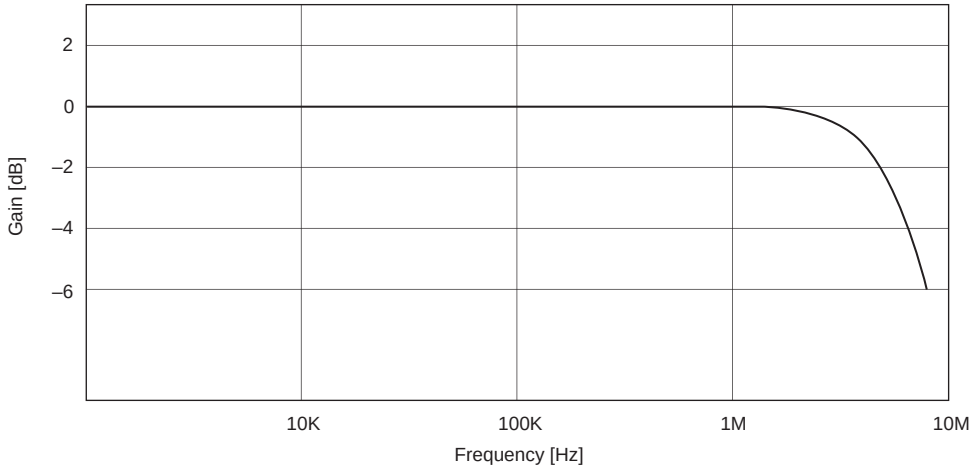
Differential gain (1H) vs. Supply voltage



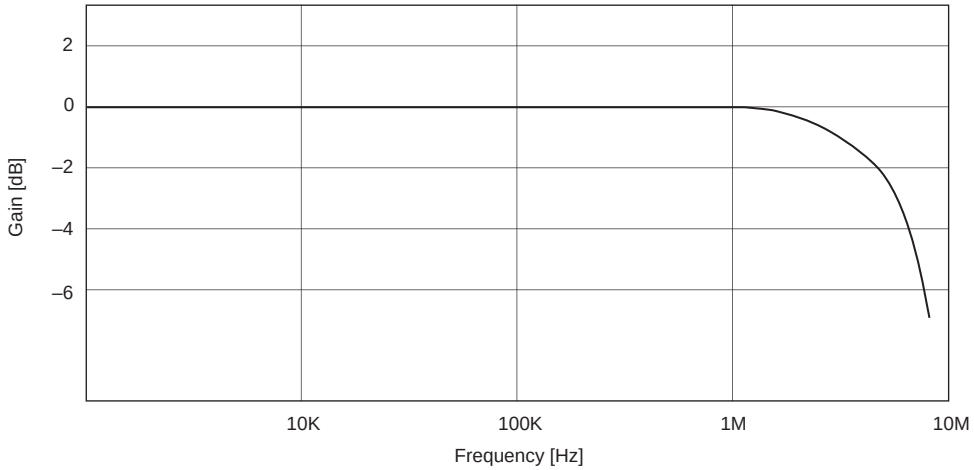
Differential gain (2H) vs. Supply voltage



Frequency response (1H)



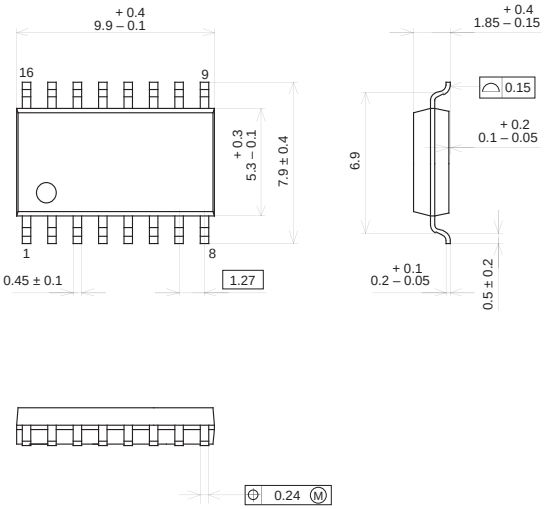
Frequency response (2H)



Note) 1H and 2H shown in brackets indicate 1H and 2H outputs.

Package Outline Unit: mm

CXL1506M 16PIN SOP (PLASTIC)

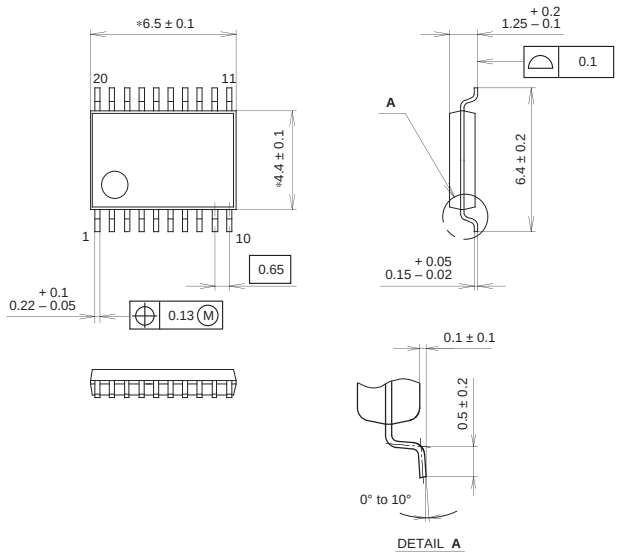


SONY CODE	SOP-16P-L01
EIAJ CODE	SOP016-P-0300
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g

CXL1506N 20PIN SSOP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	SSOP-20P-L01
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g