

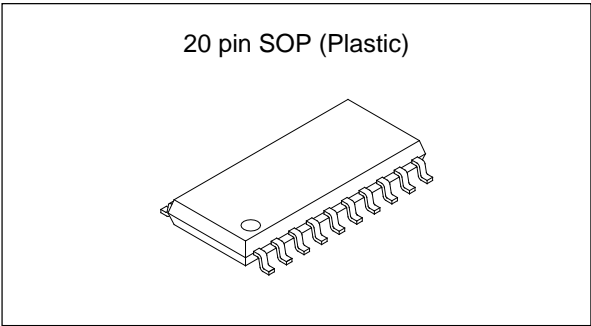
**CCD Vertical Clock Driver**

**Description**

The CXD1268M is a clock driver for CCD vertical register drive.

**Features**

- On-chip 4-channel driver.  
(Binary driver × 2, and trinary driver × 2)
- Low output ON resistance provides optimal drive for large load capacity CCD.



**Applications**

CCD cameras

**Structure**

CMOS

**Absolute Maximum Ratings (GND = 0V, Ta = 25°C)**

• Supply voltage	V <sub>H</sub>	V <sub>L</sub> to V <sub>L</sub> + 25	V
• Supply voltage	V <sub>M</sub>	V <sub>L</sub> to V <sub>L</sub> + 17*1	V
• Supply voltage	V <sub>DD</sub>	GND to GND + 7	V
• Supply voltage	V <sub>L</sub>	GND – 10 to GND	V
• Input voltage	V <sub>i</sub>	–0.5 to V <sub>DD</sub> + 0.5	V
• Input/output clamp diode current	I <sub>ic, loc</sub>	–10 to +10	mA
• Maximum DC load current	I <sub>oDC</sub>	–3 to +3	mA
• Maximum load capacity	C <sub>L</sub>	to 30,000	pF/pin
• Allowable power dissipation	P <sub>D</sub>	to 200	mW
• Storage temperature	T <sub>stg</sub>	–60 to +150	°C

\*1 Use V<sub>M</sub> at less than V<sub>DD</sub>.

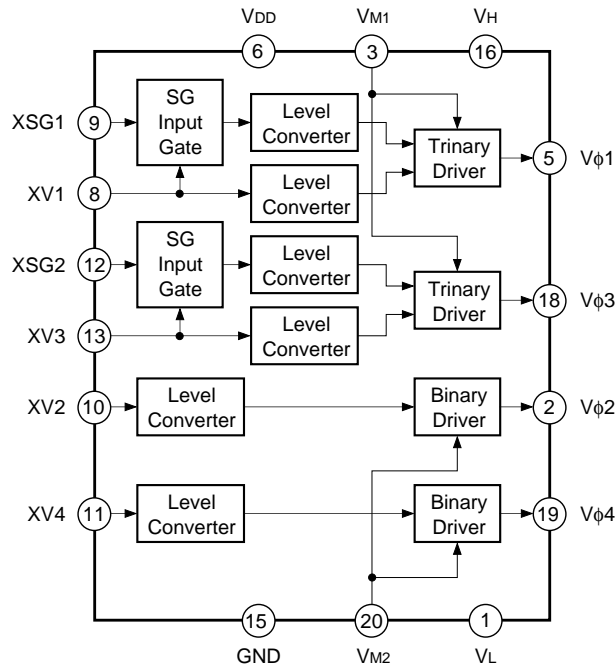
**Recommended Operating Conditions**

• Supply voltage	V <sub>H</sub>	V <sub>M</sub> + 6.5 to V <sub>M</sub> + 15.5	V
• Supply voltage	V <sub>L</sub>	V <sub>M</sub> – 10.0 to V <sub>M</sub> – 7.0	V
• Supply voltage	V <sub>M</sub>	0.0 to 4.0	V
• Supply voltage	V <sub>DD</sub>	4.75 to 5.25	V
• High level input voltage	V <sub>IH</sub> *2	3.5 to V <sub>DD</sub>	V
• Low level input voltage	V <sub>IL</sub> *2	0.0 to 1.0	V
• Operating temperature	T <sub>opr</sub>	–10 to +60	°C

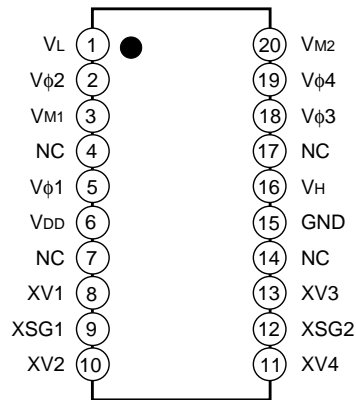
\*2 V<sub>DD</sub> = 5V

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Block Diagram



Pin Configuration (Top View)



## Pin Description

Pin No.	Symbol	I/O	Description
1	V <sub>L</sub>	—	Low level power supply
2	V <sub>φ2</sub>	O	High-voltage output (2 levels: V <sub>M2</sub> , V <sub>L</sub> )
3	V <sub>M1</sub>	—	Middle level power supply for trinary
4	NC		
5	V <sub>φ1</sub>	O	High-voltage output (3 levels: V <sub>H</sub> , V <sub>M1</sub> , V <sub>L</sub> )
6	V <sub>DD</sub>	—	Input section power supply
7	NC		
8	XV1	I	Output control (V <sub>φ1</sub> )
9	XSG1	I	Output control (V <sub>φ1</sub> )
10	XV2	I	Output control (V <sub>φ2</sub> )
11	XV4	I	Output control (V <sub>φ4</sub> )
12	XSG2	I	Output control (V <sub>φ3</sub> )
13	XV3	I	Output control (V <sub>φ3</sub> )
14	NC		
15	GND	—	GND
16	V <sub>H</sub>	—	High level power supply for trinary
17	NC		
18	V <sub>φ3</sub>	O	High-voltage output (3 levels: V <sub>H</sub> , V <sub>M1</sub> , V <sub>L</sub> )
19	V <sub>φ4</sub>	O	High-voltage output (2 levels: V <sub>M2</sub> , V <sub>L</sub> )
20	V <sub>M2</sub>	—	Middle level power supply for binary

## Truth Table

X: Don't care

Input			Output	
XV1, XV3	XSG1, XSG2	XV2, XV4	V <sub>φ1</sub> , V <sub>φ3</sub>	V <sub>φ2</sub> , V <sub>φ4</sub>
H	L	X	V <sub>L</sub>	X
H	H	X	V <sub>L</sub>	X
L	L	X	V <sub>H</sub>	X
L	H	X	V <sub>M1</sub>	X
X	X	L	X	V <sub>M2</sub>
X	X	H	X	V <sub>L</sub>

## Electrical Characteristics

(Unless otherwise specified,  $V_H = 14.5V$ ,  $V_M = 1V$ ,  $V_{DD} = 5V$ ,  $GND = 0V$ ,  $V_L = -6V$ ,

### 1. DC Characteristics

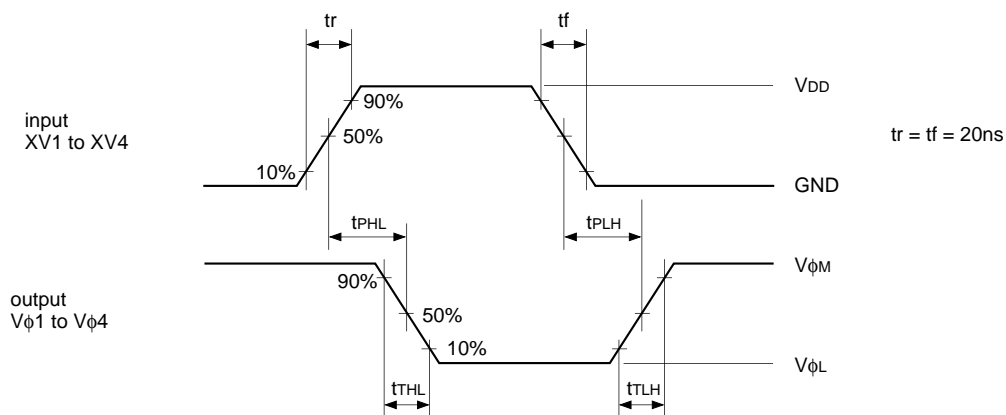
$V_{IL} = GND$ ,  $V_{IH} = V_{DD}$ ,  $T_a = -10$  to  $+60^\circ C$ )

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" level output voltage	$V_{\phi H}$	$I_{\phi H} = -1mA$	$V_H - 0.1$		$V_H$	V
"M" level output voltage	$V_{\phi M}$	$I_{\phi M} = -1mA$	$V_M - 0.1$		$V_M$	V
"L" level output voltage	$V_{\phi L}$	$I_{\phi L} = 1mA$	$V_L$		$V_L + 0.1$	V
Input current	$I_I$				1.0	$\mu A$
"H" level output ON resistance	$R_{on (H)}$	$I_{\phi H} = -50mA$		18	30	$\Omega$
"M" level output ON resistance	$R_{on (M)}$	$I_{\phi M} = -50mA$		18	30	$\Omega$
"L" level output ON resistance	$R_{on (L)}$	$I_{\phi L} = 50mA$		18	30	$\Omega$
Static current consumption	$I_{DD} + I_H + I_M$			$10^{-4}$	100	$\mu A$

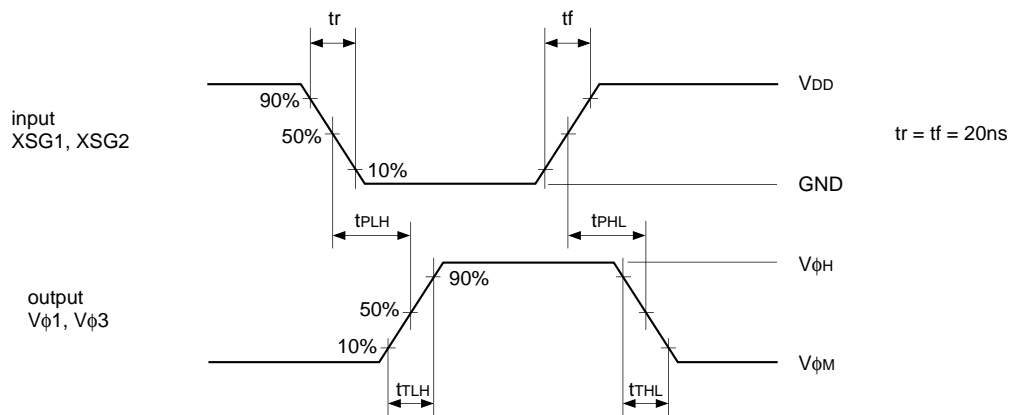
### 2. AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time L $\rightarrow$ M, M $\rightarrow$ L	$t_{PLH}$ , $t_{PHL}$	Waveform diagram (1), no load		100	200	ns
Propagation delay time M $\rightarrow$ H, H $\rightarrow$ M	$t_{PLH}$ , $t_{PHL}$	Waveform diagram (2), no load		200	400	ns
Rise time L $\rightarrow$ M Fall time M $\rightarrow$ L	$t_{TLH}$ , $t_{THL}$	Refer to waveform diagram (1), output load circuit diagram		200	300	ns
Rise time M $\rightarrow$ H Fall time H $\rightarrow$ M	$t_{TLH}$ , $t_{THL}$	Refer to waveform diagram (2), output load circuit diagram		200	300	ns
Operating current consumption	$I_{dyn}$ ( $I_{DD} + I_H + I_M + I_L$ )	Refer to input pulse timing diagram, output load circuit diagram		6.0	10.0	mA
	$I_{DD}$			0.02	0.2	mA
	$I_H + I_M$			3.8	5.0	mA
	$I_L$		-5.0	-3.8		mA

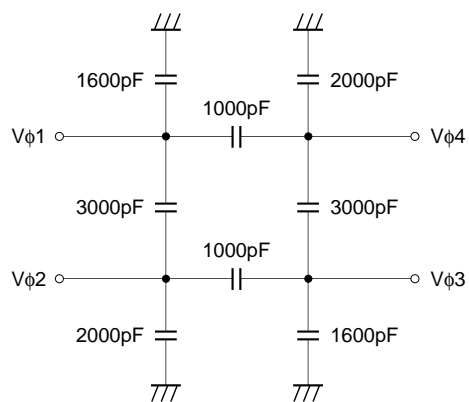
Waveform Diagram (1)



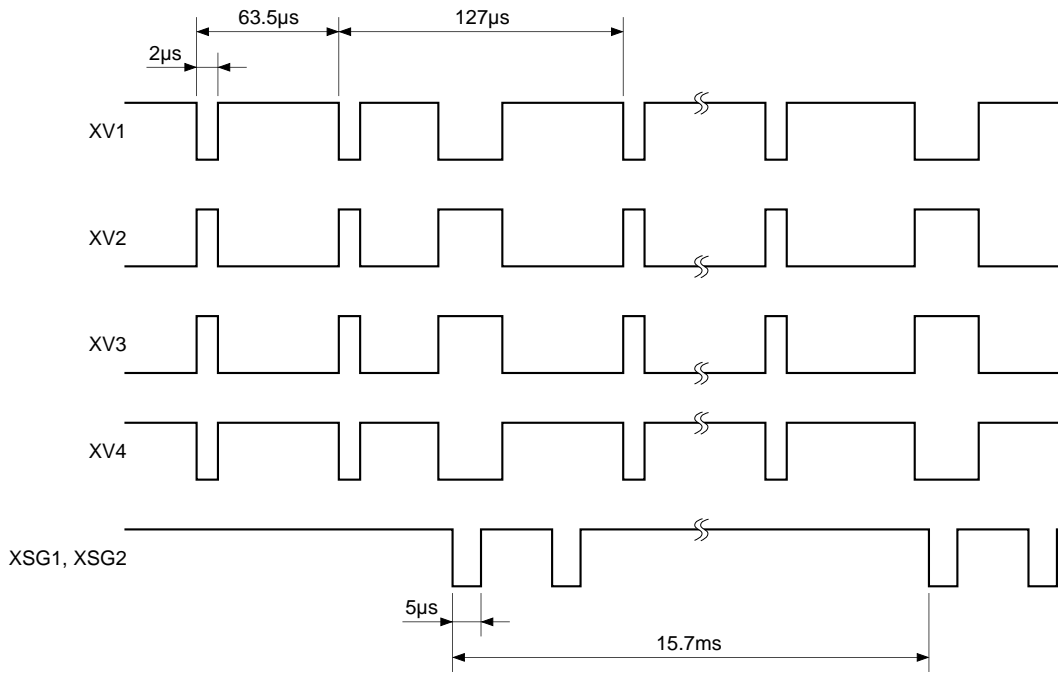
Waveform Diagram (2)



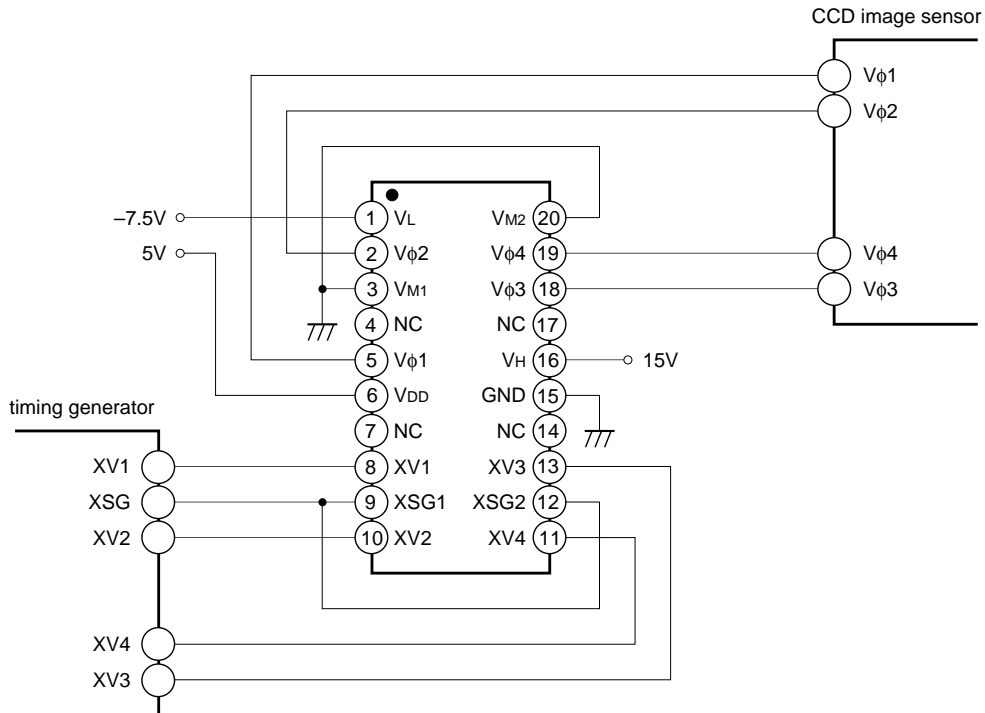
Output Load Circuit Diagram



**Input Pulse Timing Diagram**



**Application Circuit**



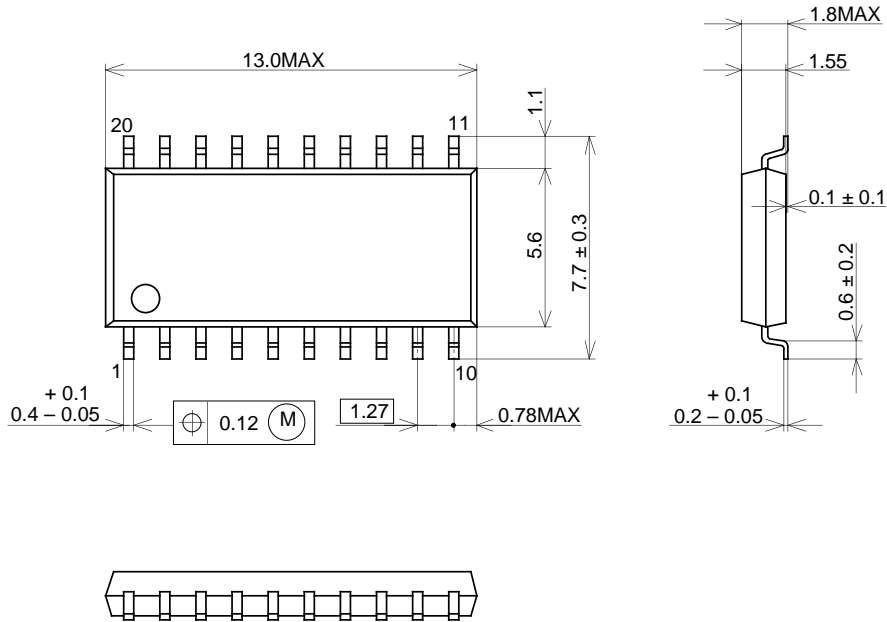
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**Notes on Operation**

1. When applying power, be sure to apply  $V_H$  before  $V_{DD}$  and  $V_M$ .
2. XSG1 (Pin 9) and XSG2 (Pin 12) can be input separately, although they are also common input.

Package Outline Unit: mm

20PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-20P-L071
EIAJ CODE	SOP020-P-0300
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.3g