# SONY

# CXD1196AR

## CD-ROM DECODER

### Description

The CXD1196AR is a CD-ROM decoder LSI with a built-in ADPCM decoder.

### Features

- CD-ROM, CD-I and CD-ROM XA format compatible
- Real time error correction
- Double speed playback compatible (when $V_{DD}$=5.0±10 %)
- Can be connected to a standard SRAM up to 32 Kbytes (256 Kbits).
- All audio output sampling frequency : 132.3 kHz (Built-in oversampling filter)
- Built-in de-emphasis digital filter
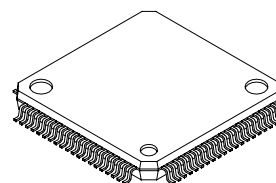- Capable of $V_{DD}$ 3.5 V operation

### Applications

CD-ROM drive

### Structure

Silicon gate CMOS IC

80 pin LQFP (Plastic)

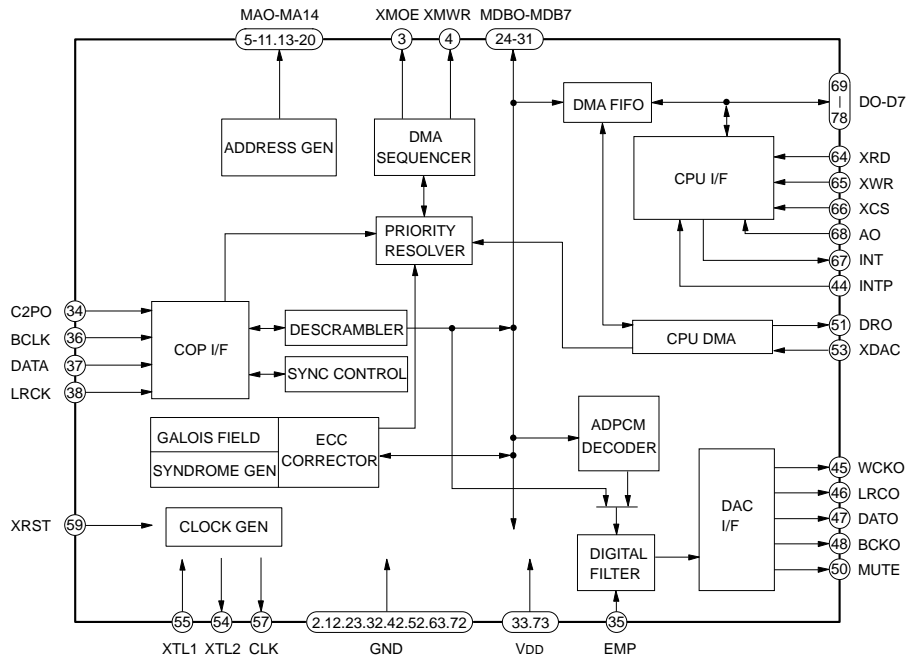### Absolute Maximum Ratings (Ta=25 °C)

- Supply voltage $V_{DD}$ $V_{SS}$ −0.5 to +7.0 V
- Input voltage $V_I$ $V_{SS}$ −0.5 to $V_{DD}$ +0.5 V
- Output voltage $V_O$ $V_{SS}$ −0.5 to $V_{DD}$ +0.5 V
- Operating temperature
  Topr −20 to +75 ℃
- Storage temperature
  Tstg −55 to +150 ℃

### Recommended Operating Conditions

- Supply voltage
  $V_{DD}$ +3.5 to +5.5 (+5.0 Typ.) V
- Operating temperature
  Topr −20 to +75 ℃

E92128B78-TE

## Block Diagram

MAO-MA14 (5-11.13-20) XMOE (3) XMWR (4) MDBO-MDB7 (24-31)

DMA FIFO — (69 | 78) DO-D7

ADDRESS GEN

DMA SEQUENCER

CPU I/F — (64) XRD — (65) XWR — (66) XCS — (68) AO — (67) INT — (44) INTP

PRIORITY RESOLVER

C2PO (34) BCLK (36) DATA (37) LRCK (38)

COP I/F

DESCRAMBLER

SYNC CONTROL

CPU DMA — (51) DRO — (53) XDAC

GALOIS FIELD / SYNDROME GEN — ECC CORRECTOR

ADPCM DECODER

XRST (59) CLOCK GEN

DIGITAL FILTER

DAC I/F — (45) WCKO — (46) LRCO — (47) DATO — (48) BCKO — (50) MUTE

(55) XTL1 (54) XTL2 (57) CLK — (2.12.23.32.42.52.63.72) GND — (33.73) VDD — (35) EMP

—2—

**Pin Description**

| No. | Symbol | I/O | Description |
|---|---|---|---|
| 1 | TD7 | I/O | Test pin |
| 2 | GND | — | Ground pin |
| 3 | XMOE | O | Buffer memory output enable negative logic signal |
| 4 | XMWR | O | Buffer memory write enable negative logic signal |
| 5 | MA0 | O | Buffer memory address (LSB) |
| 6 | MA1 | O | Buffer memory address |
| 7 | MA2 | O | Buffer memory address |
| 8 | MA3 | O | Buffer memory address |
| 9 | MA4 | O | Buffer memory address |
| 10 | MA5 | O | Buffer memory address |
| 11 | MA6 | O | Buffer memory address |
| 12 | GND | — | Ground pin |
| 13 | MA7 | O | Buffer memory address |
| 14 | MA8 | O | Buffer memory address |
| 15 | MA9 | O | Buffer memory address |
| 16 | MA10 | O | Buffer memory address |
| 17 | MA11 | O | Buffer memory address |
| 18 | MA12 | O | Buffer memory address |
| 19 | MA13 | O | Buffer memory address |
| 20 | MA14 | O | Buffer memory address (MSB) |
| 21 | TD6 | I/O | Test pin |
| 22 | TD5 | I/O | Test pin |
| 23 | GND | — | Ground pin |
| 24 | MDB0 | I/O | Buffer memory data bus (LSB) |
| 25 | MDB1 | I/O | Buffer memory data bus |
| 26 | MDB2 | I/O | Buffer memory data bus |
| 27 | MDB3 | I/O | Buffer memory data bus |
| 28 | MDB4 | I/O | Buffer memory data bus |
| 29 | MDB5 | I/O | Buffer memory data bus |
| 30 | MDB6 | I/O | Buffer memory data bus |
| 31 | MDB7 | I/O | Buffer memory data bus (MSB) |
| 32 | GND | — | Ground pin |
| 33 | $V_{DD}$ | — | Power supply pin |
| 34 | C2PO | I | C2 pointer positive logic signal from CD player |
| 35 | EMP | I | Emphasis positive logic signal from CD player |
| 36 | BCLK | I | Bit clock signal from CD player |
| 37 | DATA | I | Data signal from CD player |
| 38 | LRCK | I | LR clock signal from CD player |
| 39 | TD4 | I/O | Test pin |
| 40 | TD3 | I/O | Test pin |

| No. | Symbol | I/O | Description |
|---|---|---|---|
| 41 | TD2 | I/O | Test pin |
| 42 | GND | — | Ground pin |
| 43 | TD1 | I/O | Test pin |
| 44 | INTP | I | INT pin polarity control signal |
| 45 | WCKO | O | Word clock signal to DA converter |
| 46 | LRCO | O | LR clock signal to DA converter |
| 47 | DATO | O | Data signal to DA converter |
| 48 | BCKO | O | Bit clock signal to DA converter |
| 49 | N. C | — | |
| 50 | MUTE | O | Mute positive logic signal |
| 51 | DRQ | O | DMA request positive logic signal |
| 52 | GND | — | Ground pin |
| 53 | XDAC | I | Acknowledge negative logic signal for DRQ |
| 54 | XTL2 | O | Crystal oscillator circuit output pin |
| 55 | XTL1 | I | Crystal oscillator circuit input pin |
| 56 | TD0 | I/O | Test pin |
| 57 | CLK | O | Clock with 1/2 frequency of XTL1 |
| 58 | TDIO | I | Test pin |
| 59 | XRST | I | Chip reset negative logic signal |
| 60 | TA3 | I | Test pin |
| 61 | TA2 | I | Test pin |
| 62 | TA1 | I | Test pin |
| 63 | GND | — | Ground pin |
| 64 | XRD | I | CPU register read strobe negative logic signal |
| 65 | XWR | I | CPU register write strobe negative logic signal |
| 66 | XCS | I | Chip select negative logic signal from CPU |
| 67 | INT | O | Interrupt request signal to CPU |
| 68 | A0 | I | CPU address signal |
| 69 | D7 | I | CPU data bus (MSB) |
| 70 | D6 | I | CPU data bus |
| 71 | D5 | I | CPU data bus |
| 72 | GND | — | Ground pin |
| 73 | $V_{DD}$ | — | Power supply pin |
| 74 | D4 | I | CPU data bus |
| 75 | D3 | I | CPU data bus |
| 76 | D2 | I | CPU data bus |
| 77 | D1 | I | CPU data bus |
| 78 | D0 | I | CPU data bus (LSB) |
| 79 | TA0 | I | Test pin |
| 80 | N. C | — | |

## Electrical Characteristics

**DC characteristics** (V$_{DD}$=5 V±10 %, V$_{SS}$=0 V, Topr=−20 to 75 °C)

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| TTL input level pin (*1) input voltage H level | V$_{IH1}$ | | 2.2 | | | V |
| TTL input level pin (*1) input voltage L level | V$_{IL1}$ | | | | 0.8 | V |
| CMOS input level pin (*2) input voltage H level | V$_{IH2}$ | | 0.7 V$_{DD}$ | | | V |
| CMOS input level pin (*2) input voltage L level | V$_{IL2}$ | | | | 0.3 V$_{DD}$ | V |
| TTL schmitt input level pin (*3) input voltage H level | V$_{IH3}$ | | 2.2 | | | V |
| TTL schmitt input level pin (*3) input voltage L level | V$_{IL3}$ | | | | 0.8 | V |
| TTL schmitt input level pin (*3) input voltage hysteresis | V$_{IH3}$ −V$_{IL3}$ | | | 0.4 | | V |
| CMOS schmitt input level pin (*4) input voltage H level | V$_{IH4}$ | | 0.8 V$_{DD}$ | | | V |
| CMOS schmitt input level pin (*4) input voltage L level | V$_{IL4}$ | | | | 0.2 V$_{DD}$ | V |
| CMOS schmitt input level pin (*4) input voltage hysteresis | V$_{IH4}$ −V$_{IL4}$ | | | 0.6 | | V |
| Pull-up resistor provided input pin (*5) input current | I$_{IL1}$ | V$_{IN}$=0 V | −40 | −100 | −240 | µA |
| Pull-down resistor provided input pin (*6) input current | I$_{IL2}$ | V$_{IN}$=0 V | 40 | 100 | 240 | µA |
| Pull-up resistor provided bidirectional pin (*7) input current | I$_{IL3}$ | V$_{IN}$=0 V | −90 | −200 | −440 | µA |
| Output voltage H level (*8) | V$_{OH1}$ | V$_{OH}$=−2 mA | V$_{DD}$−0.8 | | | V |
| Output voltage L level (*8) | V$_{OL1}$ | I$_{OL}$=4 mA | | | 0.4 | V |
| Input leak current (*9) | I$_{IL2}$ | | −40 | | 40 | µA |
| Oscillation cell (*10) input voltage H level | V$_{IH4}$ | | 0.7 V$_{DD}$ | | | V |
| Oscillation cell input voltage L level | V$_{IL4}$ | | | | 0.3 V$_{DD}$ | V |
| Oscillation cell logic threshold value | LV$_{TH}$ | | | 0.5 V$_{DD}$ | | V |
| Oscillation cell feedback resistance value | R$_{FB}$ | V$_{IN}$=V$_{SS}$ or V$_{DD}$ | 500 K | 1 M | 2 M | Ω |
| Oscillation cell output voltage H level | V$_{OH2}$ | I$_{OH}$=−3 mA | 0.5 V$_{DD}$ | | | V |
| Oscillation cell output voltage L level | V$_{OL2}$ | I$_{OL}$=3 mA | | | 0.5 V$_{DD}$ | V |

## DC characteristics

(V$_{DD}$=3.5 V, V$_{SS}$=0 V, Topr=−20 to 75 °C)

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| TTL input level pin (*1) input voltage H level | V$_{IH1}$ | | 2.2 | | | V |
| TTL input level pin (*1) input voltage L level | V$_{IL1}$ | | | | 0.6 | V |
| CMOS input level pin (*2) input voltage H level | V$_{IH2}$ | | 0.7 V$_{DD}$ | | | V |
| CMOS input level pin (*2) input voltage L level | V$_{IL2}$ | | | | 0.3 V$_{DD}$ | V |
| TTL schmitt input level pin (*3) input voltage H level | V$_{IH3}$ | | 2.2 | | | V |
| TTL schmitt input level pin (*3) input voltage L level | V$_{IL3}$ | | | | 0.6 | V |
| TTL schmitt input level pin (*3) input voltage hysteresis | V$_{IH3}$ −V$_{IL3}$ | | | 0.3 | | V |
| CMOS schmitt input level pin (*4) input voltage H level | V$_{IH4}$ | | 0.8 V$_{DD}$ | | | V |
| CMOS schmitt input level pin (*4) input voltage L level | V$_{IL4}$ | | | | 0.2 V$_{DD}$ | V |
| CMOS schmitt input level pin (*4) input voltage hysteresis | V$_{IH4}$ −V$_{IL4}$ | | | 0.5 | | V |
| Pull-up resistor provided input pin (*5) input current | I$_{IL1}$ | V$_{IN}$=0 V | −10 | −25 | −60 | μA |
| Pull-down resistor provided input pin (*6) input current | I$_{IL2}$ | V$_{IN}$=0 V | 10 | 25 | 60 | μA |
| Pull-up resistor provided bidirectional pin (*7) input current | I$_{IL3}$ | V$_{IN}$=0 V | −20 | −50 | −110 | μA |
| Output voltage H level (*8) | V$_{OH1}$ | V$_{OH}$=−1.6 mA | V$_{DD}$−0.8 | | | V |
| Output voltage L level (*8) | V$_{OL1}$ | I$_{OL}$=3.2 mA | | | 0.4 | V |
| Input leak current (*9) | I$_{IL2}$ | | −40 | | 40 | μA |
| Oscillation cell (*10) input voltage H level | V$_{IH4}$ | | 0.7 V$_{DD}$ | | | V |
| Oscillation cell input voltage L level | V$_{IL4}$ | | | | 0.3 V$_{DD}$ | V |
| Oscillation cell threshold value | LV$_{TH}$ | | | 0.5 V$_{DD}$ | | V |
| Oscillation cell feedback resistance value | R$_{FB}$ | V$_{IN}$=V$_{SS}$ or V$_{DD}$ | 1.2 K | 2.5 M | 5 M | Ω |
| Oscillation cell output voltage H level | V$_{OH2}$ | I$_{OH}$=−1.3 mA | 0.5 V$_{DD}$ | | | V |
| Oscillation cell output voltage L level | V$_{OL2}$ | I$_{OL}$=1.3 mA | | | 0.5 V$_{DD}$ | V |

*1. D7 to 0, MDB7 to 0, TD7 to 0

*2. DATA, LRCK, C2PO, EMP, INTP, TDIO, TA3 to 0

*3. XWR, XRD, XCS, A0, XDAC

*4. BCLK, XRST

*5. XDAC, TA3 to 0

*6. C2PO, INTP

*7. D7 to 0, MDB7 to 0, TD7 to 0

*8. All output pins except XTL2

*9. All input pins except *7

*10. input : XTL1, output : XTL2

**Input/Output Capacitance** $(V_{DD}=V_I=0$ V, f=1 MHz)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input pin | $C_{IN}$ | | | 9 | pF |
| Output pin | $C_{OUT}$ | | | 11 | pF |
| Input/Output pin | $C_{OUT}$ | | | 11 | pF |

—7—

**AC Characteristics** (VDD=5 V±10 %, VSS=0 V, Topr=−20 to 75 °C, Output load=50 pF)

The values in parentheses in the table are those obtained when VDD=3.5 V, VSS=0 V, Topr=−20 to 75 °C, and output load=50 pF.

Values without parentheses are common to VDD=5 V±10 % and 3.5 V.

**1. CPU interface**

(1) Read
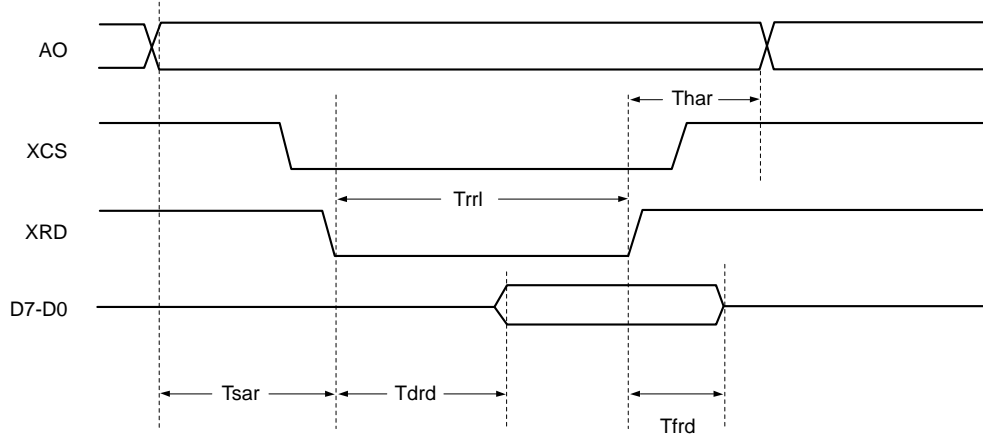


| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Address setting time (with respect to XCS & XRD ↓) | Tsar | 30 (70) | | | ns |
| Address holding time (with respect to XCS & XRD ↑) | Thar | 20 (50) | | | ns |
| Data delay time (with respect to XCS & XRD ↓) | Tdrd | | | 120 (200) | ns |
| Data float time (with respect to XCS & XRD ↑) | Tfrd | 0 | | 20 (40) | ns |
| L level XRD pulse width | Trr1 | 150 (250) | | | ns |

(2) Write
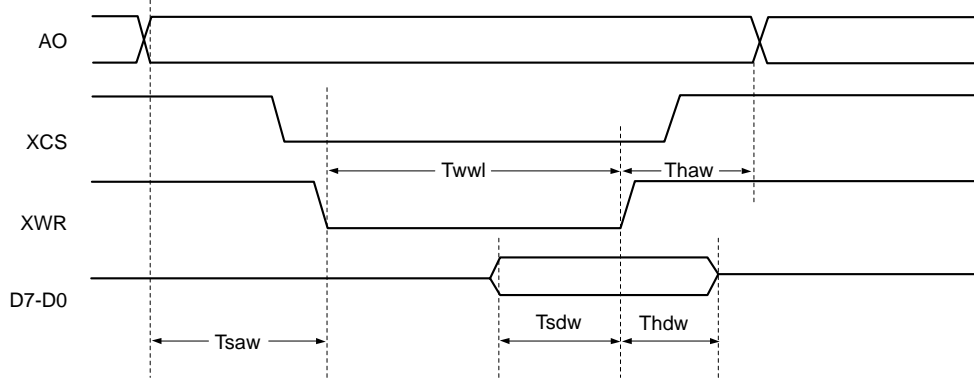


| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Address setting time (with respect to XCS & XWR ↓) | Tsaw | 30 (70) | | | ns |
| Address holding time (with respect to XCS & XWR ↑) | Thaw | 20 (50) | | | ns |
| Data setting time (with respect to XCS & XWR ↓) | Tsdw | 50 (70) | | | ns |
| Data holding time (with respect to XCS & XWR ↑) | Thwd | 20 (30) | | | ns |
| L level XWR pulse width | Twwl | 70 (100) | | | ns |

(3) DMA
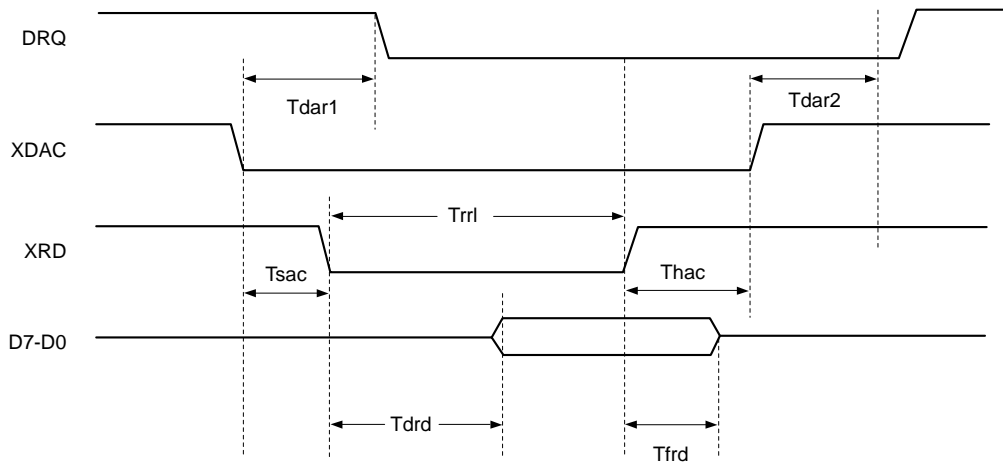


| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| DRQ fall time (with respect to XDAC ↓) | Tdar1 | | | 50 (120) | ns |
| DRQ rise time (with respect to XDAC ↑) | Tdar2 | | | 50 (120) | ns |
| XDAC setting time (with respect to XRD ↓) | Tsac | 10 (30) | | | ns |
| XDAC holding time (with respect to XRD ↑) | Thac | 10 (30) | | | ns |
| Data delay time (with respect to XRD ↓) | Tdrd | | | 120 (200) | ns |
| Data float time (with respect to XRD ↑) | Tfrd | 0 | | 20 (40) | ns |
| L level XRD pulse width | Trrl | 150 (250) | | | ns |

—9—

## 2. SRAM interface

### (1) Read
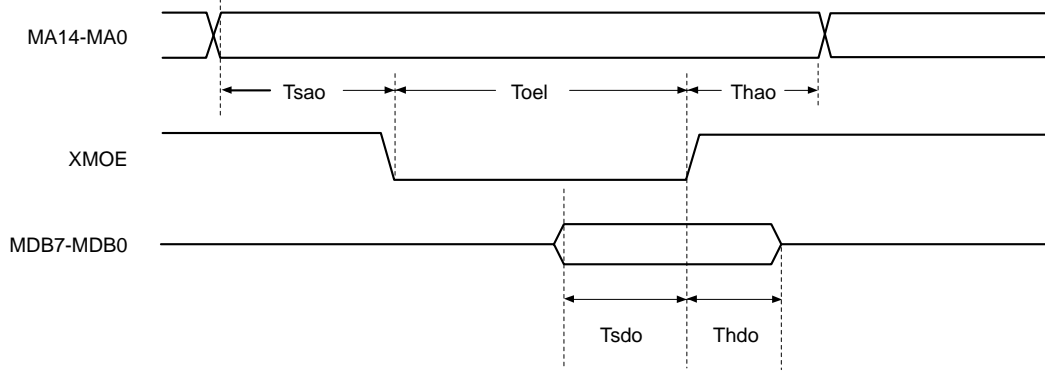


| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Address setting time (with respect to XMOE $\downarrow$) | Tsao | $T_1-30$ | | | ns |
| Address holding time (with respect to XMOE $\uparrow$) | Thao | $T_1-10$ | | | ns |
| Data setting time (with respect to XMOE $\uparrow$) | Tsdo | 50 (100) | | | ns |
| Data holding time (with respect to XMOE $\uparrow$) | Thdo | 10 (20) | | | ns |
| L level XMOE pulse width | Toel | | $2 \cdot T_1$ | | ns |

### (2) Write
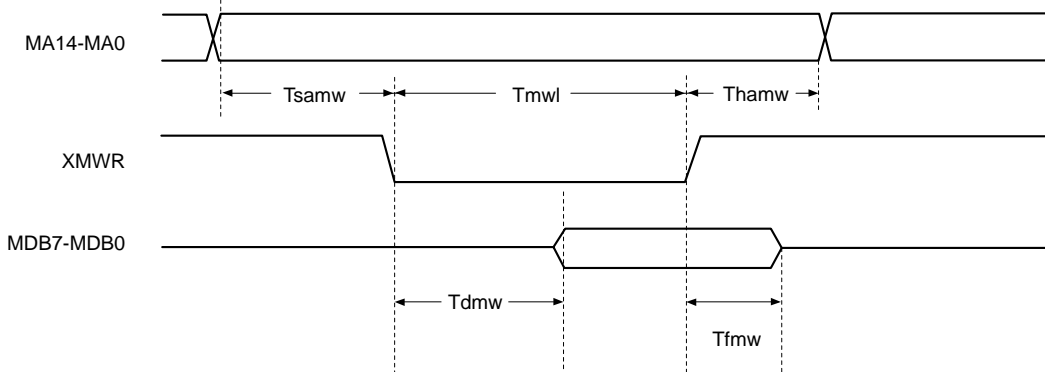


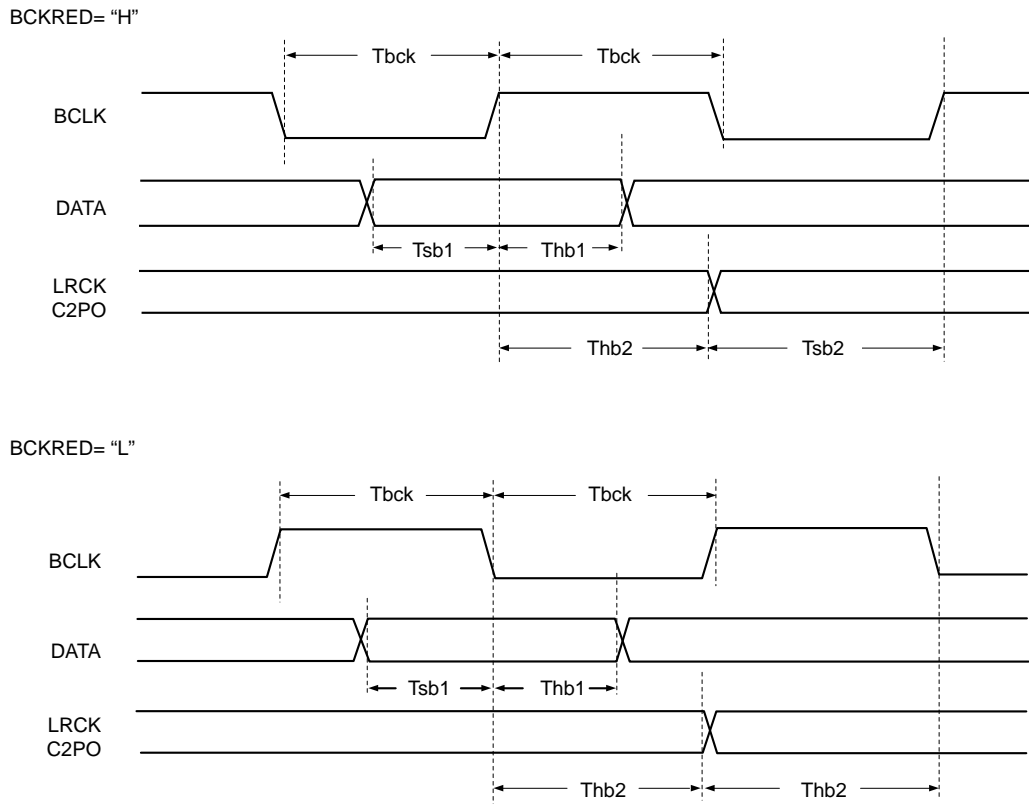| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Address setting time (with respect to XMWR $\downarrow$) | Tsamw | $T_1-30$ | | | ns |
| Address holding time (with respect to XMWR $\uparrow$) | Thamw | $T_1-10$ | | | ns |
| Data delay time (with respect to XMWR $\downarrow$) | Tdmw | | | 0 | ns |
| Data float time (with respect to XMWR $\uparrow$) | Tfmw | 10 | | | ns |
| L level XMWR pulse width | Tmwl | | $2 \cdot T_1$ | | ns |

$$T_1 = \begin{cases} 59 \text{ ns :} & \text{XSLOW = 'H'} \\ 238 \text{ ns :} & \text{XSLOW = 'L'} \end{cases}$$

Note that XSLOW is bit 7 of DRVIF register.

When XSLOW = 'H' , make sure that the CXD1196AR is connected to an SRAM with an access time of less than 120 ns.

When XSLOW = 'L' , make sure that the CXD1196AR is connected to an SRAM with an access time of less than 320 ns.

—10—

## 3. DSP Interface for CD

BCKRED= "H"



BCKRED= "L"



| Item | Symbol | Min. | Typ. | Max. | Unit |
|------|--------|------|------|------|------|
| BCLK frequency | Fbck | | | 5.7 | MHz |
| BCLK pulse width | Tbck | 85 | | | ns |
| Data setting time (with respect to BCLK) | Tsb1 | 50 | | | ns |
| Data holding time (with respect to BCLK) | Thb1 | 50 | | | ns |
| LRCK, C2PO setting time (with respect to BCLK) | Tsb2 | 50 | | | ns |
| LRCK, C2PO holding time (with respect to BCLK) | Thb2 | 50 | | | ns |

—11—

### 4. DAC interface
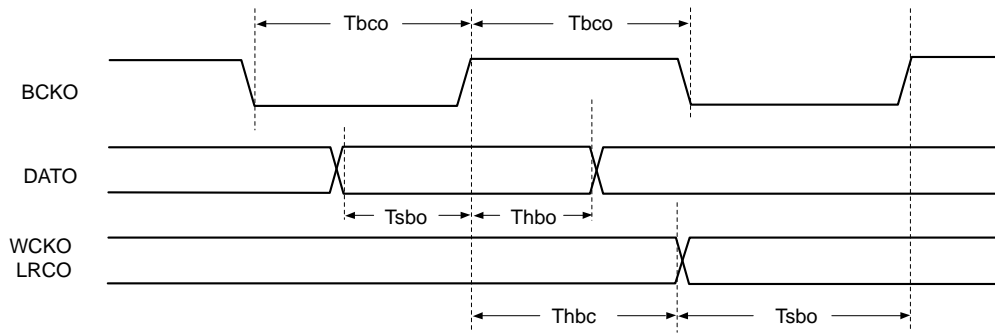


| Item | Symbol | Min. | Typ. | Max. | Unit |
|------|--------|------|------|------|------|
| BCKO frequency | Fbco | | 8.4672 | | MHz |
| BCKO pulse width | Tbco | 50 | | | ns |
| DATO, WCKO, LRCO setting time (with respect to BCKO ↑) | Tsbo | 30 | | | ns |
| DATO, WCKO, LRCO holding time (with respect to BCKO ↑) | Thbo | 30 | | | ns |

—12—

## 5. XTL1 pin, XTL2 pins

(1) Self-excited oscillation

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Oscillation frequency | Fmax | | 16.9344 | | MHz |

(2) When pulses are to be input to XTL1 pin
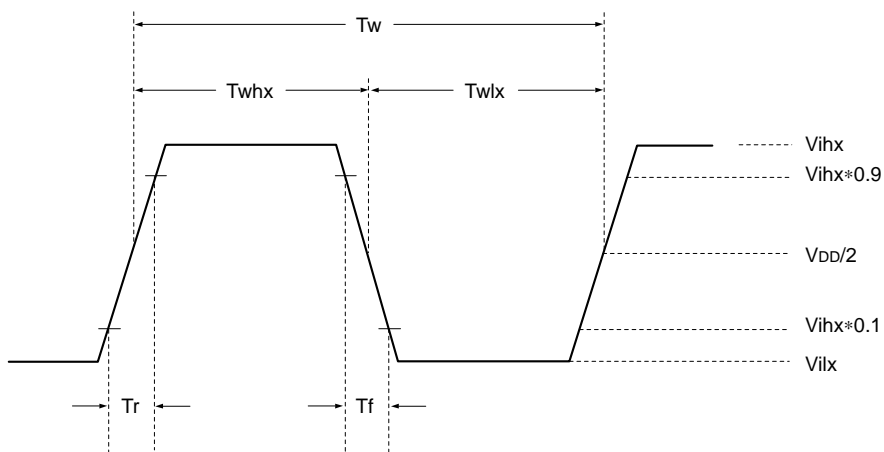


| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| H level pulse width | Twhx | 20 | | | ns |
| L level pulse width | Twlx | 20 | | | ns |
| Pulse interval | Tw | | 59 | | ns |
| Input H level | Vihx | $V_{DD}$–1.0 | | | V |
| Input L level | Vilx | | | 0.8 | V |
| Rise time | Tr | | | 15 | ns |
| Fall time | Tf | | | 15 | ns |

**Note)** Synchronize XTL1 clock with DSP clock for CD.

(Use the clock generated from the same oscillator unit.)

—13—

**Description of Functions**

**1.  Description of Pins**

1.1   CD player interface
The CXD1196AR can be directly connected to digital signal processing LSIs for CD of Sony and other company.  The digital signal processing LSI for CD is referred to as a DSP for CD.
(1)  DATA (DATA : Input)
Serial data stream from a CIRC LSI
(2)  BCLK (Bit Clock : Input)
Bit clock signal for strobing DATA signal
(3)  LRCK (LR Clock : Input)
LR clock signal indicating Lch and Rch of DATA signal
(4)  C2PO (C2 Pointer : Input)
C2 pointer signal indicating that DATA input contains an error
(5)  EMP (Emphasis : Input)
Emphasis indicating that the data from the DSP is emphasized.  (positive logic signal)

1.2   Buffer memory interface
The CXD1196AR can be connected to a standard SRAM up to 32 Kbytes (256 Kbits).
(1)  XMWR (BUFFER MEMORY WRITE : OUT)
Data write signal to buffer memory (strobe negative logic output)
(2)  XMOE (BUFFER MEMORY OUTPUT ENABLE : OUT)
Data read signal to buffer memory (strobe negative logic output)
(3)  MA0-14 (BUFFER MEMORY ADDRESS : OUT)
Address signals to buffer memory
(4)  MDB0-7 (BUFFER MEMORY DATA BUS : BUS)
Buffer memory data bus signal pulled up by a typical 25 k$\Omega$ resistor

In an ADPCM decode playback drive, make sure that the CXD1196AR is connected to a 256 Kbit ($8^b \times$ 32 K$^w$, 32 Kbyte) SRAM

1.3   CPU interface

(1)  XWR (CPU WRITE : Input)
Strobe signal for writing to register in chip (negative logic input)
(2)  XRD (CPU READ : Input)
Strobe for reading out status of register chip (negative logic input signal)
(3)  D0-7 (CPU DATA BUS : Input and output)
8-bit data bus
(4)  A0 (CPU ADDRESS : Input)
CPU address signal for selecting internal register of the CXD1196AR
(5)  INT (CPU INTERRUPT : Output)
Interrupt request output signal for CPU.  The polarity of this signal can be controlled by the INTP pin.
(6)  INTP (INTERRUPT POLARITY : Input)
This pin controls the polarity of the INT pin.  In the IC, it is pulled up by a typical 50 k$\Omega$ register.
When INTP= 'H' or open, the INT pin goes low active.
When INTP= 'L' , the INT pin goes high active.
(7)  XCS (CHIP SELECT : Input)
Chip select signal for CPU to select the CXD1196AR (negative logic input)

—14—

(8) DRQ (DATA REQUEST : Output)
  DMA data request signal (positive logic output)
(9) XDAC (DATA ACKNOWLEDGE : Input)
  The acknowledge signal for DRQ (negative logic input).  In the IC, it is pulled up by a typical 50 kΩ
  resistor.

1.4   DAC interface
  (1) BCKO (BIT CLOCK OUTPUT : Output)
    Bit clock output signal to DA converter
  (2) WCKO (WORD CLOCK OUTPUT : Output)
    Word clock output signal to DA converter
  (3) LRCO (LR CLOCK OUTPUT : Output)
    LR clock output signal to DA converter
  (4) DATO (DATA OUTPUT : Output)
    Data output signal to DA converter

    Fig. 1.1 shows a timing chart for interface with the DA converter.

1.5   Miscellaneous
  (1) MUTE (MUTE : Output)
    Output H when DA data is muted
  (2) XRST (RESET : Input)
    Chip reset signal (negative logic input)
  (3) XTL1 (X'TAI1 : Input)
  (4) XTL2 (X'TAI2 : Output)
    Connect a 16.9344 MHz crystal oscillator unit between XTL1 and XTL2.  (The value of the capacitor
    depends on the crystal oscillator unit.)  Or input 16.9344 MHz clock to the XTL1 pin.  For ADPCM or
    CD-DA playback, the clocks of the DSP for CD and this IC must be synchronized.
  (5) CLK (CLOCK : Output)
    Output 8.4672 clock.
    When this clock is not be used, the output of the CLK pin may be fixed at 'L'.

1.6   Test pins
  These pins are normally kept in the opened state.
  (1) TD0-7 (Input/Output) : Data bus for IC test.  Pulled up by a typical 25 kΩ resistor.
  (2) TDIO (Input) : Input pin for IC test.  Pulled up by a typical 50 kΩ resistor.
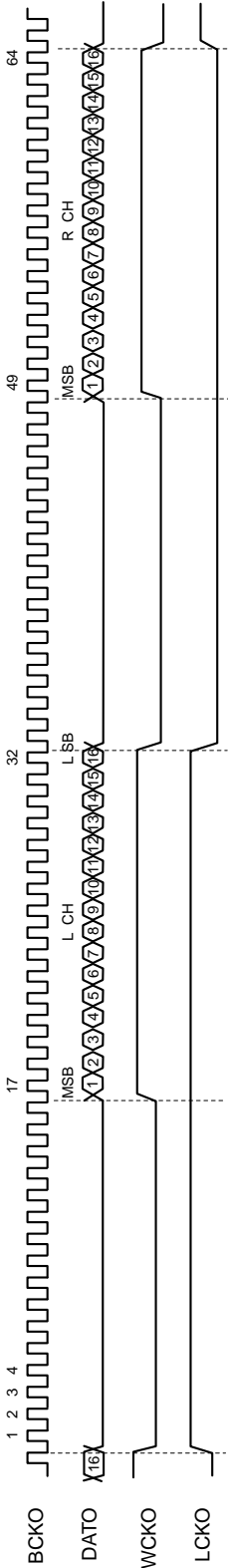  (3) TA0-3 (Input) : Input pins for IC test.  Pulled up by a typical 50 kΩ resistor.

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CXD1196AR

**Fig. 1.1  Output Format to DA Converter**

—16—

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## 2. Register Functions

### 2.1 Write register

#### 2.1.1 Register address (REGADR) register
This register is used for selection of the internal registers.
(1) When A0 = XCS = 'L', the REGADR register is selected. When A0 = 'H' and XCS = 'L', the register specified by the REGADR is selected.
(2) When the low order 4 bits of REGADR are not 0 (hex), and a register write or read is made by setting A0 = 'H' and XCS = 'L', the low order 4 bits of REGADR are incremented.
(3) REGADR is cleared by rising edge of DMAEN bit (bit3) of the DMACTL register. (Cleared to 00 (hex).)

#### 2.1.2 DRIVE Interface (DRVIF) register
Bit7   XSLOW (/SLOW SPEED)
     'H'   :   A DMA cycle is performed in 4 clocks.
                In this case, a standard SRAM with an access time of less than 120 nsec can be connected to the CXD1196AR.
     'L'   :   A DMA cycle is performed in 12 clocks. When the CXD1196R is connected to an SRAM with a slower access time, set this bit at 'L'. In this case, a standard SRAM with an access time of less than 320 ns can be connected to the CXD1196AR. For operation at $V_{DD}$ = 3.5 V, set this bit to L.

Bit6   C2PL1ST (C2PO Ler-byte 1st)
     'H'   :   To input two bytes of DATA input, each with a C2PO identifying the lower or upper byte, in the order of the lower and upper bytes
     'L'   :   To input two bytes of DATA input, each with a C2PO identifying the upper or lower byte, in the order of the upper and lower bytes.
Here, the upper byte means the 8 (eight) upper bits including the MSB from the DSP for CD. And the lower byte means the 8 (eight) lower bits including the LSB from the DSP for CD. For example, the minute byte of the Header is a lower byte and the sec byte is a upper byte.

Bit5   LCHLOW (LCH LOW)
     'H'   :   To determine that the data is Lch data when LRCK = 'L'
     'L'   :   To determine that the data is Lch data when LRCK = 'H'

Bit4   BCKRED (BCLK Rising Edge)
     'H'   :   To strobe DATA by the rising edge of BCLK
     'L'   :   To strobe DATA by the falling edge of BCLK

Bit3, 2   BCKMD1, 0 (BCLK Mode 1, 0)
Set these bits, depending on the number of BCLK clocks output by the DSP for CD during a cycle of WCLK.

| BCKMD1 | BCKMD0 | |
|--------|--------|--------------|
| 'L' | 'L' | 16BCLKs/WCLK |
| 'L' | 'H' | 24BCLKs/WCLK |
| 'H' | 'X' | 32BCLKs/WCLK |

Bit1   LSB 1ST (LSB First)
     'H'   :   To connect to a DSP for CD which outputs DATA on an LSB first basis
     'L'   :   To connect to a DSP for CD which outputs DATA on an MSB first basis

Bit0   CLKLOW (CLK LOW)
     'H'   :   To fix CLK pin output at 'L'
     'L'   :   To output 8.4672 MHz clock from CLK pin output
The values of the individual bits of this register must be changed with the decoder in the disabled state. Table 2.1.1 shows the values of bits of bit 6 through 1 to be set when the CXD1196AR is connected to Sony DSPs for CD. Fig. 2.2.1 (1) through (3) show input timing charts.

| Sony DSP for CD | DRVIF register | | | | | | Timing chart |
|---|---|---|---|---|---|---|---|
| | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | |
| CDL30 series<br>CDL35 series | L | L | L | L | H | L | Fig. 2.1.1 (1) |
| CDL40 series<br>(48-bit slot mode) | L | L | H | L | H | L | Fig. 2.1.1 (2) |
| CDL40 series<br>(64-bit slot mode) | L | H | L | H | X | H | Fig. 2.1.1 (3) |

**Table 2.1.1   DRVIF Register Settings**

**(Note 1)**

| CDL30 series | CXD1125Q/QZ, CXD1130Q/QZ, CXD1135Q/QZ, CXD1241Q/QZ, CXD1245Q, CXD1246Q/QZ, CXD1247Q/QZ/R, etc. |
|---|---|
| CDL35 series | CXD1165Q, CXD1167Q/QZ/R, etc. |
| CDL40 series | CXD2500Q/QZ, etc. |

2.1.3   Chip Control (CHPCTL) register

Bit7-5   RESERVED

Bit4   CHPRST (Chip Reset)

When this bit is set at 'H', the CXD1196AR is internally initialized.  The bit setting will automatically change to 'L' when the internal initialization of the CXD1196AR is completed.  Therefore, there is no need for the CPU to change the setting at 'L'.  Initialization of the CXD1196AR will be completed in 500ns after the bit has been set at 'H' by the CPU.

Bit3   CD-DA (CD-Digital Audio)

'H'   :   When a CD-DA disc is to be played back, this bit is set at 'H'.
The decoder must be placed in the disabled state (DECCTL register) when this bit is set at 'H'.

'L'   :   When a CD-ROM disc is to be played back, this bit is set at 'L'.

Bit2   SWOPN (Sync Window Open)

'H'   :   When this bit is set at 'H', the window for detection of SYNC mark will open.  In this case, the SYNC protection circuit in the CXD1196AR will be disabled.

'L'   :   When this bit is set at 'L', the window for detection of SYNC mark will be controlled by the SYNC protection circuit in the CXD1196AR.

Bit1   RPSTART (Repeat Correction Start)

When the DECODER is placed in the repeat correction mode, and this bit set at 'H', the error correction of the current sector will begin.  The bit setting will automatically change to 'L' when correction begins.  Therefore, there is no need for the CPU to change the setting at 'L'.

Bit0   ADPEN (ADPCM Enable)

When the current sector is an ADPCM sector, the CPU sets this bit at 'H' in less than 11.5 ms after a decoder interrupt (DECINT).  When the current sector is not an ADPCM sector, the CPU changes the bit setting at 'L' in less than 11.5 ms after a decoder interrupt (DECINT).

—18—

2.1.4   DECODER CONTROL (DECCTL) Register
   Bit7   AUTOCI (Auto Coding Information)
         'H'   :   To perform ADPCM playback according to the coding information from the drive.   In this
                  case, the CI register need not be set.
         'L'   :   To perform ADPCM playback according to the value of the CI register.
   Bit6   RESERVED
         Should be kept at 'L' at all times.
   Bit5   MODESEL (Mode Select)
   Bit4   FORMSEL (Form Select)
         When AUTODIST = 'L', the sector is corrected as the following MODE and FORM.

| MODESEL | FORMSEL | |
|---------|---------|----------------|
| 'L' | 'L' | MODE1 |
| 'H' | 'L' | MODE2, FORM1 |
| 'H' | 'L' | MODE2, FORM2 |

   Bit3   AUTODIST (Auto Distinction)
         'H'   :   Errors are corrected according to the MODE byte and FORM bit read from the drive.
         'L'   :   Errors are corrected according to bit 5 MODESEL and bit4 FORMSEL.

   Bit2-0   :   DECMD 2-0 (Decoder Mode 2-0)

| DECMD2 | DECMD1 | DECMD0 | |
|--------|--------|--------|----------------------------|
| 'L' | 'L' | 'X' | Decoder disable |
| 'L' | 'H' | 'X' | Monitor only mode |
| 'H' | 'L' | 'L' | Write only mode |
| 'H' | 'L' | 'H' | Real time correction mode |
| 'H' | 'H' | 'L' | Repeat correction mode |
| 'H' | 'H' | 'H' | Inhibit |

   These bits are set at 'L' when the CDDA bit (bit3) of the CHPCTL register is 'H'.

2.1.5   Interrupt Mask (INTMSK) Register
   When the individual bits of this register are set at 'H', an interrupt request from the CXD1196AR to the CPU
   is enabled in response to the corresponding interrupt status.  (That is, when the interrupt status is created,
   the INT pin is made active.)   The value of the individual bits of the register does not affect the
   corresponding interrupt status.

   Bit7   ADPEND (ADPCM End)
         When this chip has completed the ADPCM decode for a sector, if the ADPCM decode for the next
         sector is not enabled, the ADPEND status is created.
   Bit6   DECTOUT (Decoder Time Out)
         If no SYNC mark is detected during a period of 3 sectors (40.6 ms in normal speed playback mode)
         after the DECODER has been set in the monitor only, and real time correction modes, the DECTOUT
         status is created.
   Bit5   DMACMP (DMA Complete)
         When DMA is ended by DMAXFRC, the DMACMP status is created.

Bit4   DECINT (Decoder Interrupt)

If a SYNC mark is detected or internally inserted during execution of the write only, monitor only and real time correction modes by the DECODER, the DECINT status is created.  When the SYNC mark detected window is open, however, if the SYNC mark spacing is less than 2352 bytes, the DECINT status is not created.  During execution of the repeat correction mode by the DECODER, the DECINT status is created each time a correction ends.

Bit3   CIERR (Coding Information Error)

When AUTOCI bit of DECCTL register is set at "H" and ADPCM decode playback is done, if there is an error in a CI byte of an ADPCM sector, the CIERR status is created.  ADPCM decode playback of this sector will not be done.

Bit2-0   RESERVED

### 2.1.6   Clear Interrupt Status (INCTCLR) Register

When the individual bit of this register is set at 'H', the corresponding interrupt status is cleared.  The individual bit is automatically set at 'L' after the interrupt status has been cleared.  Therefore, there is no need for the CPU to change the setting at 'L'.

Bit7   ADPEND (ADPCM End)

Bit6   DECTOUT (DECODER Time Out)

Bit5   DMACMP (DMA Complete)

Bit4   DECINT (DECODER Interrupt)

Bit3   CIERR (Coding Information Error)

Bit2-0   RESERVED

### 2.1.7   Coding Information (CI) Register

When ADPCM decoding is to be done by setting AUTOCI = 'L', the coding information is written to this register.  The bit configuration is the same as that of the coding information byte of the sub header.

### 2.1.8   DMA Address Counter-L (DMAADRC-L)

### 2.1.9   DMA Address Counter-H (DMAADRC-H)

This counter retains the address to be used by the CPU when reading data from the buffer.  When the data to be sent to the CPU is read from the buffer, the contents of the DMAADRC are output from MA0-14.  Each time data to be sent to the CPU is read from the buffer, the DMAADRC is incremented.

The CPU sets the head address of DMA in the DMAADRC before starting DMA.  The CPU can read and set the contents of the DMAADRC at any time.  Do not change the contents of the DMAADRC during execution of DMA.

2.1.10  DMAXFRC-L

2.1.11  DMA Control (DMACTL) register
   Bit7    DMAXFRC11
           Bit11 (MSB) of DMAXFRC (Transfer Counter)
   Bit6    DMAXFRC10
           bit10 of DMAXFRC
   Bit5    DMAXFRC9
           bit9 of DMAXFRC
   Bit4    DMAXFRC8
           bit8 of DMAXFRC
   Bit3    DMAEN (CPU DMA Enable)
           'H'    :    To enable DMA
           'L'    :    To inhibit DMA
   Bit2-0  RESERVED

The DMAXFRC (DMA Transfer Counter) is a counter which indicates the number of DMA transfers.  Each time the data to be transferred to the CPU is read from the buffer, the counter is decremented.  When the value of the DMAXFRC reaches 0, DMA ends.  At this point, interrupt request may be output to the CPU. When data transfer is not to be ended by DMAXFRC as in the case of data transfer in the I/O mode, DMAXFRC should be set at 0 when data transfer is started (when DMAEN bit is set at 'H').  The CPU can read and set the contents of DMAXFRC at any time.  During execution of DMA, do not change the contents of DMAXFRC.

2.1.12  DRVADRC-L (Drive Address Counter-L)

2.1.13  DRVADRC-H
The DRVADRC is a counter which retains the address for writing the data from the drive to the buffer. When the drive data is written to the buffer, the value of DRVADRC is output from MA01-14 pins.  Each time a byte of data from the drive is written to the buffer, the DRVADRC is incremented.
Before execution of the write only mode and real time correction mode of the DECODER, the CPU sets the buffer write head address in the DRVADRC.
The CPU can read and set the contents of DRVADRC at any time.  During execution of DMA, do not change the contents of DRVADRC.
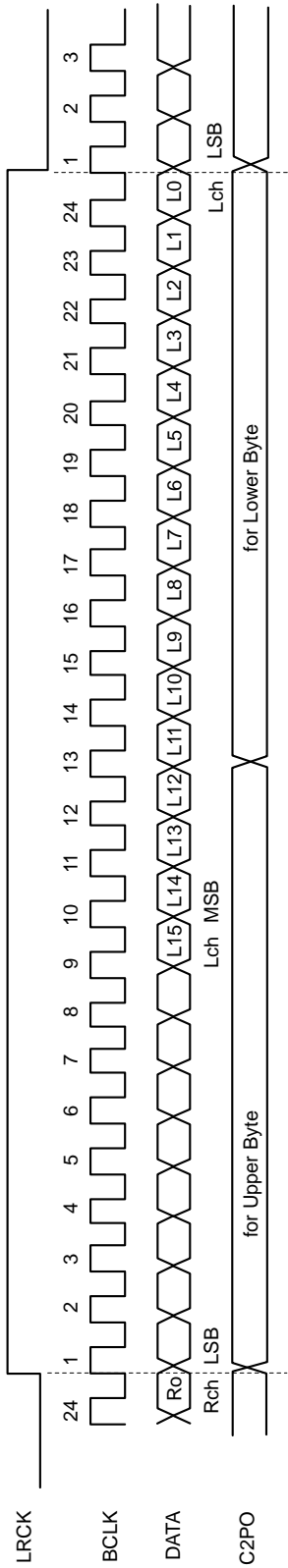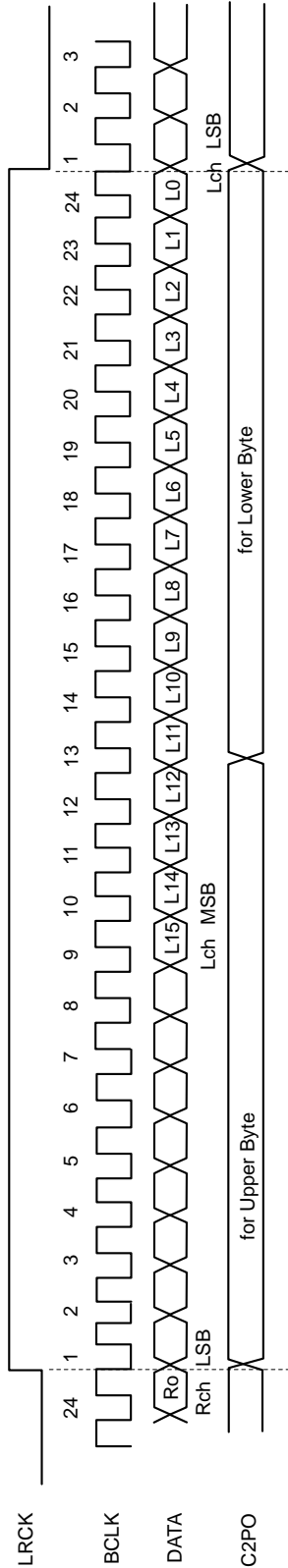
**Fig. 2.1.1 (1)  CDL30 and 35 Series Timing Chart**

**Fig. 2.1.1 (2)  CDL40 Series 48-Bit Slot Mode Timing Chart**
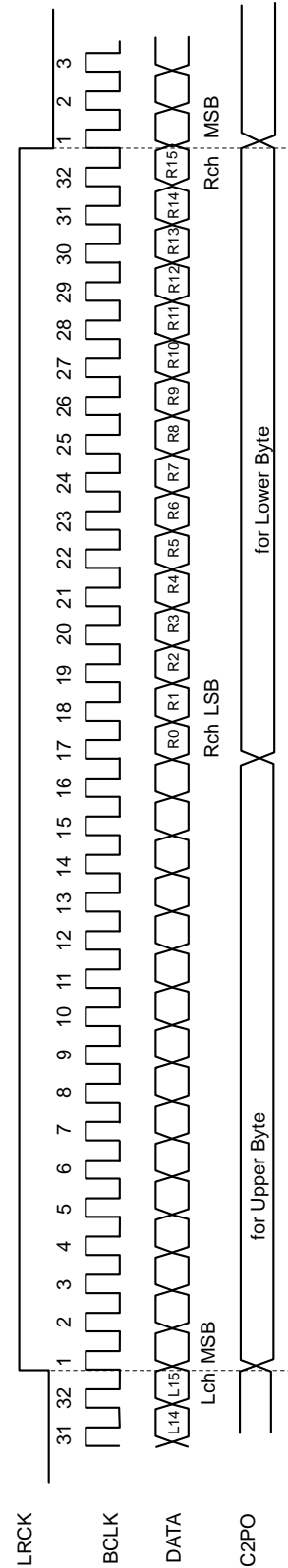
**Fig. 2.1.1 (3)  CDL40 Series 64-Bit Slot Mode Timing Chart**

—22—

2.2   Read register
In the descriptions of the registers STS, HDRFLG, HDR, SHDR and CMADR, what is referred to as the current sector refers to the sector where registers are valid for a decoder interrupt (DECINT).  In the monitor only and write only modes, the sector from the DSP for CD just before a decoder interrupt is called the current sector.   In the real time correction mode and repeat correction mode, the sector that has gone through error detection and correction is referred to as the current sector.

2.2.1   Register Address (REGADR) Register

2.2.2   DMADATA Register
When data transfer (buffer read) is to be made in the I/O mode, the CPU reads data from this register.

2.2.3   Interrupt Status (INTSTS) Register
The values of the individual bits of this register indicate the respective associated values of interrupt status.  These bits are not affected by the values of the individual bits of the INTMSK register.
Bit7   ADPEND (ADPCM End)
Bit6   DECTOUT (DECODER Time Out)
Bit5   DMACMP (DMA Complete)
Bit4   DECINT (DECODER Interrupt)
Bit3   CIERR (Coding Information Error)

2.2.4   Status (STS) Register
Bit7   DRQ (Data Request)
       This bit indicates the value of the DRQ pin.
Bit6   ADPBSY (ADPCM BUSY)
       This bit goes 'H' during ADPCM playback.
Bit5   ERINBLK (Erasure in Block)
       On all the bytes of the current sector except the SYNC byte, this bit goes 'H' if there is one or more bytes from the DSP for CD whose C2 pointer is ON.
Bit4   CORINH (Correction Inhibit)
       When the DECCTL register is set AUTODIST bit = 'H', this bit goes 'H' if the error flag is ON in the MODE (and FORM) byte.
Bit3   EDCOK
       Indicates EDC check showed there were no errors in the current sector.
Bit2   ECCOK
       Indicates there are no more errors from the Header to P parity bytes in the current sector. (In the MODE2, FORM2 sector, this bit is treated as a DON'T CARE bit.)
Bit1   SHRTSCT (Short Sector)
       Indicates the Sync Mark interval was less than 2351 bytes.  On this sector, neither ECC nor EDC is executed.
Bit0   NOSYNC
       Indicates that the SYNC Mark, not detected in the predetermined position, is one internally inserted.

2.2.5   Header Flag (HDRFLG) Register
Indicates the value of the error pointer of the Header and Sub Header registers.

—23—

### 2.2.6　Header (HDR) Register

It is a 4-byte register indicating the Header byte of the current sector.  The CPU can find the value of the Header byte of the current sector from the Minute byte as it sets the REGADR register at X4 hex and successively reads data.

### 2.2.7　Sub Header (SHDR) Register

It is a 4-byte register indicating the Sub Header byte of the current sector.  The CPU can find the value of the Sub Header byte of the current sector from the File byte as it sets the REGADR register at 08 hex and successively reads data.

### 2.2.8　Current Minute Address L (CMADR-L) Register

### 2.2.9　Current Minute Address H (CMADR-H) Register

Indicates the buffer memory address where the Minute bytes of the current sector (after correction) is in store.

### 2.2.10　MODE/FORM (MDFM) Register

Bit4-2　RMODE2-0

RMODE2 : Indicates the logic sum of the value of the high-order 6 bits of the raw MODE byte and the pointer.

RMODE1, 0 : Respectively indicate the values of the low-order 2 bits of the raw MODE byte.

Bit1　CMODE (Correction Mode)

Bit0　CFORM (Correction Form)

These bits indicate which of the MODEs and FORMs this IC determined that the current sector was associated with when it corrected errors.

| CFORM | CMODE | |
|-------|-------|------|
| 'X' | 'L' | MODE1 |
| 'L' | 'H' | MODE2, FORM1 |
| 'H' | 'H' | MODE2, FORM2 |

### 2.2.11　ADPCI (ADPCM Coding Information) Register

Bit7　MUTE

This bit goes 'H' when the DA data is muted on.

Bit6　EMPHASIS

This bit goes 'H' when the ADPCM data is emphasized.

Bit5　EOR (End of Record)

This bit goes 'H' when the Sub Mode byte bit0 = 'H' and there is no error in the Sub Mode byte.

Bit4　BITLNGTH (Bit Length)

This bit indicates the bit length of ADPCM playback coding information.

'H'　:　8 bits

'L'　:　4 bits

Bit2　FS (Sampling Frequency)

This bit indicates the ADPCM playback sampling frequency.

'H'　:　18.9 kHz

'L'　:　37.8 kHz

Bit0　M/S (MONO/STEREO)

This bit indicates "monaural" or "stereo" of ADPCM playback coding information.

'H'　:　Stereo

'L'　:　Monaural

—24—

2.2.12 DMAXFRC-L

2.2.13 DMAXFRC-H

2.2.14 DMAADRC-H

2.2.15 DMAADRC-H

2.2.16 DRVADRC-L

2.2.17 DRVADRC-H

| REG | A0 | RA | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|---|---|---|
| REGADR | L | X | L | L | L | RA4 | RA3 | RA2 | RA1 | RA0 |
| RESERVED | H | X0 | L | L | L | L | L | L | L | L |
| DRVIF | H | X1 | XSLOW | C2POL1st | LCHLOW | BCKRED | BCKMD1 | BCKMD0 | LSB1st | CLKL |
| CHPCTL | H | X2 | L | L | CLRADP | CHPRST | CD-DA | SWOPEN | RPSTART | ADPEN |
| DECCTL | H | X3 | AUTOCI | L | MODESEL | FORMSEL | AUTODIST | DECMD2 | DECMD1 | DECMD0 |
| INTMSK | H | X4 | ADPEND | DECTOUT | DMACMP | DECINT | CIERR | L | L | L |
| INTCLR | H | X5 | ADPEND | DECTOUT | DMACMP | DECINT | CIERR | L | L | L |
| CI | H | X6 | L | EMPHASIS | L | BITL4H8 | L | FSL3H1 | L | MONOSTE |
| DMAADRC-L | H | X7 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| DMAADRC-H | H | X8 | L | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 |
| DMAXFRC-L | H | X9 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| DMACTL | H | XA | xfrc11 | xfrc10 | xfrc9 | xfrc8 | DMAEN | L | L | L |
| DRVADRC-L | H | XB | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| DRVADRC-H | H | XC | L | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 |
| TEST2 | H | 1D | L | L | L | L | L | L | L | L |
| TEST1 | H | 1E | L | L | L | L | L | L | L | L |
| TEST0 | H | 1F | L | L | L | L | L | L | L | L |

Write Registers

| REG | A0 | RA | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|---|---|---|
| REGADR | L | X | X | X | X | RA4 | RA3 | RA2 | RA1 | RA0 |
| DMA DATA | H | 00 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| INTSTS | H | 01 | ADP END | DEC TOUT | DMA CMP | DEC INT | CI ERR | X | X | X |
| STS | H | 02 | DRQ | ADP BSY | ERIN BLK | COR INH | EDC OK | ECC OK | SHRT SCT | NO SYNC |
| HDRFLG | H | 03 | MIN | SEC | BLO CK | MODE | FILE | CHAN NEL | SUB MODE | CI |
| HDR MIN | H | X4 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| HDR SEC | H | X5 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| HDR BLOCK | H | X6 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| HDR MODE | H | X7 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| SHDR FILE | H | 08 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| SHDR CH | H | 09 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| SHDR S-MODE | H | 0A | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| SHDR CI | H | 0B | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| CMADR L | H | 0C | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| CMADR H | H | 0D | X | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 |
| MDFM | H | XE | X | X | X | RAW MD2 | RAW MD1 | RAW MD0 | C MODE | C FORM |
| ADPCI | H | XF | MUTE | EMPH ASIS | EOR | BIT L4H8 | X | FS L3H1 | X | MONO STE |
| DMA XFRC-L | H | 18 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| DMA XFRC-H | H | 19 | X | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 |
| DMA ADRC-L | H | 1A | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| DMA ADRC-H | H | 1B | X | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 |
| DRV ADRC-L | H | 1C | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| DRV ADRC-H | H | 1D | X | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 |
| TEST 0 to 2 | H | 10 to 2 | X | X | X | X | X | X | X | X |

Read Registers

—26—
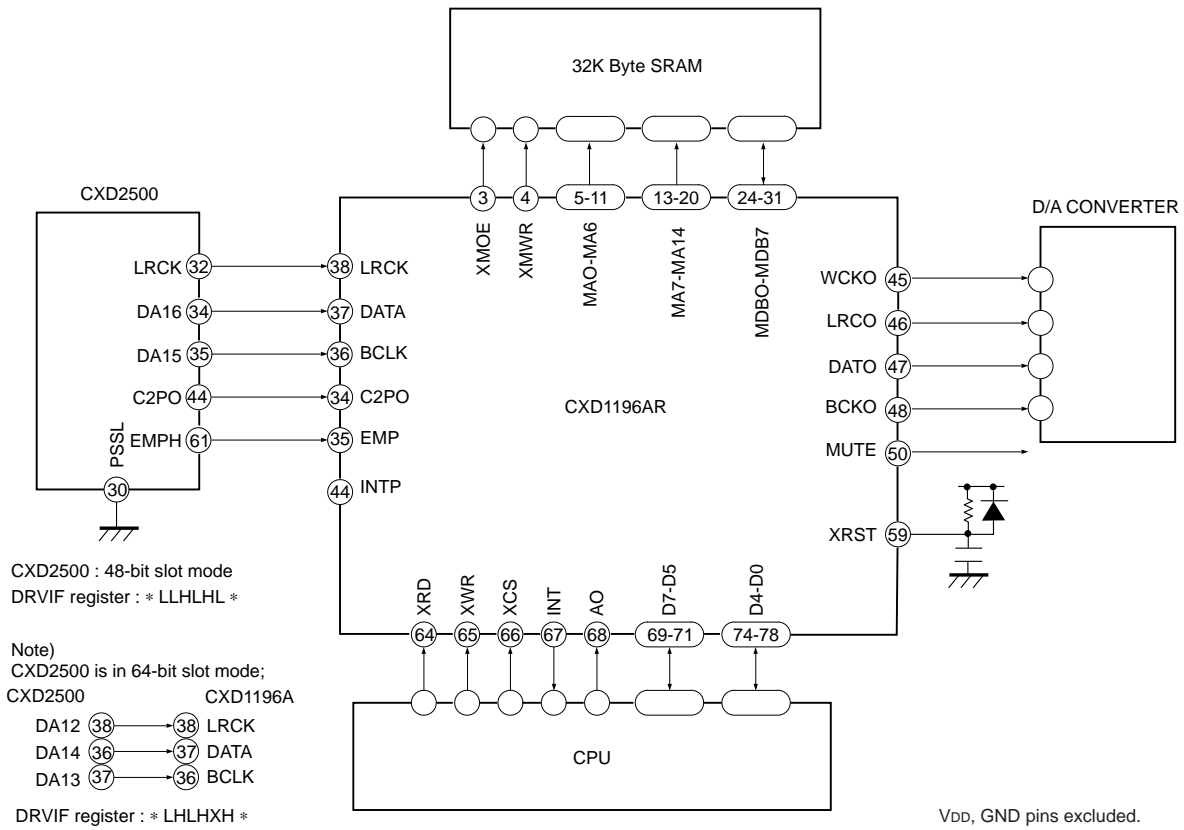
**CXD1196AR Connection Diagram**

**Package Outline**    Unit : mm

80PIN LQFP (PLASTIC)

□ 14.0 ± 0.2

∗ □ 12.0 ± 0.1

60        41

61                40

80        21
(0.22)

0.5    1        + 0.08        20
            0.18 − 0.03

⊕ 0.13 Ⓜ

(13.0)

0.5 ± 0.2

A

+ 0.05
0.127 − 0.02

+ 0.2
1.5 − 0.1

◠ 0.1

0.1 ± 0.1

0.5 ± 0.2

0° to 10°
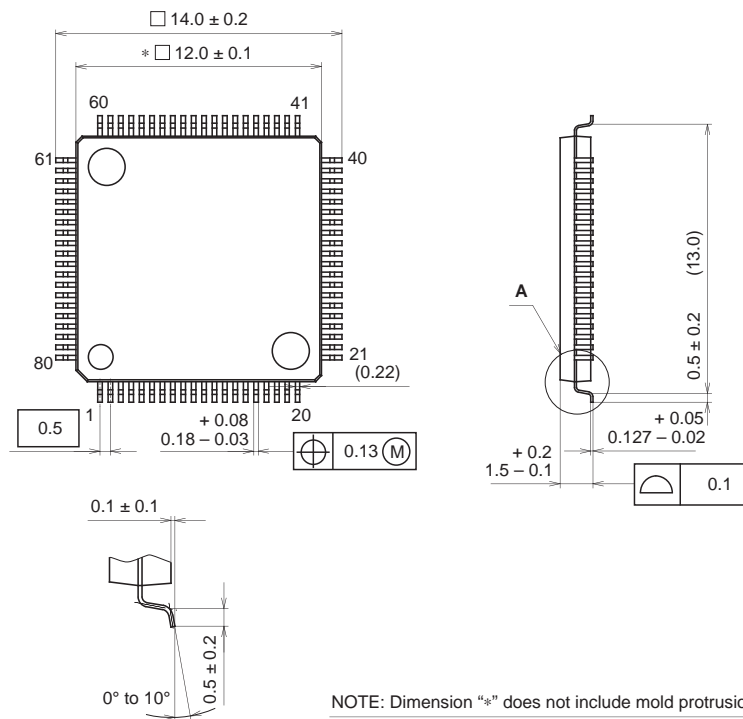
NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

| SONY CODE | LQFP-80P-L01 |
|---|---|
| EIAJ CODE | LQFP080-P-1212 |
| JEDEC CODE | |

PACKAGE STRUCTURE

| PACKAGE MATERIAL | EPOXY RESIN |
|---|---|
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE MASS | 0.5g |

—28—