

# SANYO Semiconductors DATA SHEET



# Monolithic Linear IC M — Sync Separator IC with AFC and Sync Detection Functions

#### Overview

The LA7218M is a sync separator IC with AFC designed for use in video cameras, VCRs, TVs, and similar products. It also provides a sync detection function. This IC can implement an adjustment-free system with high detection precision using a ceramic oscillator VCO and a PLL-based horizontal sync detection circuit.

#### Functions

- Sync separator
- Vertical sync separator
- Horizontal AFC
- VCO (32fH)
- Sync detector
- \* : Since the pin functions are fixed, this ICs performance cannot be adjusted with external signals. Furthermore, since this IC includes no EPROM or other memory, its software cannot be rewritten.

#### Features

- Ceramic oscillator adopted for adjustment-free manufacturing
- Negative outputs
- High-impedance video signal inputs
- Supply voltage : 5V

#### **Specifications**

#### Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		7	V
Allowable power dissipation	Pd max	Ta ≤ 65°C	150	mW
Operating temperature	Topr		-15 to +65	°C
Storage temperature	Tstg		-40 to +125	°C

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#### **Operating Conditions** at $Ta = 25^{\circ}C$

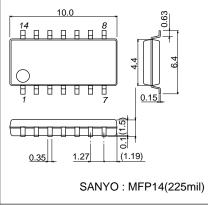
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	VCC		5.0	V
Operating supply voltage range	V <sub>CC</sub> op		4.5 to 5.5	V

# Electrical Characteristics at $Ta = 25^{\circ}C$ , $V_{CC} = 5V$

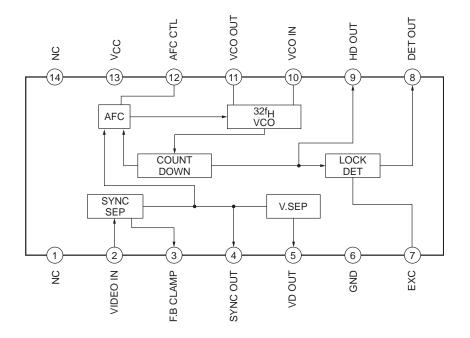
Parameter	Symbol	Conditions	Ratings			11-21
			min	typ	max	Unit
Current drain	ICC	Standard color bar input	4.9	7	9.1	mA
Sync separator minimum input level	V <sub>I</sub> min		-15	-11	-8	dB
HD output delay time	T <sub>HD</sub>	Compare pins 2 and 9	0	0.4	0.8	μs
HD output pulse width	T <sub>HW</sub>		3.5	4.9	5.3	μs
VD output delay time	T <sub>VD</sub>	Compare pins 2 and 5	9	13	17	μs
VD output pulse width	T <sub>VW</sub>		0.16	0.21	0.26	ms
Free-running frequency	FO	With switch SW1 off	15.4	15.75	16.1	kHz
Capture range 1	FCH	Discriminated by comparing pins 2 and 9	300	500		Hz
Capture range 2	FCL	Discriminated by comparing pins 2 and 9	1000	1500		Hz
SYNC output high level	V <sub>SH</sub>	Read from the pin 4 waveform	3.9	4.2		V
SYNC output low level	V <sub>SL</sub>	Read from the pin 4 waveform		0.8	1.0	V
HD output high level	V <sub>HH</sub>	Read from the pin 9 waveform	3.9	4.2		V
HD output low level	V <sub>HL</sub>	Read from the pin 9 waveform		0.8	1.0	V
VD output high level	VVH	Read from the pin 5 waveform	3.9	4.2		V
VD output low level	V <sub>VL</sub>	Read from the pin 5 waveform		0.8	1.0	V
DET output high level	VDH		4.8	5.0		V
DET output low level	V <sub>DL</sub>	SW1 off		0.1	0.3	V
Comparator threshold high level	VTH	SW2-a	2.7	2.95	3.2	V
Comparator threshold low level	V <sub>TL</sub>	SW2-a	2.4	2.7	3.0	V
Threshold width	V <sub>TW</sub>	V <sub>TH</sub> -V <sub>TL</sub>	0.10	0.22	0.40	V
DET operating current (high)	I <sub>DH</sub>	SW2-b	40	65	90	μΑ
DET operating current (low)	IDL	SW2-b	40	65	90	μΑ

## **Package Dimensions**

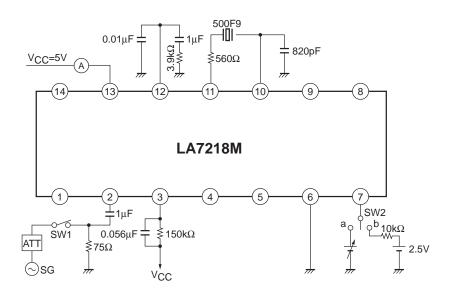




## **Equivalent Circuit Block Diagram**



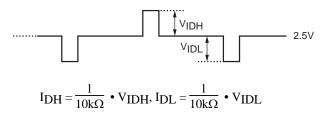
# **Test Circuit Diagram**



- $\bullet$  Set switch SW1 off only for f0 and  $V_{\mbox{\scriptsize DL}}$  measurement. Set it on for all other measurements.
- Switch SW2 has a neutral position, and is set to the "a" position for the V<sub>TH</sub> and V<sub>TL</sub> measurements, to the "b" position for the I<sub>DH</sub> and I<sub>DL</sub> measurements, and to neutral for all other measurements.
- Use a 1Vp-p standard color bar signal for the SG signal, use an attenuator for the VI min measurement, and use the waveform shown below for the f<sub>CH</sub> and f<sub>CL</sub> measurements.



- A square wave, such as that shown above, is used for the IDH and IDL measurement. It's frequency is 31.5kHz.
- The  $f_{CH}$  (and  $f_{CL}$ ) measurement is performed by setting the SG signal frequency high (or low) so that lock is lost and lowering (raising) the frequency from those points and measuring the two frequencies at which the circuit locks. The difference between these frequencies and f0 is  $f_{CH}$  (and  $f_{CL}$ ).
- The V<sub>TH</sub> (and V<sub>TL</sub>) measurement is performed by setting the pin 7 applied voltage V1 to 0V (or 5V) and raising (or lowering) the voltage from those points and measuring the V1 voltages at the points pin 8 switches (inverts) from low (high) to high (low). Those voltages are V<sub>TH</sub> and V<sub>TL</sub>, respectively.
- IDH and IDL are calculated from the pin 7 waveform as shown in the figure below.



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