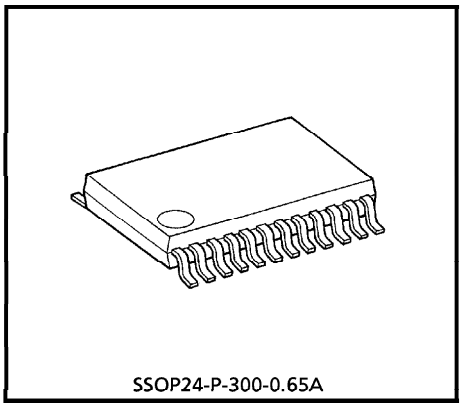
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA1297AFN

RF MODULATOR FOR VCR

The TA1297AFN is a PLL RF modulator for the UHF frequency range. The multi system can easily make the lineup development.



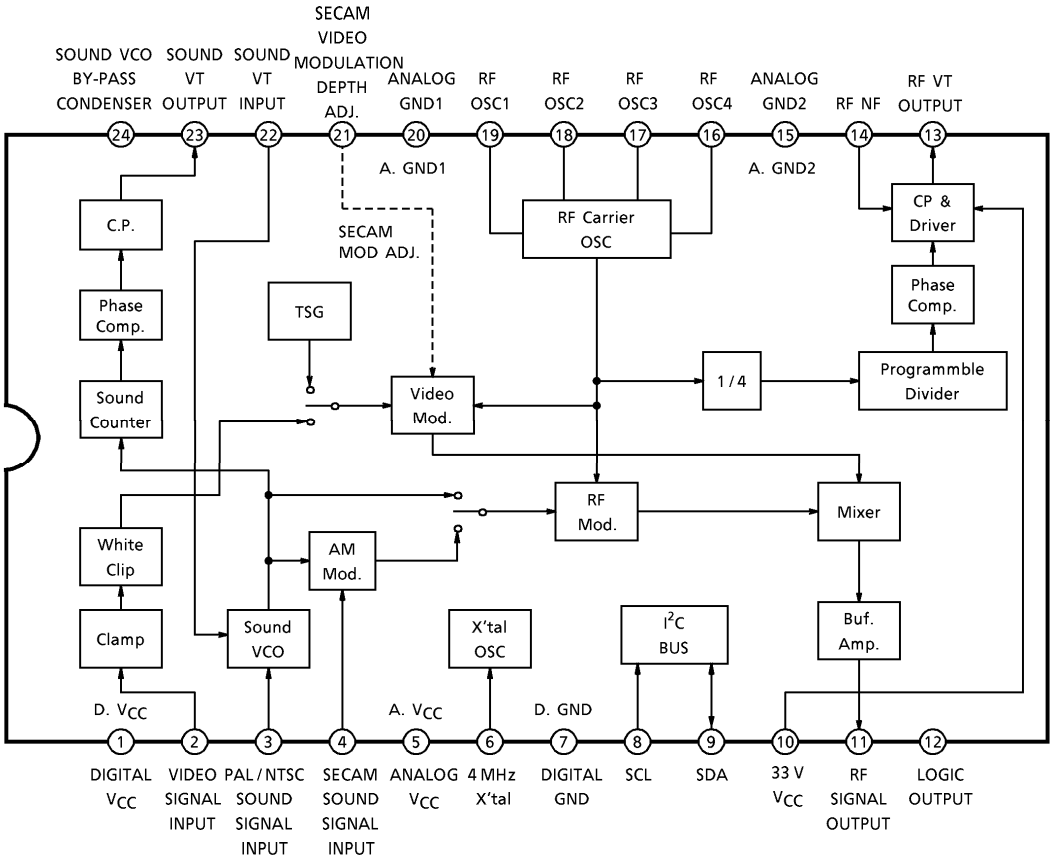
SSOP24-P-300-0.65A

Weight : 0.14 g (Typ.)

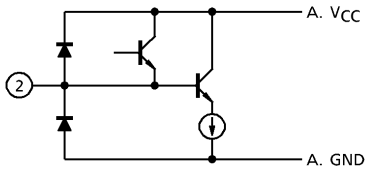
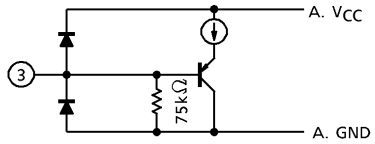
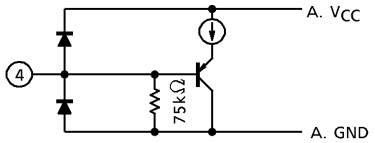
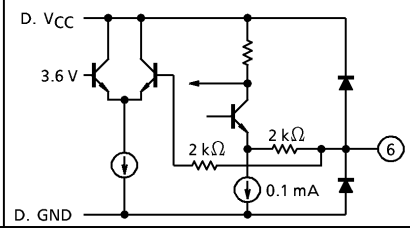
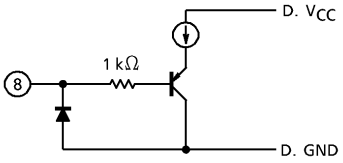
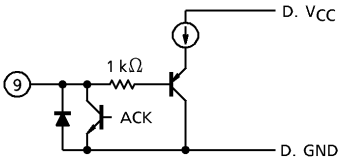
FEATURES

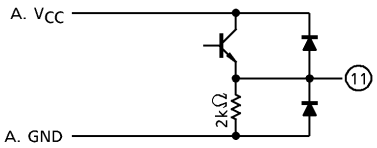
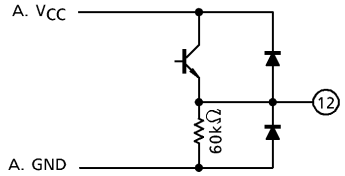
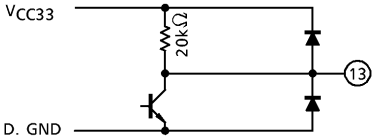
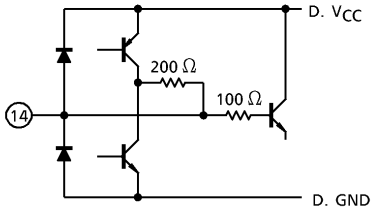
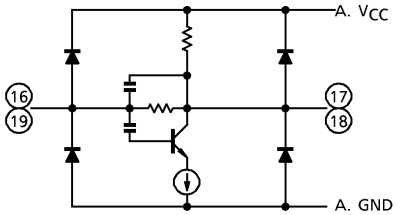
- Phase locked loop frequency synthesizer for RF carrier and sound subcarrier
- Programmable of no adjustment sound subcarriers (4.5 MHz, 5.5 MHz, 6.0 MHz, 6.5 MHz)
- Possible to use for L-SECAM
- Programmable picture to sound ratio
- Bus controlled Test pattern Signal Generator
- Bus controlled one logic output port
- Bus controlled power save mode
- Controlled by I^2C bus (Conforms to a fast-mode)
- The sound S/N ratio is improved from TA1243CFN

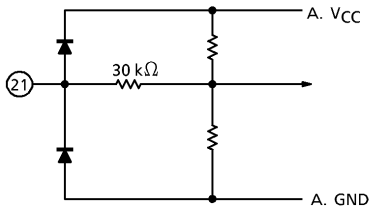
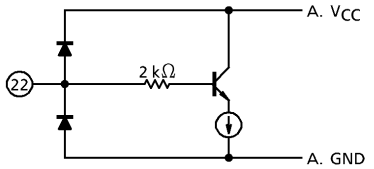
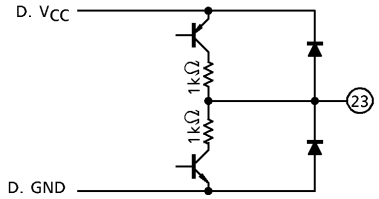
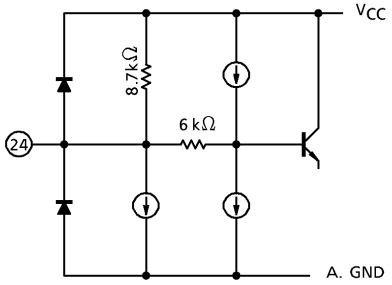
BLOCK DIAGRAM



TERMINAL CHARACTERISTICS (V_{CC1} = 5.0 V, V_{CC2} = 33 V, Ta = 25°C)

PIN No.	FUNCTION	TYP. DC VOLTAGE	TYP. AC VOLTAGE	INTERFACE	NOTE
1	Digital V_{CC}	(5.0 V)	—	—	—
2	Video Signal Input	2.4 V (Sync TIP)	0.5 V_{p-p}		Sync TIP clamp input
3	PAL / NTSC Sound Signal Input	0 V	200 mV_{p-p}		Switch terminal of normal mode and test mode. L : Normal mode (The voltage is under 2 V.) H : Test mode
4	SECAM Sound Signal Input	0 V	200 mV_{p-p}		
5	Analog V_{CC}	(5.0 V)	—	—	Analog power supply
6	4 MHz X'tal	2.7 V	—		Switch terminal of internal oscillation and external input mode. (Refer to page 9)
7	Digital GND	(0 V)	—	—	Digital ground
8	SCL	OPEN BASE	5 V_{p-p}		I^2C BUS serial clock
9	SDA	OPEN BASE	5 V_{p-p}		I^2C BUS serial data
10	V_{CC33}	(33 V)	—	—	Tuning voltage power supply

PIN No.	FUNCTION	TYP. DC VOLTAGE	TYP. AC VOLTAGE	INTERFACE	NOTE
11	RF Signal Output	3.8 V	80 dBμV (Picture)		
12	Logic Output	H : 4.3 V L : 0 V	—		BUS control I_{max} = 10 mA
13	RF V_T Output	—	—		Tuning voltage output
14	RF NF	—	—		
15	Analog GND2	(0 V)	—	—	Analog ground
16	RF OSC4	3.4 V	—		
17	RF OSC3	3.4 V			
18	RF OSC2	3.4 V			
19	RF OSC1	3.4 V			
20	Analog GND1	(0 V)	—	—	Analog ground

PIN No.	FUNCTION	TYP. DC VOLTAGE	TYP. AC VOLTAGE	INTERFACE	NOTE
21	SECAM Video Modulation depth Adj.	3.1 V	—		Possible to adjustment by the outside resistance. Resistance is inserted between V_{CC} and 21 pin : Modulation depth decreases Resistance is inserted between GND and 21 pin : Modulation depth increases
22	Sound VT Input	—	—		
23	Sound VT Output	—	—		
24	Sound VCO by-pass condenser	—	—		

I²C-BUS DATA FORMAT

		MSB							LSB	ACK
Address Byte	ADR	1	1	0	0	1	0	1	0	ACK
Control Byte1	C1	1	(*)	(*)	(*)	PS2	PS1	PS0	LE	ACK
Control Byte2	C2	WO	PSA	LO	FA1	FA0	(*)	(*)	(*)	ACK
Prog. Data Byte1	PD1	0	TSG	N10	N9	N8	N7	N6	N5	ACK
Prog. Data Byte2	PD2	N4	N3	N2	N1	0	1	0	0	ACK

(*) : Don't care

Bus data transmission : ADR + C1 + C2 + PD1 + PD2 or
ADR + PD1 + PD2 + C1 + C2 or
ADR + C1 + C2 or
ADR + PD1 + PD2

1. PS2~PS0 : Picture to sound ratio setting (Video signal input : Stair case (B / W) 0.5 V_{p-p}
Sound signal input : 1 kHz sin wave 0.2 V_{p-p})

PS RATIO (SYSTEM L)	PS RATIO (OTHER THAN SYSTEM L)	PS2	PS1	PS0
– 6 dB	– 10 dB	0	0	0
– 7 dB	– 11 dB	0	0	1
– 8 dB	– 12 dB	0	1	0
– 9 dB	– 13 dB	0	1	1
– 10 dB	– 14 dB	1	0	0
– 11 dB	– 15 dB	1	0	1
– 12 dB	– 16 dB	1	1	0
– 13 dB	– 17 dB	1	1	1

2. LE : System L enable

1 . . . This mode is SYSTEM L. Positive modulation for video and AM modulation for sound inter carrier at 6.5 MHz.
In this case, FA1 and FA2 don't care.

0 . . . Modes other than SYSTEM L. Negative modulation for video and FM modulation for sound inter carrier at 4.5 MHz, 5.5 MHz, 6.0 MHz, 6.5 MHz.
The system is selected by FA1 and FA2.

3. WO : Control of white clip

1 . . . White clip off. The system L is used, and the characteristic of 100% modulations can be evaluated.

0 . . . White clip on.

4. PSA : Control of power save

   1 ... Power save off. (normal operation)
   0 ... Power save on. Becomes waiting for the bus data.
   And power supplies other than the bus decoder are turned off.

The data of the decoder is maintained while V_{CC} is added.
When V_{CC} is turned off, power on reset changes the data of the decoder by turning on V_{CC} again.

5. LO : Control of logic out

   1 ... 12 pin become high voltage.
   0 ... 12 pin become low voltage.

6. FA1~FA0 : Sound Inter Carrier Frequencies setting

FA1	FA0	SOUND INTER CARRIER FREQUENCY	FREQUENCY DEVIATION
0	0	4.5 MHz	± 25 kHz
0	1	5.5 MHz	± 50 kHz
1	0	6.0 MHz	± 50 kHz
1	1	6.5 MHz	± 50 kHz

7. TPSG : Control of test pattern signal generator

   1 ... ON
   0 ... OFF (normal operation)

8. N10~N1 : Programmable Divider Data setting

   The frequency of VCO is calculated by the next expression.

   f_{VCO} = 31.25 kHz × 32 × N + 250 kHz
   N = 512 × N10 + 256 × N9 + 128 × N8 + 64 × N7 + 32 × N6 + 16 × N5 + 8 × N4 + 4 × N3 + 2 × N2 + N1

   The frequency step is 1 MHz, and 250 kHz is given in the IC.
   The divider data N is made frequency – 250 kHz of the set channel.

POWER ON RESET MODE

Power on reset functions when the power supply is turned on.
The decoder data is the data of power on reset until the bus data is received.
In this mode, because the power saving is turned on, the RF signal is not output.

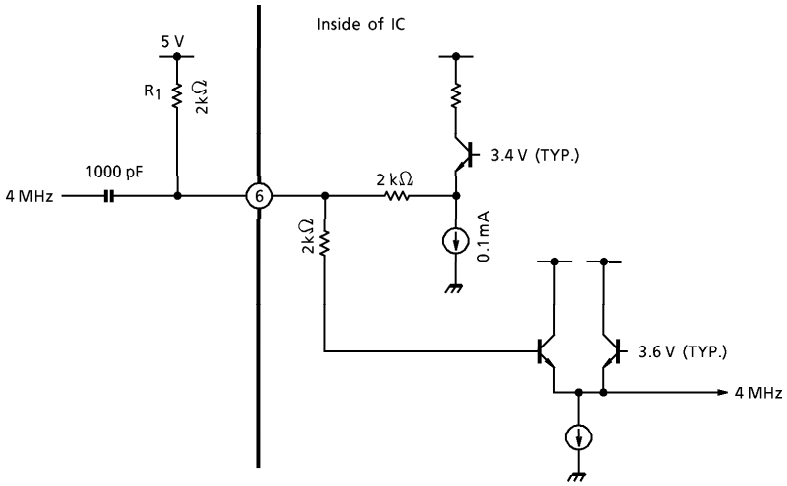
- VCO Frequency Setting : 591.25 MHz (CCIR 36 ch)
- Television System : System G (Sound carrier frequency : 5.5 MHz,
  FM deviation : ±50 kHz,
  Video modulation polarity : negative modulation)
- P/S Ratio Set Up : – 13 dB
- White Clip : ON
- Power Save : ON
- Logic Output : LOW
- TPSG : OFF

		MSB							LSB	ACK
Address Byte	ADR	1	1	0	0	1	0	1	0	ACK
Control Byte1	C1	1	(*)	(*)	(*)	0	1	1	0	ACK
Control Byte2	C2	0	0	0	0	1	(*)	(*)	(*)	ACK
Prog. Data Byte1	PD1	0	0	1	0	0	1	0	0	ACK
Prog. Data Byte2	PD2	1	1	1	1	0	1	0	0	ACK

(*) : Don't care

EXTERNAL 4 MHz INPUT MODE

It is possible to change to external 4 MHz input mode by connecting resistance (R_1) between terminal 6 and 5 V V_{CC}.



Condition of external 4 MHz input mode : In terminal 6, the voltage is above 3.8 V, the amplitude of 4 MHz signal is above 100 mV_{p-p} (sine wave).
Please design R_1, and an external circuit to suit the condition.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage 5 V System	V_{CC1}	8	V
Supply Voltage 33 V System	V_{CC2}	35	V
Power Dissipation (Note)	P_D	850	mW
Input Terminal Voltage	V_{IN}	GND − 0.3~V_{CC} + 0.3	V
Operating Temperature	T_{opr}	− 20~75	°C
Storage Temperature	T_{stg}	− 55~150	°C

(Note) : Derated linearly above Ta = 25°C in the proportion of 6.8 mW / °C.

Please note the product design of the board because the calorific value is large.

- The copper area is widened.
- Hole for heat radiation of shield case.
- Other enough consideration.

RECOMMENDED OPERATING CONDITION

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage 5 V System	V_{CC1}	4.5	5	5.5	V
Supply Voltage 33 V System	V_{CC2}	27	33	35	V

ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V, V_{CC2} = 33 V, Ta = 25°C, fp = 591.25 MHz)

	No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	MIN.	TYP.	MAX.	UNIT	NOTE
Whole	1-1	Supply Current 1 (A.V_{CC} + D.V_{CC})	I_{CC1}	—	41	58	66	mA	Power supply of 5 V part
	1-2	Supply Current 2 (A.V_{CC} + D.V_{CC})	I_{CC2}	—	4	6	8	mA	5 V power supply of power save
	1-3	Supply Current 3 (V_{CC} 33 V)	I_{CC3}	—	1.4	2.2	3.0	mA	Power supply of 33 V part
	1-4	Operating Frequency Range	fop	—	471.25	—	855.25	MHz	fp frequency
Video Part	2-1-1	Video RF Output Level (Negative Modulation)	$V_{on\,(fp)}$	—	77	80	83	dBμV	50 Ω Termination STAIR CASE (B / W) signal : 0.5 V_{p-p} input
	2-1-2	Video RF Output Level (Positive Modulation)	$V_{op\,(fp)}$						
	2-2-1	Video modulation Depth (Negative Modulation)	mpn	—	75	79	83	%	WHITE signal : 0.5 V_{p-p} input
	2-2-2	Video modulation Depth (Positive Modulation)	mpp	—	85	89	93		
	2-3-1	White Clipping Level (Negative Modulation)	mpn (MAX)	—	90	94	98	%	WHITE signal : 1.0 V_{p-p} input
	2-3-2	White Clipping Level (Positive Modulation)	mpp (MAX)	—	210	230	—		DG / DP : 5% / 5°, WHITE CLIP : OFF
	2-4-1	Differential Gain (Negative Modulation)	DGn	—	—	±3	±5	%	STAIR CASE : 0.5 V_{p-p} (chrominance signal 20 IRE)
	2-4-2	Differential Gain (Positive Modulation)	DGp						

	No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	MIN.	TYP.	MAX.	UNIT	NOTE
Video Part	2-5-1	Differential Phase (Negative Modulation)	DPn	—	—	±3	±5	°	STAIR CASE : 0.5 V_{p-p} (Chrominance signal 20 IRE)
	2-5-2	Differential Phase (Positive Modulation)	DPp						
	2-6-1	Video S/N Ratio (Negative Modulation)	mpn (S/N)	—	51	53	—	dB	0.1~5 MHz, Unweighting, WHITE 50% signal input
	2-6-2	Video S/N Ratio (Positive Modulation)	mpp (S/N)						
	2-7-1	Video Frequency Response (Negative Modulation)	fpn	—	—	±1	±2	dB	0.1~5 MHz 1 MHz Reference
	2-7-2	Video Frequency Response (Positive Modulation)	fpp						
	2-8	Average Picture Level Drift	mp (APL)	—	—	±0.5	±3.0	%	APL 10-90%, 50% Reference
	2-9	Sync Crush Level	Δsync	—	—	1	3	%	{1 − (Vsync/Vwhite) × (100/40)}
	2-10-1	Chroma Beat (Negative Modulation)	V_{cn}	—	—	−75	−70	dB	4.43 MHz sin wave : 0.5 V_{p-p} input, Video carrier level reference, P/S = −13 dB
	2-10-2	Chroma Beat (Positive Modulation)	V_{cp}	—	—	−65	−60		
	2-11-1	RF Carrier 2'nd Harmonic Level	V_{2fp}	—	—	−26	−20	dB	Reference = Video carrier level
	2-11-2	RF Carrier 3'rd Harmonic Level	V_{3fp}	—	—	−20	−12		
	2-12	Video Signal 2nd Harmonic Level	V_{pH}	—	—	−55	−50	dB	1 MHz sin wave : 0.5 V_{p-p} input, fp + 1 MHz Reference, fp + 2 MHz measurement
	2-13-1	Prescaller Spurious (fp × 1/2)	$V_{PR1/2}$	—	—	0	10	dBμV	—
	2-13-2	Prescaller Spurious (fp × 3/2)	$V_{PR3/2}$	—	—	10	20		
	2-14-1	Video Carrier Frequency Accuracy	Δfp	—	—	—	±100	kHz	X'tal series capacitor : 6 pF

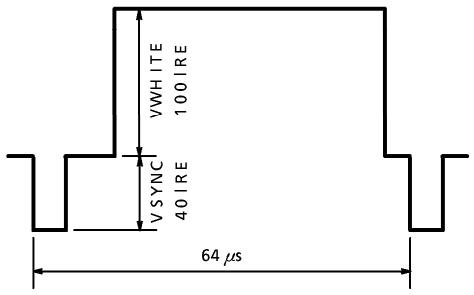
	No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	MIN.	TYP.	MAX.	UNIT	NOTE
TPSG Part	3-1-1	TPSG Modulation Depth (Negative Modulation)	mpn (TPSG)		64	74	84	%	TPSG mode
	3-1-2	TPSG Modulation Depth (Positive Modulation)	mpp (TPSG)		82	92	97		
	3-2	TPSG V / S Ratio	V / S		2.0	2.4	2.8	—	
	3-3-1	TPSG Horizontal Sync Signal Cycle	Tsync	—	62	64	66	μs	
	3-3-2	TPSG Horizontal Sync Signal Width	Wsync		3.6	4.0	4.4		
	3-4-1	TPSG SYNC-1'st Signal Time	W1		22	24	26		
	3-4-2	TPSG SYNC-2'nd Signal Time	W2		38	40	42		
Sound Part	4-1-1	P / S Ratio FM	$R_{P/S}$ FM	—	– 15	– 13	– 11	dB	Set in – 13 dB by bus, STAIR CASE (B / W) signal : 0.5 V_{p-p} input, 1 kHz sin wave input : 0.2 V_{p-p} (AM)
	4-1-2	P / S Ratio AM	$R_{P/S}$ AM	—	– 11	– 9	– 7		
	4-2-1	Range of P / S Ratio	$\Delta R_{P/SFM}$	—	– 17	—	– 10	dB	P / S ratio can be adjusted by 1 dB. 1 kHz sin wave input : 0.2 V_{p-p} (AM)
	4-2-2	Range of P / S Ratio	$\Delta R_{P/SAM}$	—	– 13	—	– 6		
	4-3-1	Sound Modulation Sensitivity FM1 (5.5 MHz/ 6.0 MHz / 6.5 MHz)	β_{FM1}	—	0.558	0.62	0.682	kHz / mV	1 kHz sin wave : 0.2 V_{p-p} input, β_{FM} = Δf (kHz) / 200 (mV)
	4-3-2	Sound Modulation Sensitivity FM2 (4.5 MHz)	β_{FM2}	—	0.279	0.31	0.341	kHz / mV	
	4-3-3	Sound Modulation Sensitivity AM	β_{AM}	—	63.9	71.0	78.1	%	1 kHz sin wave : 0.2 V_{p-p} input

	No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	MIN.	TYP.	MAX.	UNIT	NOTE
Sound Part	4-4-1	Sound S / N Ratio FM1 (5.5 MHz / 6.0 MHz / 6.5 MHz)	S / N (FM1)	—	54	59	—	dB	1kHz sin wave input : ±50 kHz dev. = 0 dB Inter Carrier demod., de-emph = IN, Colorbar signal : 0.5 V_{p-p} input
	4-4-2	Sound S / N Ratio FM2 (4.5 MHz)	S / N (FM2)	—	50	55	—		1 kHz sin wave input : ±25 kHz dev. = 0 dB Inter Carrier demod., de-emph = IN, Colorbar signal : 0.5 V_{p-p} input
	4-4-3	Sound S / N Ratio AM	S / N (AM)	—	50	55	—		1 kHz sin wave input : 60% mod. = 0 dB de-emph = IN, Colorbar signal : 0.5 V_{p-p} input
	4-5-1	Sound Distortion FM	THD (FM)	—	—	0.25	0.5	%	1 kHz sin wave : ±50 (25) kHz dev.
	4-5-2	Sound Distortion AM	THD (AM)	—					1 kHz sin wave : 60% MOD.
	4-6-1	Sound Frequency Response FM	fs (FM)	—	—	±1	±2	dB	100 Hz~20 kHz, 1 kHz reference
	4-6-2	Sound Frequency Response AM	fs (AM)	—	—	±0.5	±1		
	4-7-1	Sound 2'nd Harmonic Level	V_{SH1}	—	—	−65	−60	dB	P / S ratio = −13 dB, Video carrier level reference
	4-7-2	Sound 3'rd Harmonic Level	V_{SH2}	—	—	−70	−65		
	4-8	Sound Inter-Carrier Frequency Accuracy	Δfs	—	—	—	±750	Hz	X'tal series capacitor : 6 pF

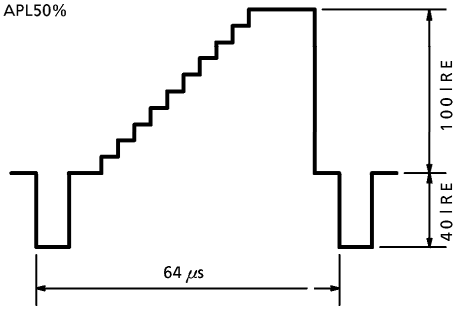
	No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	MIN.	TYP.	MAX.	UNIT	NOTE
Logic part	5-1	Input LOW Voltage of both SDA and SCL Lines	V_L	—	0	—	1.8	V	
	5-2	Input HIGH Voltage of both SDA and SCL Lines	V_H	—	2.8	—	V_{CC}		
	5-3	Maximum Output LOW Voltage of SDA Line	V_{ACK}	—	—	—	0.4	V	Isync = 3 mA, During the acknowledge clock pulse
	5-4	Threshold Voltage of Power on Reset	V_{RESET}	—	2.0	2.8	3.6	V	
	5-5	Threshold Voltage of External Reference Signal Input Mode	V_{EXT}	—	3.4	3.6	3.8	V	Voltage of terminal 6 L : Internal oscillation H : External input
	5-6	Threshold Voltage of Test mode	V_{TEST}	—	2.0	3.5	4.5	V	Voltage of terminal 3 L : Normal mode H : Test mode
	5-7	Logic Out Current	I_{LOGIC}	—	—	—	10	mA	Mounts on the board of power dissipation 830 mW. Ta (MAX) = 75°C
—	6-1	Negative Resistance of X'tal Oscillator	R_{XO}	—	− 1	—	—	kΩ	—
	6-2	Input Signal Level of External Reference Signal	V_{EXREF}	—	100	—	—	mV_{P-P}	External 4 MHz input mode, sine wave

INPUT WAVE FORM

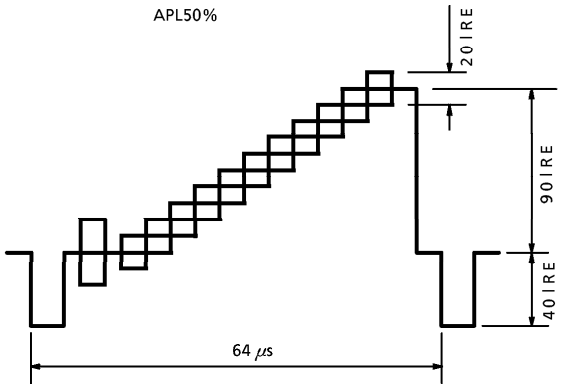
WHITE SIGNAL



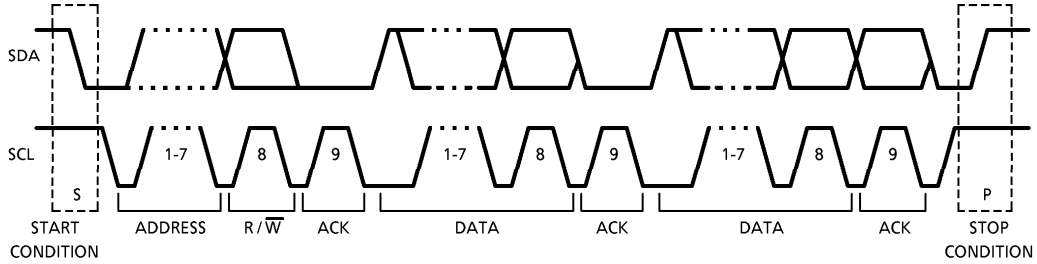
STAIRCASE (B/W) SIGNAL
APL50%



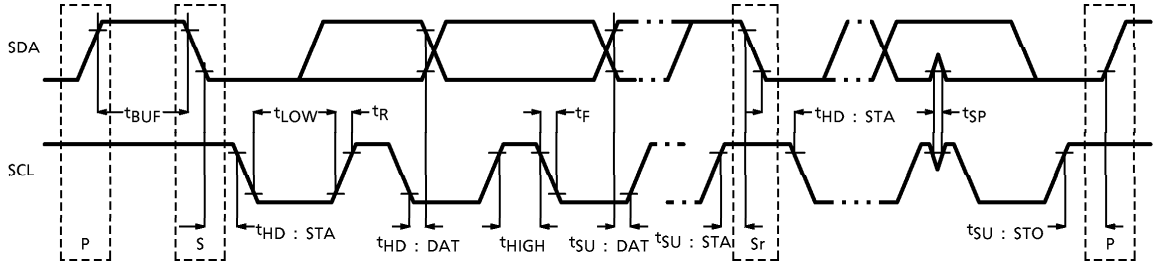
STAIRCASE SIGNAL (Sub-carrier 20 IRE)
APL50%



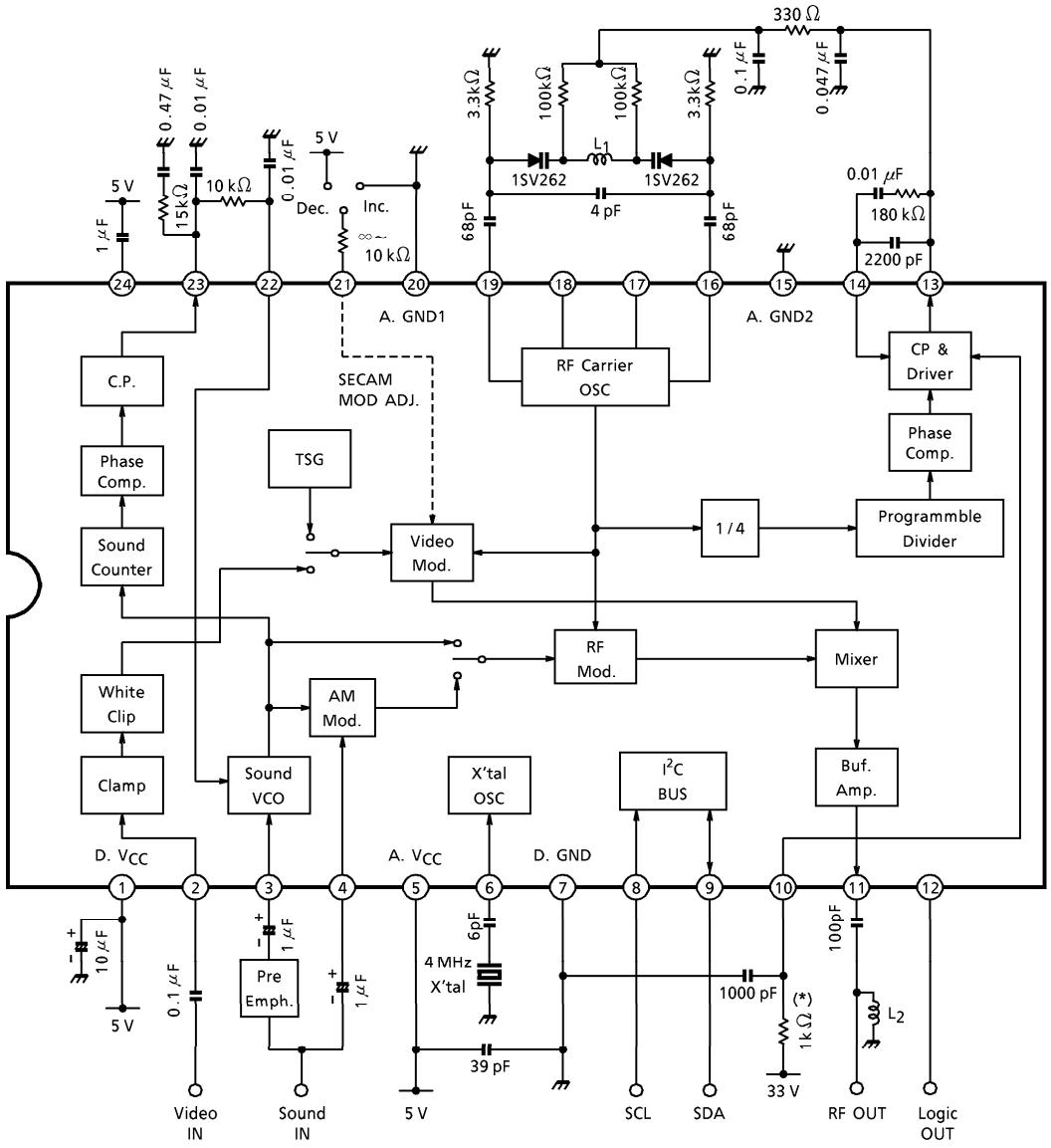
DATA TRANSFER ON THE I²C-BUS



TIMING REQUIREMENTS FOR THE I²C-BUS



APPLICATION CIRCUIT



L_1 : Coil Diameter 3.2 mm, Wire Diameter 0.4 mm, 2.5 turns, Air coil.
L_2 : For frequency response correction.
(*) : Protection resistance for prevention of overshoot.

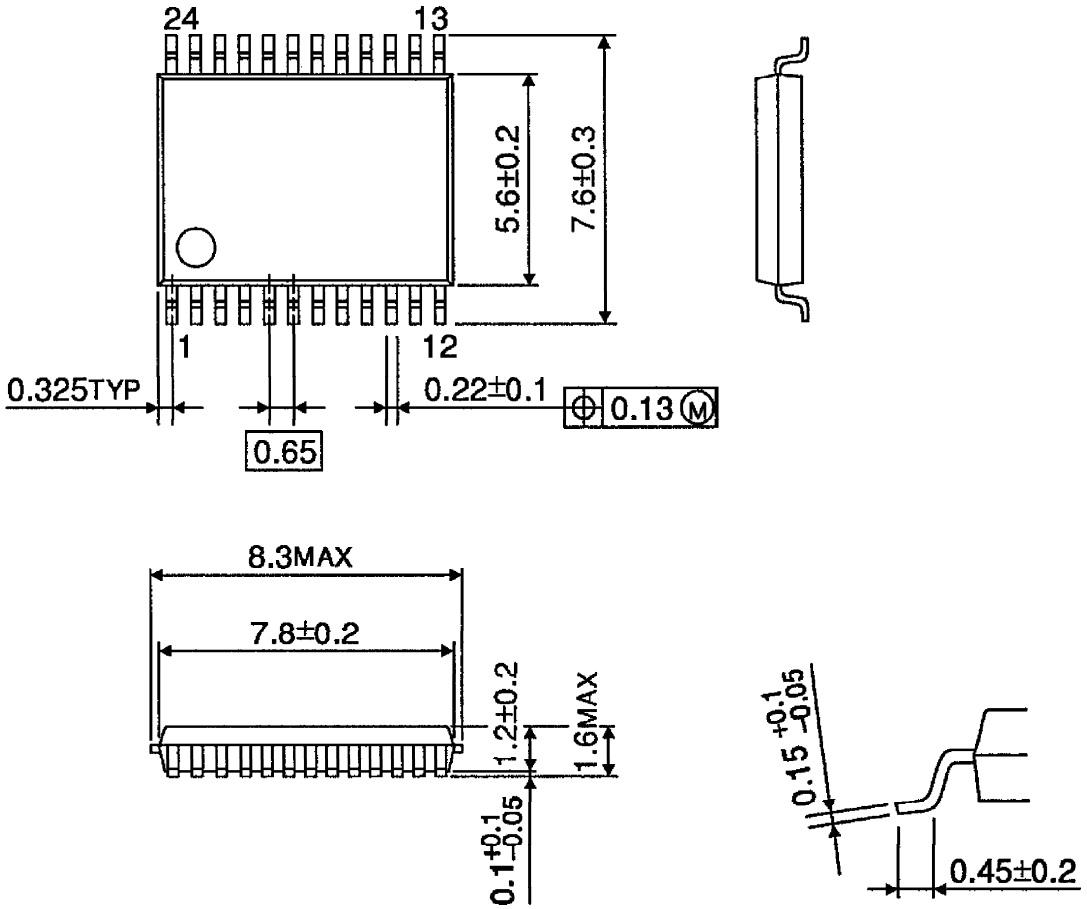
HANDLING PRECAUTIONS

1. The device should not be inserted into or removed from the test jig while the voltage is being applied: otherwise the device may be degraded or break down.
   Do not abruptly increase or decrease the power supply to the device either.
   Overshoot or chattering of the power supply may cause the IC to be degraded.
   To avoid this filters should be incorporated on the power supply line.
2. The application circuits described in this datasheet are given only as system examples for evaluating the device's performance. Toshiba Intend neither to recommend the configuration or related values of the peripheral circuits nor to manufacture such application system in large quantities.
   Please note that high-frequency characteristics of the device may vary depending on the external components, mounting method and other factors relating to the application design.
   Therefore, the characteristics of application circuits must be evaluated at the responsibility of the users incorporating the device into their design.
   Toshiba only guarantee the quality and characteristics of the device as described in this detasheet and do not assume any responsibility for the customers application design.
3. In order to better understand the quality and reliability of Toshiba semiconductor products and to incorporate them into design in an appropriate manner, please refer to the latest Semiconductor Reliability Handbook (Integrated Circuit) published by Toshiba Semiconductor Company.
   The handbook can also be viewed online at
   http://www.semicon.toshiba.co.jp/noseek/us/sinrai/sinraifm.htm

PACKAGE DIMENSIONS

SSOP24-P-300-0.65A

Unit : mm



Weight : 0.14 g (Typ.)