

3-Channel 2-LD Driver for Optical Disc Drive

Description

The CXA2640ER is a laser driver IC capable of driving two high output lasers (CD/DVD) for writeable optical discs.

Features

- CD maximum drive current: 300mA
DVD maximum drive current: 250mA
- Capable of generating three-value write waveform through control of one read channel and two write channels
- Rise/Fall times = 1ns
- Read Channel: $\times 100$
- Write Channel: $\times 840$ (CD), $\times 400$ (DVD)
- Read channel has extensive low-noise design
 $1.5\text{nA}/\sqrt{\text{Hz}}$ (@20MHz, ILD = 35mA, IMOD = 40mAp-p)
- Internal high frequency modulator circuit
Frequency variable range: 200 to 600MHz
Maximum modulator current amplitude: 100mAp-p
Can be set separately for CD and DVD.
- Timing input for generating write waveform can be adapted to both differential input (LVDS/LVPECL) and single end input (3.3V CMOS/TTL).
- Single 5V power supply

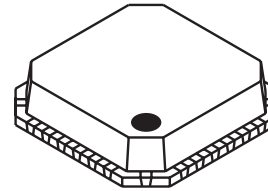
Applications

CD-R, CD-RW, DVD-R, DVD+RW, DVD-RW and DVD-RAM for high-speed writeable optical disc drives

Structure

Bipolar silicon monolithic IC

24 pin VQFN (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

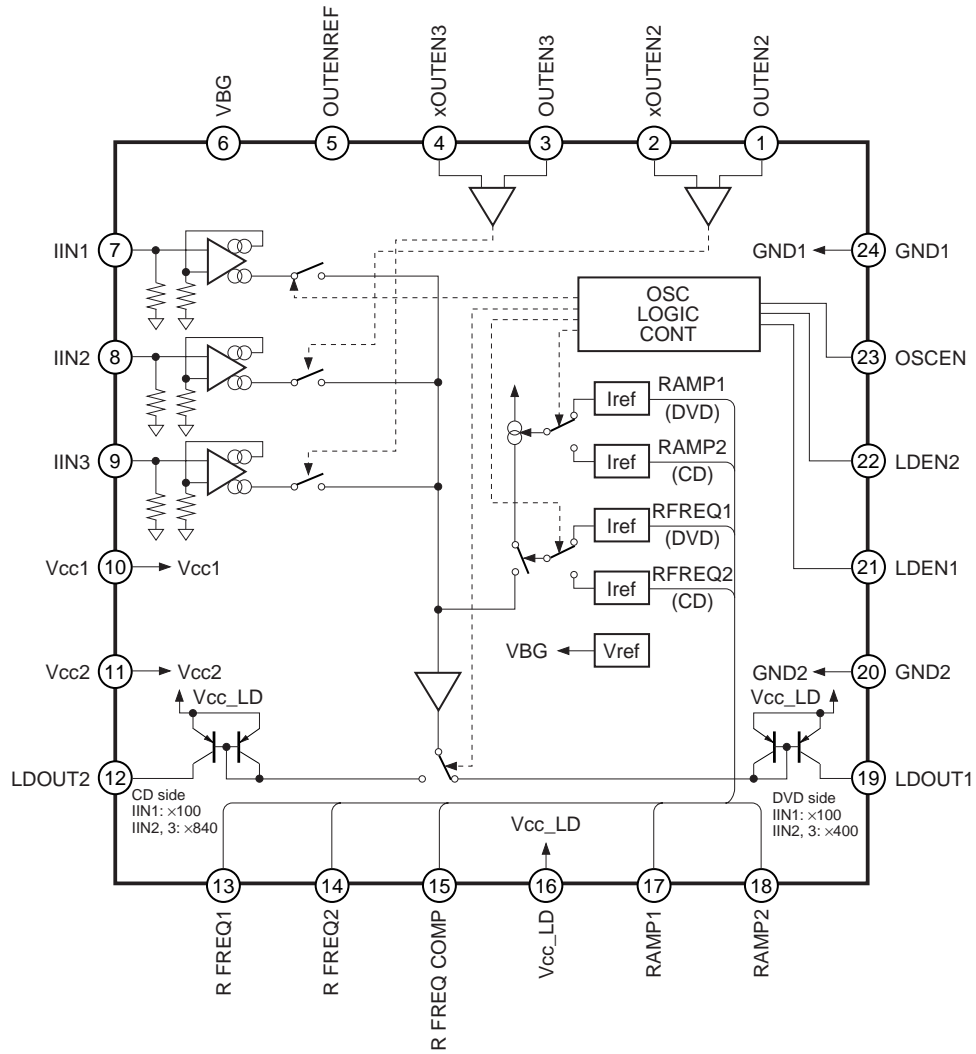
• Supply voltage	Vcc	5.5	V
• Storage temperature	Tstg	-65 to +150	°C

Operating Conditions

• Supply voltage	Vcc	4.5 to 5.5	V
• Operating temperature	Topr	-10 to +75	°C

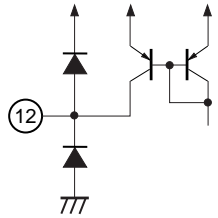
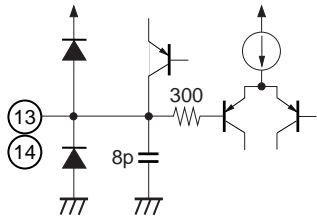
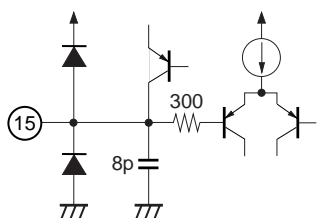
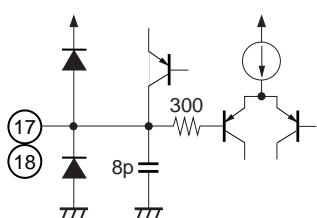
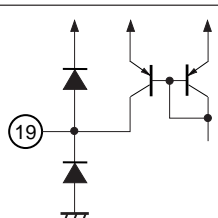
Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Pin voltage		Equivalent circuit	Description
			DC	AC		
1	OUTEN2	I	—	—		IIN2 set current control signal input. (positive logic)
2	xOUTEN2	I				IIN2 set current control signal input. (negative logic)
3	OUTEN3	I				IIN3 set current control signal input. (positive logic)
4	xOUTEN3	I				IIN3 set current control signal input. (negative logic)
5	OUTENREF	O	1.65V	—		Reference voltage output for current control signal. Connects decoupling capacitance to ground.
6	VBG	O	1.26V	—		Internal reference voltage decoupling.
7	IIN1	I	—	—		Current setting 1. The set current $\times 100$ is output when LDEN1 or LDEN2 = high.
8	IIN2	I	—	—		Current setting pin 2. The set current $\times 400$ is output through LDOUT1 when LDEN1 = high. The set current $\times 840$ is output through LDOUT2 when LDEN2 = high.
9	IIN3	I				Current setting pin 3. The set current $\times 400$ is output through LDOUT1 when LDEN1 = high. The set current $\times 840$ is output through LDOUT2 when LDEN2 = high.
10	Vcc1	I	—	—	—	Supply voltage for control system and modulator system.
11	Vcc2	I	—	—	—	Supply voltage for timing system and current switch.

Pin No.	Symbol	I/O	Pin voltage		Equivalent circuit	Description
			DC	AC		
12	LDOUT2	O	—	—		CD laser drive current output. Enabled when LDEN2 = high.
13	R FREQ1	O	—	—		Modulator frequency setting 1. Enabled when LDEN1 = high. Connects resistance to ground.
14	R FREQ2	O				Modulator frequency setting 2. Enabled when LDEN2 = high. Connects resistance to ground.
15	R FREQ COMP	O	—	—		Modulator frequency variation adjustment. Connects resistance to ground.
16	Vcc_LD	—	—	—	—	Output stage supply voltage.
17	RAMP1	O	—	—		Modulator amplitude setting 1. Enabled when LDEN1 = high. Connects resistance to ground.
18	RAMP2	O				Modulator amplitude setting 2. Enabled when LDEN2 = high. Connects resistance to ground.
19	LDOUT1	O	—	—		DVD laser drive current output. Enabled when LDEN1 = high.
20	GND2	—	—	—	—	Ground.

Pin No.	Symbol	I/O	Pin voltage		Equivalent circuit	Description
			DC	AC		
21	LDEN1	I	—	—		<p>DVD output control. (positive logic) When LDEN1 = high, the current set at IIN1 is output through LDOUT1.</p>
22	LDEN2	I	—	—		<p>CD output control. (positive logic) When LDEN2 = high, the current set at IIN1 is output through LDOUT2.</p>
23	OSCEN	I	—	—		<p>Modulator control. (positive logic) Outputs modulator waveform when OSCEN = high.</p>
24	GND1	—	—	—	—	Ground.

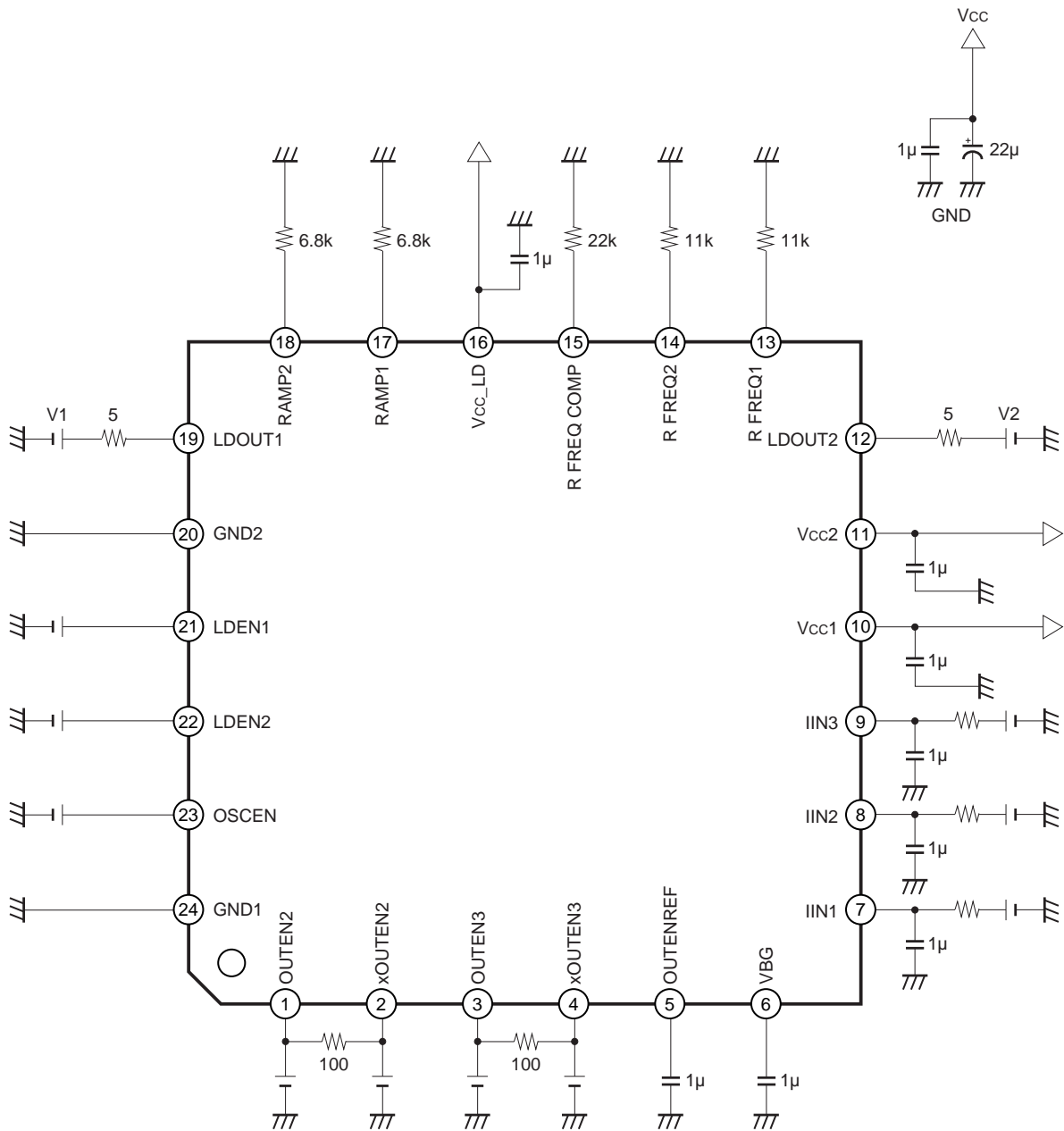
Electrical Characteristics

(V_{CC} = 5V, T_a = 25°C)

No.	Measurement item	Symbol	Min.	Typ.	Max.	Unit	Condition
1	Current consumption 1	I _{CC1}	10	16	22	mA	LDEN1, 2 = L
2	Current consumption 2	I _{CC2}	86	123	160	mA	LDEN1 (2) = H, IOUT1 = 60mA, OSCEN = H, AMP = 40mAp-p
3	Current consumption 3	I _{CC3}	128	183	238	mA	LDEN = H, IOUT1 = 60mA, IOUT2 = 120mA (Duty = 25%), IOUT3 = 60mA (Duty = 50%), IOUT = IOUT1 + IOUT2 + IOUT3
4	Current consumption 3-1	I _{CC3_1}	100	144	188	mA	LDEN = H, IOUT1 = 30mA, IOUT2 = 120mA (Duty = 25%), IOUT3 = 60mA (Duty = 50%), IOUT = IOUT1 + IOUT2 + IOUT3
<Logic input block: During single end transfer>							
5	Input voltage high level	V _{SH}	2	—	V _{CC}	V	
6	Input voltage low level	V _{SL}	GND	—	1.3	V	
<Logic input block: During differential input>							
7	Input voltage high level	V _{DH}	0.8	—	3	V	
8	Input voltage amplitude	V _{DL}	0.2	—	3	V	
<LD driver block: DC>							
9	LD drive current 1	I _{OUTR}	100	—	—	mA	
10	LD drive current 2, 3	I _{OUTW}	250	—	—	mA	
11	Total LD drive current 1 (DVD)	I _{OUT1}	250	300	—	mA	V _{CC} = 4.5V, VOP = 3V
12	Total LD drive current 2 (CD)	I _{OUT2}	300	350	—	mA	V _{CC} = 4.5V, VOP = 2.5V
13	Minimum LD drive current 1 (DVD)	OFFSET1	—	—	4	mA	I _{IIN1} = I _{IIN2} = I _{IIN3} = 0μA, LDEN1 = OUTEN2 = OUTEN3 = H
14	Minimum LD drive current 2 (CD)	OFFSET2	—	—	4	mA	I _{IIN1} = I _{IIN2} = I _{IIN3} = 0μA, LDEN2 = OUTEN2 = OUTEN3 = H
15	Output current noise 1 (DVD)	NOISE1	—	1.5	—	nA/√Hz	f = 400MHz, I _{LD} = 35mA, I _{mod} = 40mAp-p (20MHz: NOISE)
16	Output current noise 2 (CD)	NOISE2	—	1.5	—	nA/√Hz	f = 400MHz, I _{LD} = 35mA, I _{mod} = 20mAp-p (20MHz: NOISE)
<LD driver block: Pulse driving>							
17	Propagation delay	DELAY	—	3	—	ns	
18	Rise time (Tr)	TR	—	1.5	—	ns	I _{LD} = 50 to 100mA pulse Settling 10% to 90% (resistance load)
19	Fall time (Tf)	TF	—	1.5	—	ns	I _{LD} = 100 to 50mA pulse Settling 10% to 90% (resistance load)

No.	Measurement item	Symbol	Min.	Typ.	Max.	Unit	Condition
<ILD control block>							
20	Input resistance 1 (Pin 7)	ZIINR	0.56	0.8	1.04	k Ω	
21	Input resistance 2 (Pins 8, 9)	ZIINW	1.05	1.5	1.95	k Ω	
22	Input/output gain 1	GAINR	95	105	115	—	
23	Input/output gain 2, 3 (DVD)	GAINW1	360	400	440	—	
24	Input/output gain 2, 3 (CD)	GAINW2	765	840	935	—	
25	ILD control linearity 1 (DVD)	LINEA1	-3.5	—	2.5	%	Based on linearity when ILD = 50 to 150mA V _{cc} = 4.5V, V _I = 1.75V, R _L = 5 Ω , ILD = 250mA
26	ILD control linearity 2 (CD)	LINEA2	-3.5	—	2.5	%	Based on linearity when ILD = 50 to 150mA V _{cc} = 4.5V, V ₂ = 1V, R _L = 5 Ω , ILD = 300mA
27	Input/output gain relative precision	GACCU	-5	—	5	%	
28	Input/output transmission band	FBAND	7	—	—	MHz	Frequency for input/output gain of -3dB
<High frequency modulator>							
29	Frequency variable range	VARIF	200	—	600	MHz	
30	Amplitude variable range	VARIAMP	—	—	100	mA	f _{mod} = 400MHz
31	Frequency variation	FREQ	-10	—	10	%	f _{mod} = 400MHz
32	Frequency temperature characteristic	TFREQ	—	-116	—	ppm/ $^{\circ}$ C	f _{mod} = 300MHz
33	Amplitude variation	AMP	0	31	42	mAp-p	f _{mod} = 400MHz,
34	Amplitude temperature characteristic	TAMP	—	-319	—	ppm/ $^{\circ}$ C	f _{mod} = 300MHz, RAMP = 10k Ω
35	OSCEN response time (ON)	OSCREs1	—	5	—	ns	
36	OSCEN response time (OFF)	OSCREs2	—	5	—	ns	
<LDEN control>							
37	LDEN response time 1 (ON)	RLDRES1	—	—	700	ns	Time to reach 90% of Read set current (same condition as current consumption 2)
38	LDEN response time 1 (OFF)	RLDRES2	—	—	10	ns	Time to reach 10% of Read set current (same condition as current consumption 2)
39	LDEN response time 2 (ON)	WLDRES1	—	—	700	ns	Time to reach 90% of Write set current (same condition as current consumption 3)
40	LDEN response time 2 (OFF)	WLDRES2	—	—	10	ns	Time to reach 10% of Write set current (same condition as current consumption 3)

Electrical Characteristics Measurement Circuit



Description of Operation

(1) LD Drive Current Value Setting

The current controlled by the current setting pins IIN1, IIN2 and IIN3 is output from the LDOOUT1 and LDOOUT2 pins. IIN1, IIN 2 and IIN3 can be set respectively by LDEN1, LDEN2, OUTEN and xOUTEN for the output drive current from the LDOUT pin.

(2) Differential Input and Single-end Input

External processing is required for the differential input and single-end input switching. For the single-end input, if the device is used at the active Low, the OUTENREF pin and the OUTEN pin should be shorted externally; if it is used at the active High, the OUTENREF pin and the xOUTEN pin should be shorted externally. Leave the OUTENREF pin open for the differential input.

(3) Modulator Circuit

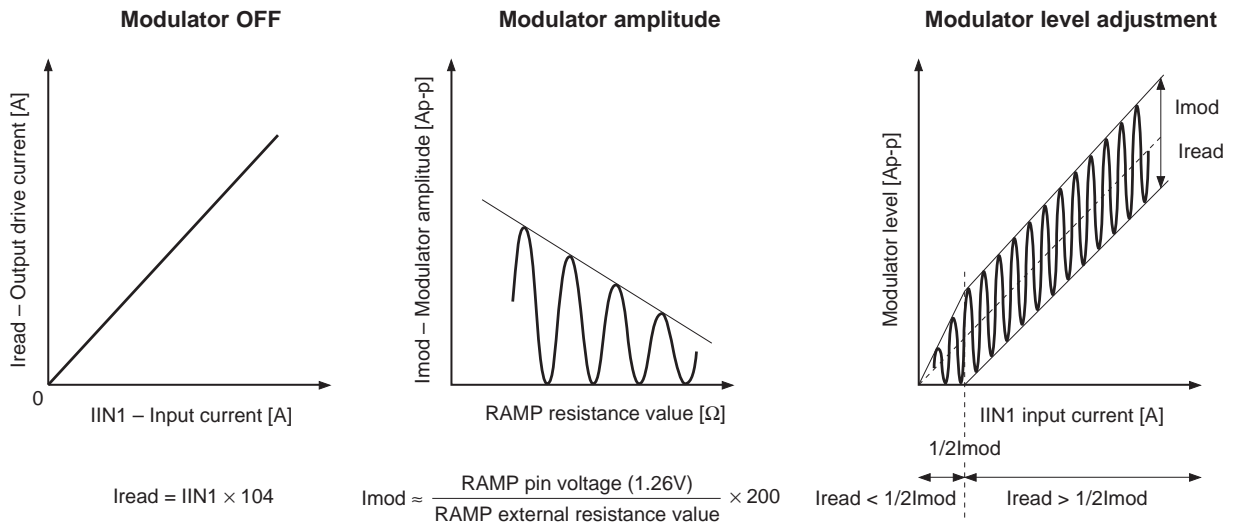
The modulator ON/OFF is controlled by the OSCEN pin. For the DVD side, the modulator frequency is varied by the external resistor connected to the RFREQ1 pin and the modulator amplitude can be varied by the external resistor value connected to the RAMP1 pin. For the CD side, the modulator frequency is varied by the external resistor connected to the RFREQ2 pin and the modulator amplitude can be varied by the external resistor value connected to the RAMP2 pin.

(4) RFREQ COMP Pin

The current depending on the internal resistor is generated using the RFREQ COMP pin external resistor to suppress the dispersion of the modulator frequency depending on the internal resistor. The RFREQ COMP pin external resistor is recommended to be fixed to 22kΩ.

(5) Modulator Level Adjustment

The modulator level adjustment can be performed by varying the IIN1 input current value.



Description of Functions

1. Logic table

Output control

LDEN1	LDEN2	xOUTEN2	xOUTEN3	OSCEN	LDOUT1 (DVD)	LDOUT2 (CD)
L	L	X	X	X	OFF	OFF
H	L	H	H	L	$100 \times \text{IIN1}$	OFF
H	L	L	H	L	$100 \times \text{IIN1} + 400 \times \text{IIN2}$	OFF
H	L	H	L	L	$100 \times \text{IIN1} + 400 \times \text{IIN3}$	OFF
H	L	L	L	L	$100 \times \text{IIN1} + 400 \times \text{IIN2} + 400 \times \text{IIN3}$	OFF
L	H	H	H	L	OFF	$100 \times \text{IIN1}$
L	H	L	H	L	OFF	$100 \times \text{IIN1} + 840 \times \text{IIN2}$
L	H	H	L	L	OFF	$100 \times \text{IIN1} + 840 \times \text{IIN3}$
L	H	L	L	L	OFF	$100 \times \text{IIN1} + 840 \times \text{IIN2} + 800 \times \text{IIN3}$
H	H	X	X	X	OFF (inhibit)	OFF (inhibit)

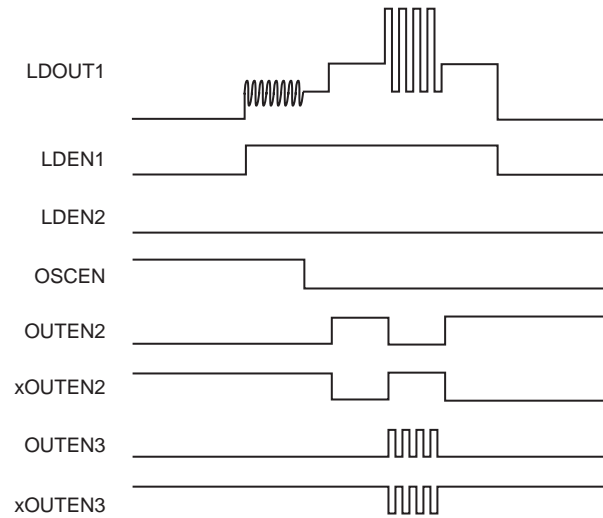
Module control

LDEN1	LDEN2	xOUTEN2	xOUTEN3	OSCEN	LDOUT1	LDOUT2
L	L	X	X	X	OFF	OFF
H	L	X	X	L	MODOFF	OFF
H	L	X	X	H	MODON (Rfreq1, Ramp1)	OFF
L	H	X	X	L	OFF	MODOFF
L	H	X	X	H	OFF	MODON (Rfreq2, Ramp2)
H	H	X	X	X	OFF (inhibit)	OFF (inhibit)

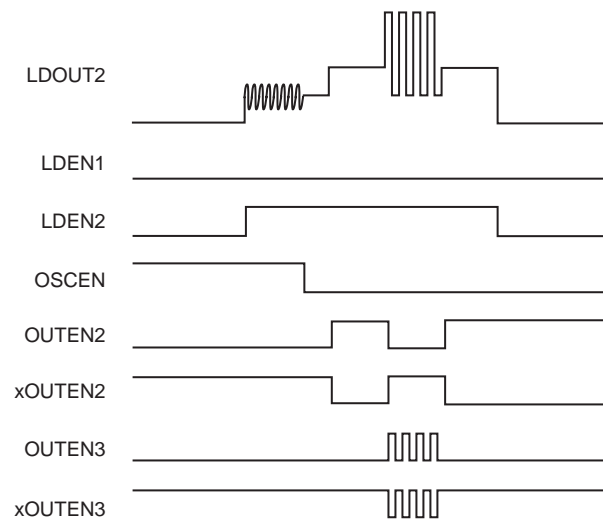
Note: Module control does not depend on a data timing signals.

2. Timing Chart

(DVD side)



(CD side)



Notes on Operation

- Arrange the external resistors connected to the IIN1, IIN2 and IIN3 pins near the IC package to reduce the affects from other signal lines.
- Wiring between the output LDOOUT pin and the laser diode, and wiring between the Vcc_LD pin and external decoupling capacitors should be the shortest. Making the distance for wiring long increases output waveform overshoots and undershoots caused by the affect of wiring inductance.
- The Vcc_LD pin's external decoupling capacity ground can be grounded to the GND grounding the load from the LDOOUT pin. This reverses the phase of the drive waveform at the LDOOUT and Vcc_LD and moves in the direction that suppresses overshoots and undershoots.

- Temperature guarantee

Thermal resistance (θ_{j-a}) when the CXA2640ER is mounted on PWB varies according to the set (PWB) and because it is difficult to predict along with the tendency for higher power for power consumption (P_o), the following points should be considered when using.

Use in a range that does not exceed a junction temperature of 150°C. Also, power consumption (P_o) should be below allowable power dissipation (P_D). Use with the thermal resistance (θ_{j-a}) of the PWB mounting lowered so that it can be operated normally at a maximum operating temperature of 75°C. To lower θ_{j-a} , radiating measures on the set, such as widening the GND region with the set PWB are needed. Also, the die-pad on the CXA2640ER 24-pin VQFN package is exposed on the backside, so thermal transmission from the IC backside to the PWB is excellent. For that reason, it is possible to release heat from the PBC to the set chassis thereby lowering the thermal resistance of the PWB mount.

Find the thermal resistance (θ_{j-a}) when mounted on PWB and power consumption (P_o) using the following method.

$$P_o = (I_{cc} \times V_{cc}) - (I_{op} \times V_{op})$$

I_{cc} : IC current consumption when operating (Including I_{op})

I_{op} : Output drive current flowed from the LDOOUT pin to the Laser Diode

V_{op} : Operating voltage of the laser diode

It is also possible for P_o when a modulator is ON ($I_{mod} = 40\text{mA}_{p-p}$), although the precision will decrease.

On the DVD side: $P_o = (50\text{mA} + I_{IN1} \times 2.6 + (I_{IN2} + I_{IN3}) \times 10) \times V_{cc} + (I_{op} \times (V_{cc} - V_{op}))$

On the CD side: $P_o = (50\text{mA} + I_{IN1} \times 2.6 + (I_{IN2} + I_{IN3}) \times 21) \times V_{cc} + (I_{op} \times (V_{cc} - V_{op}))$

Thermal resistance (θ_{j-a}) when mounted on PWB

- The thermal resistance (θ_{c-a}) is obtained by measuring the Package surface temperature using a thermo couple or a radiation thermometer.

In order to improve the precision of measurement, it is desired to calculate by the following formula.

Δ Package surface temperature when I_{op} is variable/ ΔP_o
 Assume the thermal resistance (θ_{j-c}) to be approximately 2°C/W.

- Diode thermal coefficient $-2.27mV/^\circ C$ and the positive protection diode thermal characteristics are used to find this.

The V_2 voltage found in (2) below cancels the voltage decrease caused by the wiring resistance between the positive protection diode connection V_{cc} and the V_{cc} pins as reference and is measured to find the precise temperature characteristics of the positive protection diode.

- (1) V_1 to OSCEN pin voltage to V_{cc} pin voltage, I_{cc1} to current consumption when 0V is applied to the IIN1, IIN2 and IIN3 pins.
- (2) V_2 to OSCEN pin voltage to V_{cc} pin voltage immediately after applying the arbitrary voltage to the IINx pin.
- (3) V_3 to OSCEN pin voltage to V_{cc} pin voltage, I_{cc3} to consumption current when applying the arbitrary voltage to the IINx pin and heat reaches equilibrium.

ΔT_j using the voltage drop (V_1 to V_2) between the positive protection diode connection V_{cc} and the V_{cc} pins that are the reference, as described above are:

$$\Delta T_j = ((V_3 + (V_1 - V_2)) - V_1) / -2.27mV/^\circ C$$

Thermal resistance (θ_{j-a}) is:

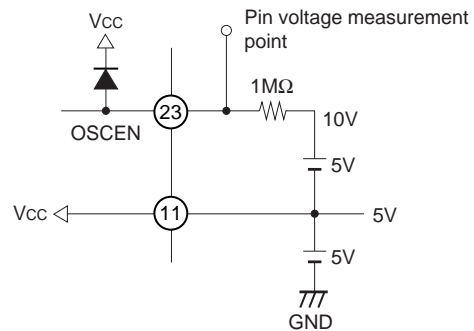
$$\theta_{j-a} = \Delta T_j / ((I_{cc3} - I_{cc1}) \times V_{cc} - I_{op} \times V_{op})$$

- Allowable power dissipation (P_D) $\geq P_O$ [W]

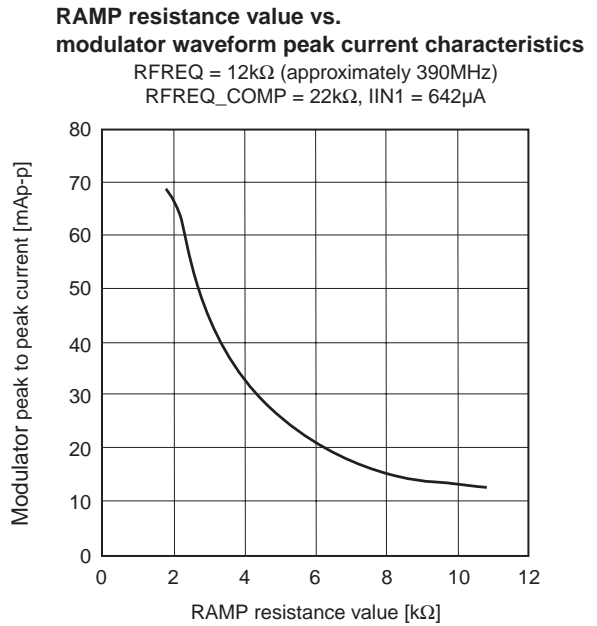
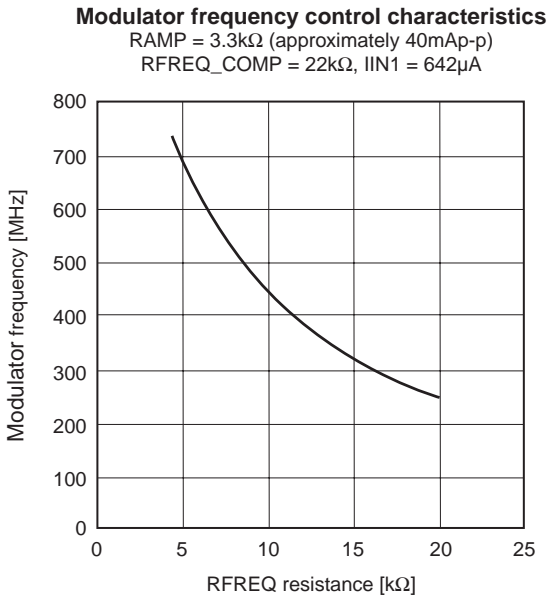
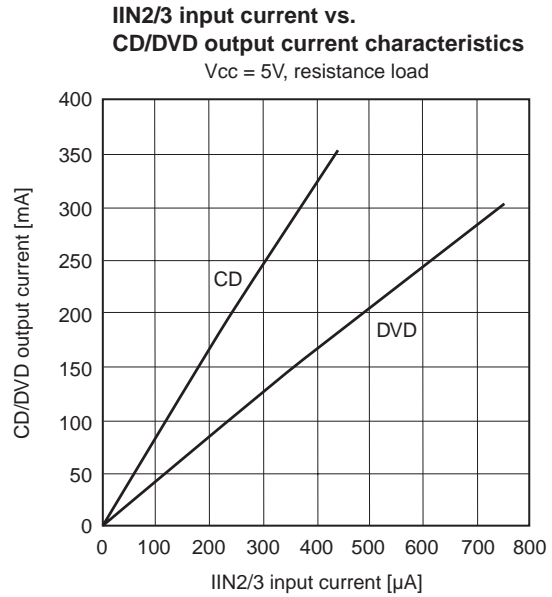
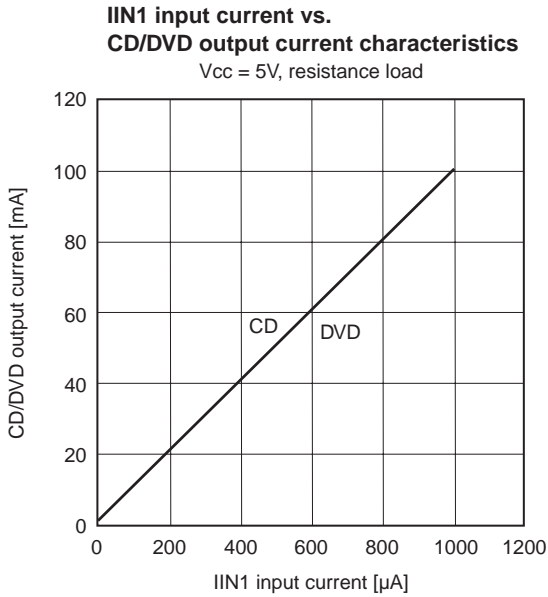
$$P_D = (150^\circ C - \text{Ambient temperature}) / \theta_{j-a}$$

- Maximum operating temperature

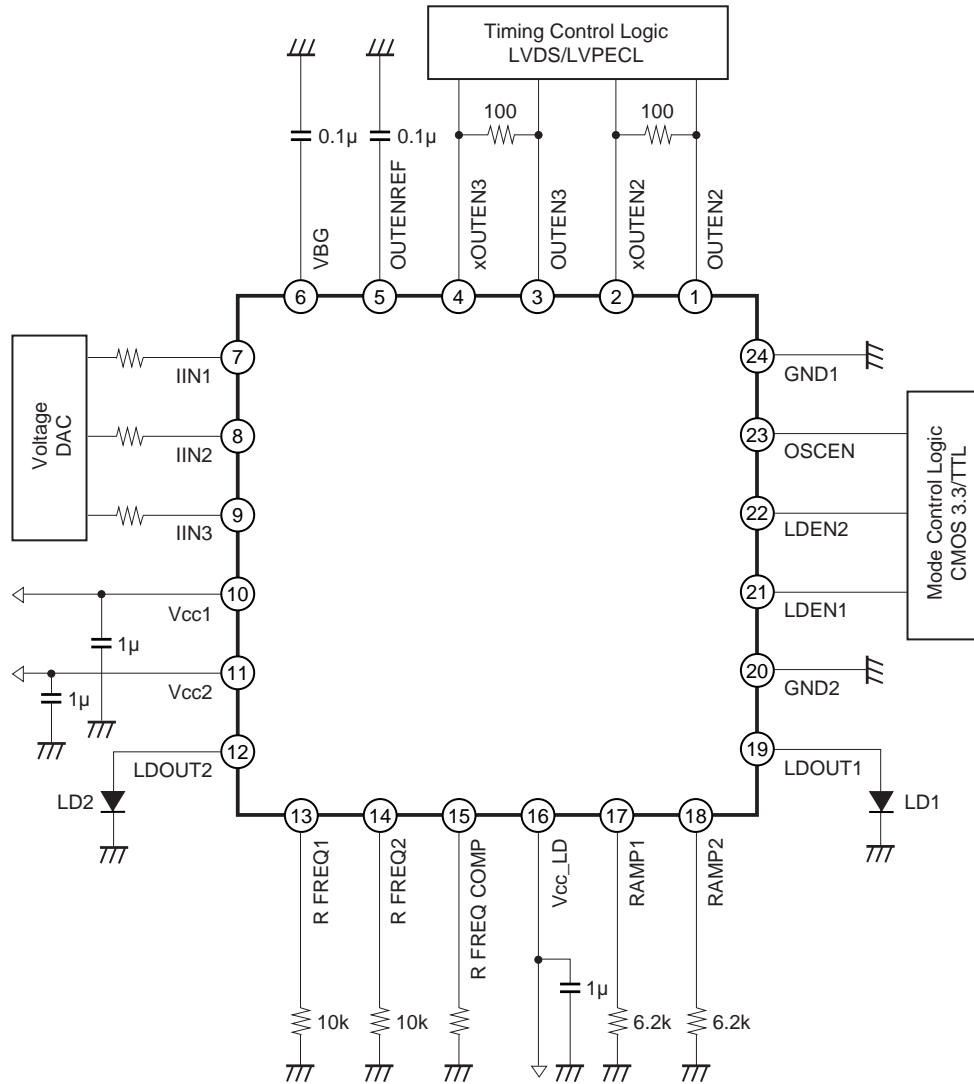
$$(150^\circ C - \Delta T_j) \geq 75^\circ C$$



Example of Representative Characteristics

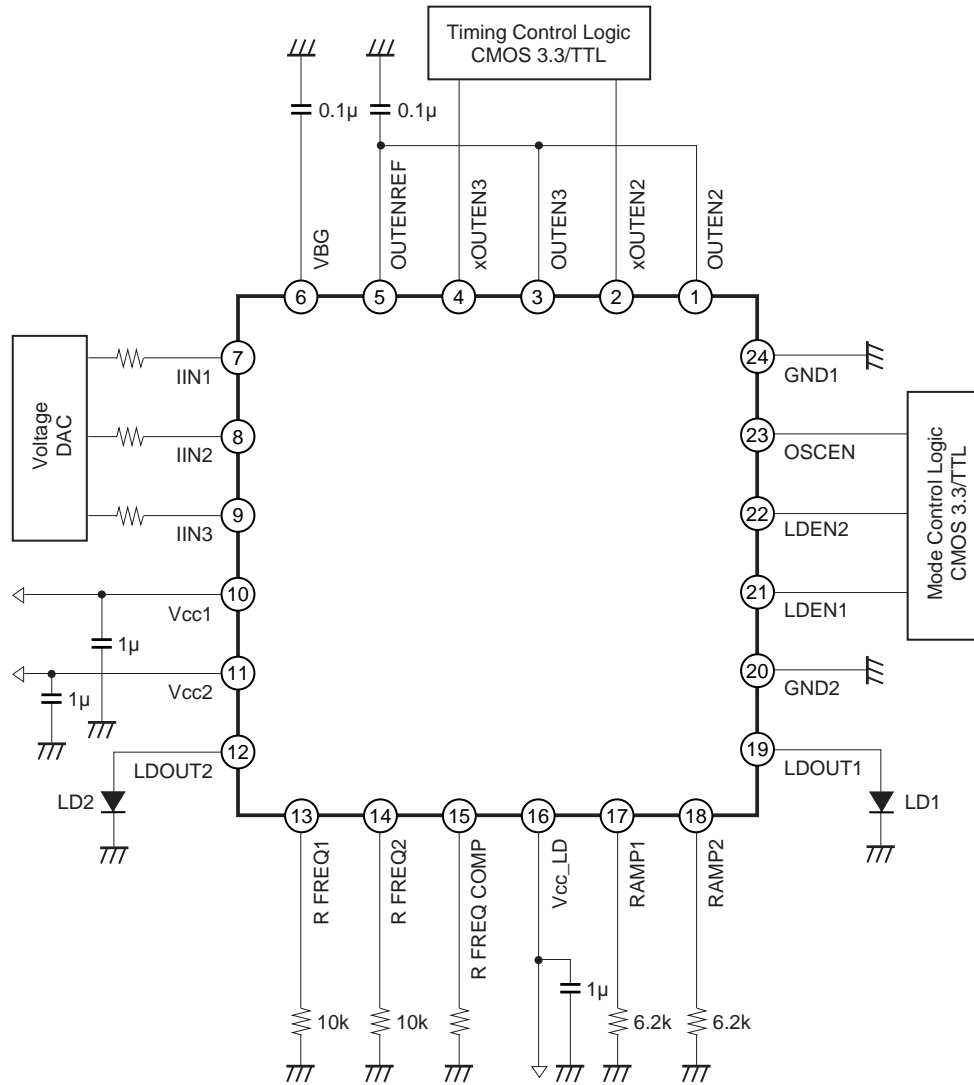


Application circuit 1



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

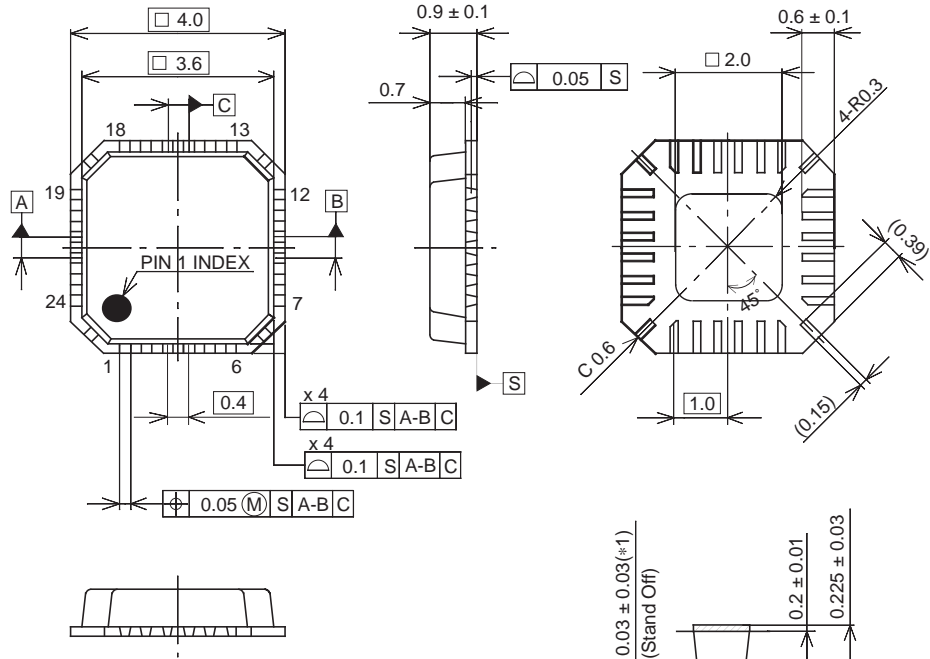
Application circuit 2



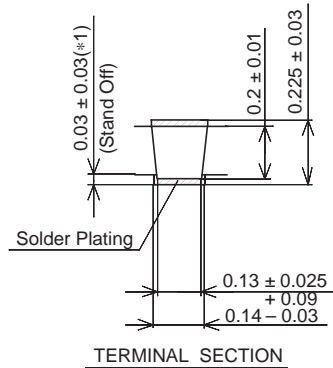
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

24PIN VQFN(PLASTIC)



NOTE: 1) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.
 2) The dimension of (*1) is apply to DiePad and the lead.



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g

SONY CODE	VQFN-24P-04
EIAJ CODE	_____
JEDEC CODE	_____

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm