SONY

CXA2610N

Laser Driver

Description

The CXA2610N is a laser driver IC for optical discs. This IC supports higher optical power output speeds.

Features

- LD driver with excellent driving capability
- Write current of 250mA (max.) possible by setting the IIN2 (Pin 2) and IIN3 (Pin 5) external resistors
- Rise time ≈ 3ns
- Fall time ≈ 4ns
- The oscillation frequency of the built-in oscillation circuit can be set from 100 to 600MHz by connecting the OSCFR (Pin 4) external resistor to GND.
- The oscillator amplitude initial value of the built-in oscillation circuit can be set by connecting the OSCGA (Pin 12) external resistor to GND, and the oscillator amplitude can be adjusted by the IINR input current value.
- Oscillation ON/OFF can be set as desired.
- Single +5V power supply
- TTL/CMOS control for control system

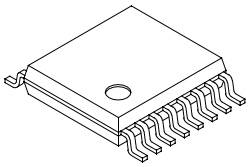
Applications

- CD-R driver
- CD-RW driver
- DVD driver
- Writable optical driver
- Laser diode current switching

Structure

Bipolar silicon monolithic IC

16 pin SSOP (Plastic)



Absolute Maximum Ratings

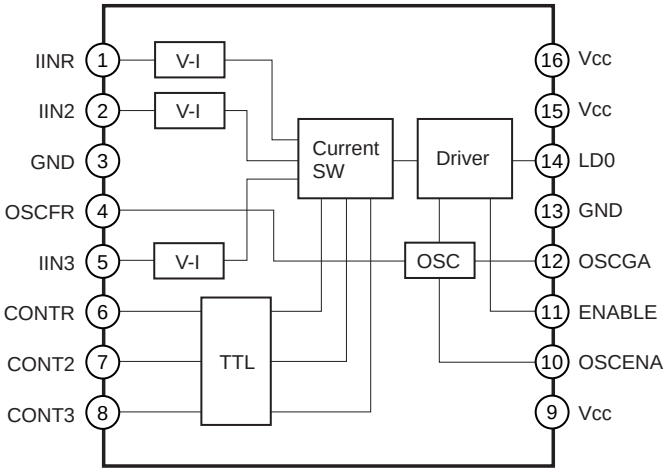
• Supply voltage	Vcc	5.5	V
• Operating temperature	Topr	–10 to +70	℃
• Storage temperature	Tstg	–65 to +150	℃

Operating Conditions

Supply voltage	4.5 to 5.5	V

E99320-PS

Block Diagram



Pin Description

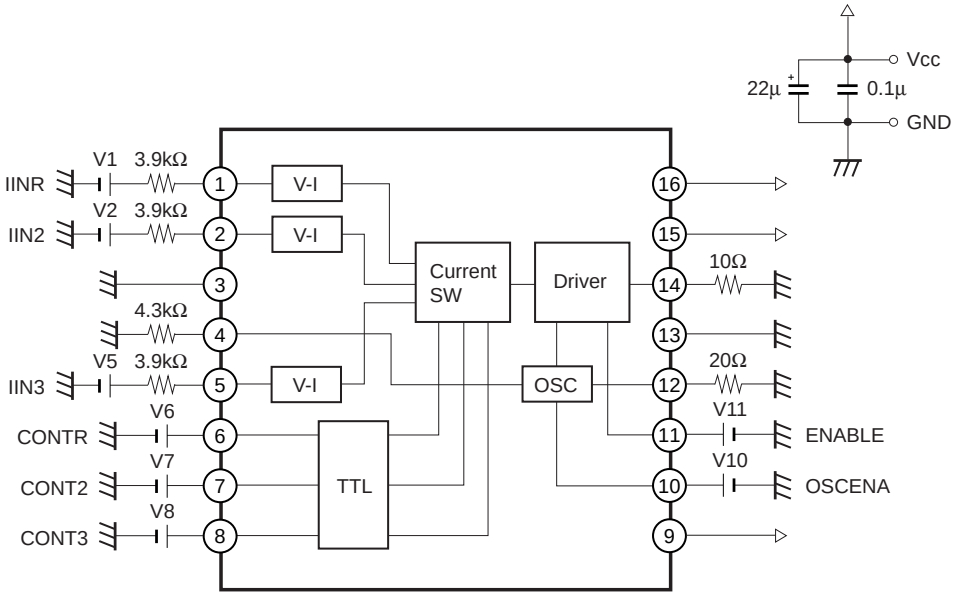
Pin No.	Symbol	I/O	Description
1	IINR	I	Oscillation level adjustment.
2	IIN2	I	LD drive current setting input.
3	GND	—	Ground.
4	OSCFR	I	Oscillation frequency adjustment.
5	IIN3	I	LD drive current setting input.
6	CONTR	I	LD drive current output setting.
7	CONT2	I	LD drive current output setting.
8	CONT3	I	LD drive current output setting.
9	Vcc	—	Vcc.
10	OSCENA	I	Oscillation ON for read/forced oscillation ON control.
11	ENABLE	I	LD drive current ON/OFF control. (High: ON, Low: OFF)
12	OSCGA	I	Oscillation level initial value setting.
13	GND	—	Ground.
14	LD0	O	LD anode side connection.
15	Vcc	—	Vcc.
16	Vcc	—	Vcc.

Electrical Characteristics

(Ta = 25°C, Vcc = 5V)

Measurement No.	Measurement item	Symbol	Control status					Measurement condition and method	Min.	Typ.	Max.	Unit
			CONTR	CONT2	CONT3	OSCENA	ENABLE					
1	Current consumption 1	$I_{CC}1$	2.0	2.0	2.0	1.3	1.3	OSC: L (write mode). LD: OFF	20	35	52	mA
2	Current consumption 2	$I_{CC}2$	↓	↓	↓	2.0	2.0	Current consumption for IINR input voltage where oscillation level = 47mAp-p	35	55	75	mA
3	Current consumption 3	$I_{CC}3$	1.3	↓	↓			Current consumption when CONTR = Low for $I_{CC}2$ (OSC: ON)	50	78	105	mA
4	Pin voltage 1	VFR	—	—	—			Pin voltage measurement	1.21	1.257	1.3	V
5	Pin voltage 2	VLE	—	—	—	↓	↓	Pin voltage measurement	80	103	120	mV
6	Output drive current	$I_{OUT}1$	1.3	2.0	2.0	1.3	2.0	Output current for IINR pin input 5V	115	125	145	mA
7	Output drive current	$I_{OUT}2$	2.0	1.3	↓	2.0		Output current for IIN2 pin input 5V	145	157	175	mA
8	Output drive current	$I_{OUT}3$	↓	2.0	1.3	↓		Output current for IIN3 pin input 5V	145	163	175	mA
9	Input/output current gain	$I_{GAIN}1$	1.3	2.0	2.0	1.3		Current gain measurement for IINR ($\Delta I_{OUT}/\Delta I_{IN}$)	95	104	115	—
10	Input/output current gain	$I_{GAIN}2$	2.0	1.3	↓	2.0		Current gain measurement for IIN2 ($\Delta I_{OUT}/\Delta I_{IN}$)	120	133	145	—
11	Input/output current gain	$I_{GAIN}3$	↓	2.0	1.3	↓	↓	Current gain measurement for IIN3 ($\Delta I_{OUT}/\Delta I_{IN}$)	120	136	145	—
AC items												
12	Rise time	TR	1.3	H → L	2.0	2.0	2.0	I_{OUT} = 40mA (CONTR) + 40mA (CONT2), settling 10 to 90%		3		ns
13	Fall time	TF		L → H				I_{OUT} = 40mA (CONTR) + 40mA (CONT2), settling 10 to 90%		4		ns
14	Overshoot	OVS	↓	H → L	↓			I_{OUT} = 40mA (CONTR) + 40mA (CONT2)		—		%
15	CONT delay 1	CDELAY1	2.0	1.3	H → L			Time from 50% of CONT3 (High → Low) to 50% of output final value		3.1		ns
16	CONT delay 2	CDELAY2	↓	↓	H → L	↓	↓	Time from 50% of CONT3 (Low → High) to 50% of output final value		3.4		ns
17	LD delay 1	LDELAY1	1.3	2.0	2.0	1.3	L → H	Time from 50% of ENABLE (Low → High) to 50% of output final value		4.4		ns
18	LD delay 2	LDELAY2	↓	↓		↓	H → L	Time from 50% of ENABLE (High → Low) to 50% of output final value		2.2		ns
19	Oscillation frequency	OSCFR	1.3	2.0		2.0	2.0	Oscillation frequency		189		MHz
20	Oscillation level	OSCLE	↓	↓	↓	↓	↓	Oscillation level when IINR = 2V	60	77	85	mAp-p
Logic												
21	Logic Low level	VTHL	—	—	—	—	—	CONTR, CONT2, CONT3, OSCENA, ENABLE			1.3	V
22	Logic High level	VTHH	—	—	—	—	—	CONTR, CONT2, CONT3, OSCENA, ENABLE	2			V
23	Input resistance	ZIN	—	—	—	—	—	Input impedance for IINR, IIN2 and IIN3	175	252	375	Ω

Electrical Characteristics Measurement Circuit



Description of Functions

(1) LD drive current value setting

The current controlled by the current setting pins IINR, IIN2 and IIN3 is output from the LD0 pin.
The current flowing to the LD0 pin can be set independently for IINR, IIN2 and IIN3 by CONTR, CONT2 and CONT3.

(2) LD drive current forced OFF

Forced OFF is enabled by setting the ENABLE pin Low.

(3) Oscillation circuit

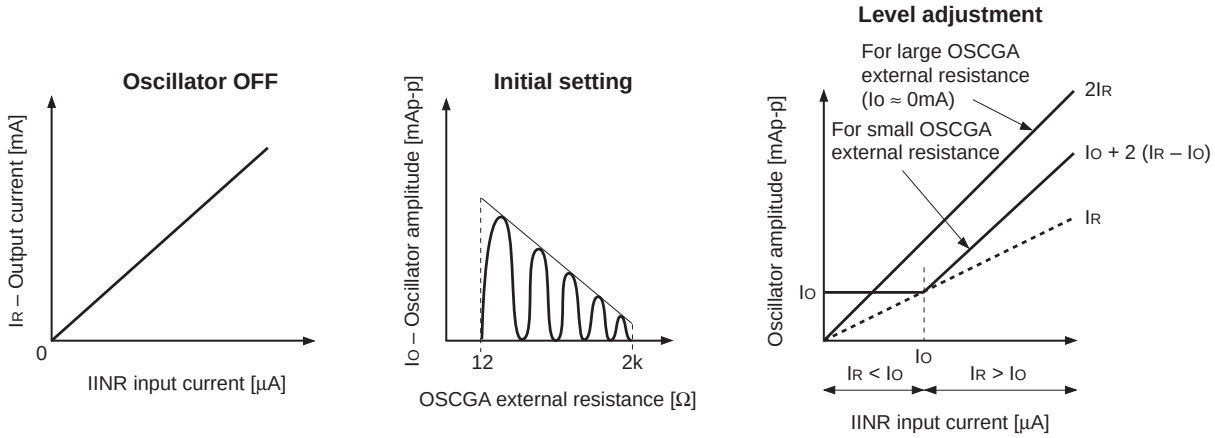
The oscillation circuit is turned ON forcibly by setting the OSCENA pin Low.
($\overline{OSCENA} \times \overline{CONTR} \times (\overline{CONT2} + \overline{CONT3})$)
The oscillation circuit is turned ON by setting the OSCENA pin High only for read.
($OSCENA \times \overline{CONTR} \times CONT2 \times CONT3$)

(4) Oscillation frequency adjustment

The oscillation frequency can be varied by the external resistance value connected to the OSCFR pin.

(5) Oscillation level adjustment

The oscillation level initial value can be set by the external resistance value connected to the OSCGA pin.
The oscillation level can be adjusted by varying the IINR input current value.
In addition, the read block DC compensation current I_R that flows when oscillation is OFF is independent of the OSCGA pin external resistance value, and is constant.



$$I_O \approx \frac{\text{OSCGA pin voltage}}{\text{OSCGA external resistance}} \times \frac{40}{9} \text{ [mAp-p]}$$

(6) Logic

The logic table for the CONTR, CONT2, CONT3 and ENABLE pins is shown below.
Be sure to also check the timing chart on page 7.

ENABLE	CONTR	CONT2	CONT3	LD0
L	X	X	X	OFF
H	H	H	H	OFF
H	L	H	H	IINR
H	L	L	H	IINR + IIN2
H	L	H	L	IINR + IIN3
H	L	L	L	IINR + IIN2 + IIN3

Notes on Operation

- Locate the external resistors connected to the IINR, IIN2 and IIN3 pins close to the IC package to prevent the effect from other signal lines.
- Make the wiring distance between the output LD0 pin and the laser diode as short as possible.
  If this wiring is longer, the output waveform characteristics show that the rise and fall times (Tr and Tf) become slower as the ringing becomes larger.
- The external resistor connected to Pin 10 (OSCGA) should be within the range from 12Ω to 2kΩ.
  In addition, this resistance value should be set in consideration of the laser diode Ith so that the oscillation level at IINR = 0V does not exceed the read power.
- Temperature assurance
  The junction temperature for the CXA2610N laser driver should not exceed 150°C. In addition, the power consumption (P_O) should be the allowable power dissipation (P_D) or less, and the IC should be used with a lowered thermal resistance (θj-a) for board mounting so that normal operation is possible at the maximum operating temperature of 70°C.
  Widening the GND area on the set board and other heat radiation countermeasures within the set are necessary in order to lower θj-a.
  This is because the CXA2610N thermal resistance (θj-a) differs according to the board, and the power consumption (P_O) is also difficult to predict with future increases in power.
  Obtain the thermal resistance (θj-a) and power consumption (P_O) of the package by the following method.

Power consumption (P_O): Oscillator ON state (OSC level = 47mAp-p)

$P_O = (I_{CC}2 + (\text{total of each input current} \times 10)) \times V_{CC} + (I_{OP} \times (V_{CC} - V_{OP}))$

$I_{CC}2$: See page 3 of this Data Sheet.
I_{OP}: Output drive current flowing from the LD0 pin to the laser diode
V_{OP}: Laser diode operating voltage

or, the power consumption can also be obtained as follows.

$P_O = (I_{CC} \times V_{CC}) - (I_{OP} \times V_{OP})$

I_{CC}: Device current consumption (including I_{OP}) during operation

Thermal resistance (θj-a) when mounted on a board

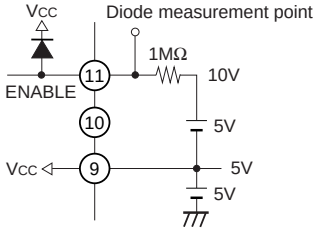
The diode temperature coefficient is –2.27mV/°C

(1) ENABLE pin voltage – V_{CC} pin voltage after applying 0V to the IINR, IIN2 and IIN3 pins = V1
(2) ENABLE pin voltage – V_{CC} pin voltage immediately after applying 3V to IINR = V2
(3) ENABLE pin voltage – V_{CC} pin voltage after applying 3V to the IINR pin and reaching a thermally balanced state = V3

The change in current consumption between (1) and (2) $\Delta I_{CC} = (3V/(Rext + 250\Omega)) \times 104$.
This ΔI_{CC} causes the ENABLE pin internal forward protective diode connection V_{CC} voltage to vary (ΔV_{CC}) due to the effects of the wiring resistance from the V_{CC} pin voltage which is used as the reference.
The voltage fall coefficient (VR) used to correct this ΔV_{CC} can be obtained by $VR = (V1 - V2)/\Delta I_{CC}$.
Using VR to apply correction to V3 yields the equation:
$(\Delta I_{CC} \times VR) + V3 = V4$.
From this, $\Delta Tj = (V4 - V2)$ mV/–2.27mV/°C, and $\theta j\text{-}a = \Delta Tj/P_O$ [°C/W].

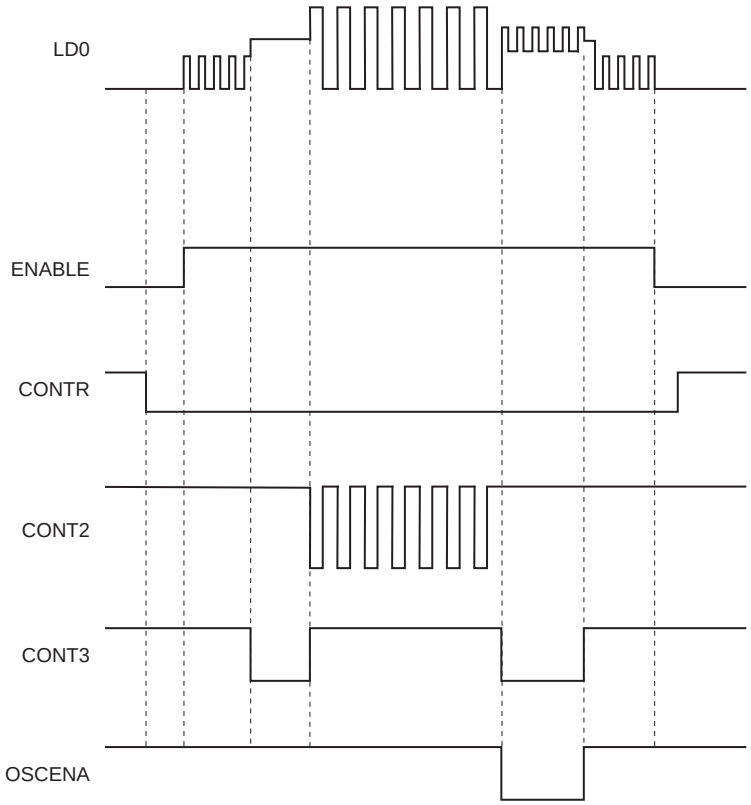
- Allowable power dissipation (P_D) ≥ P_O [W]
  P_D = (150°C – ambient temperature)/θj-a
- Maximum operating temperature 70 °C
  (150°C – ΔTj) ≥ 70°C

Thus, if θj-a can be lowered from these two conditions, the maximum operating temperature can also be raised.

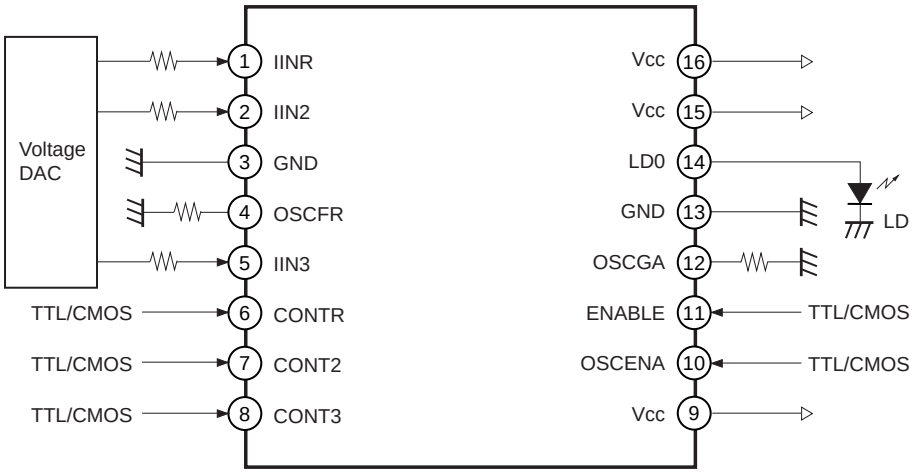


Thermal Resistance Measurement Circuit

Timing Chart



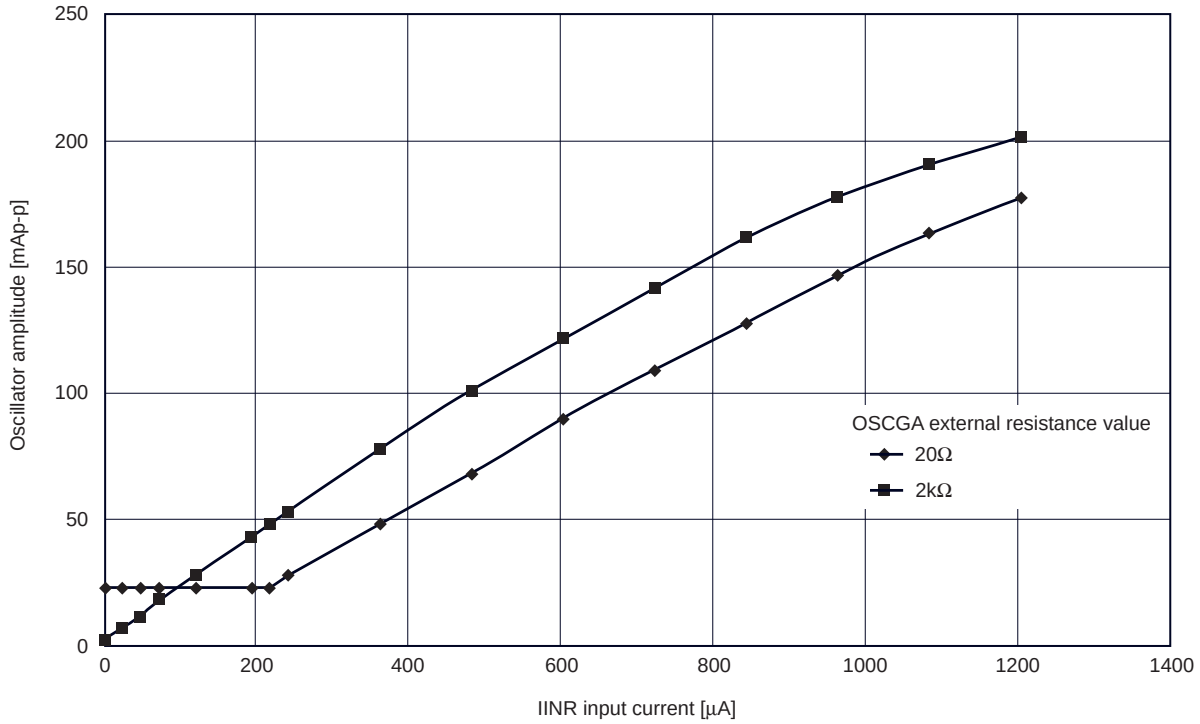
Application Circuit



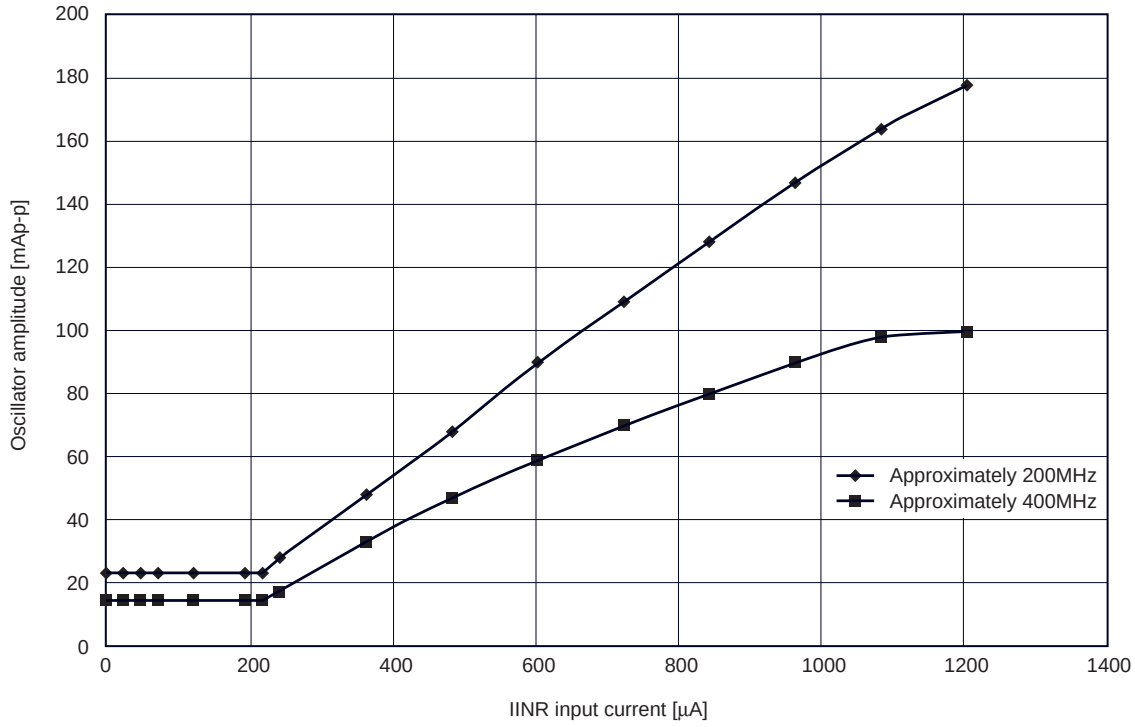
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

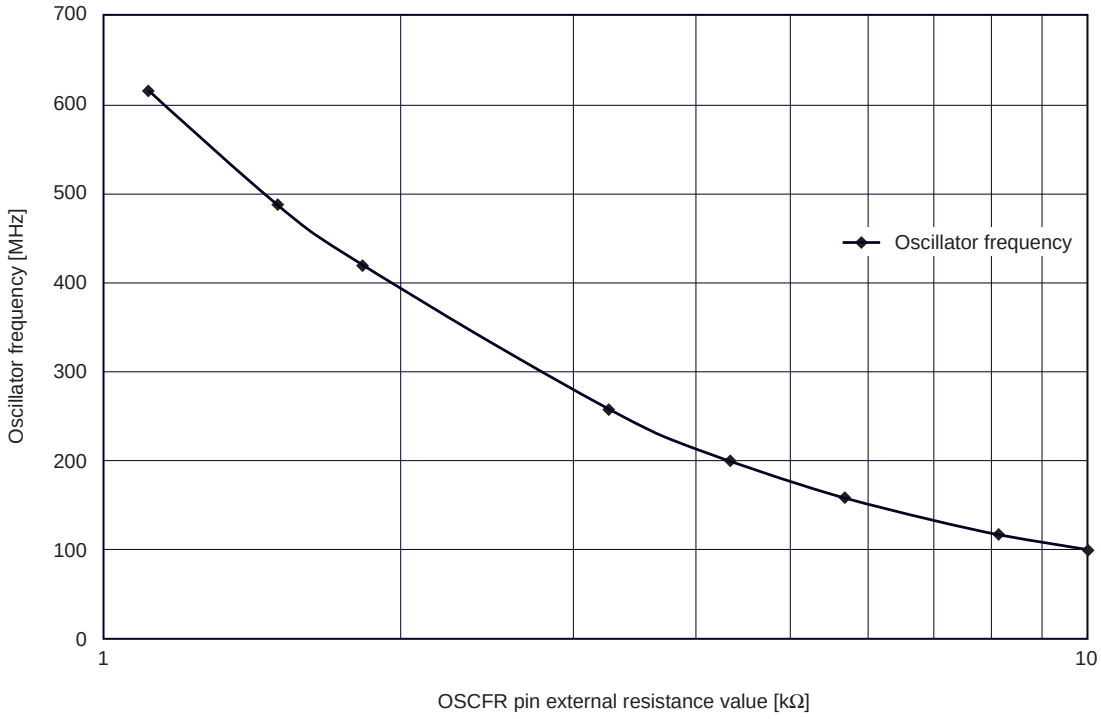
High frequency oscillator amplitude vs. Read current characteristics



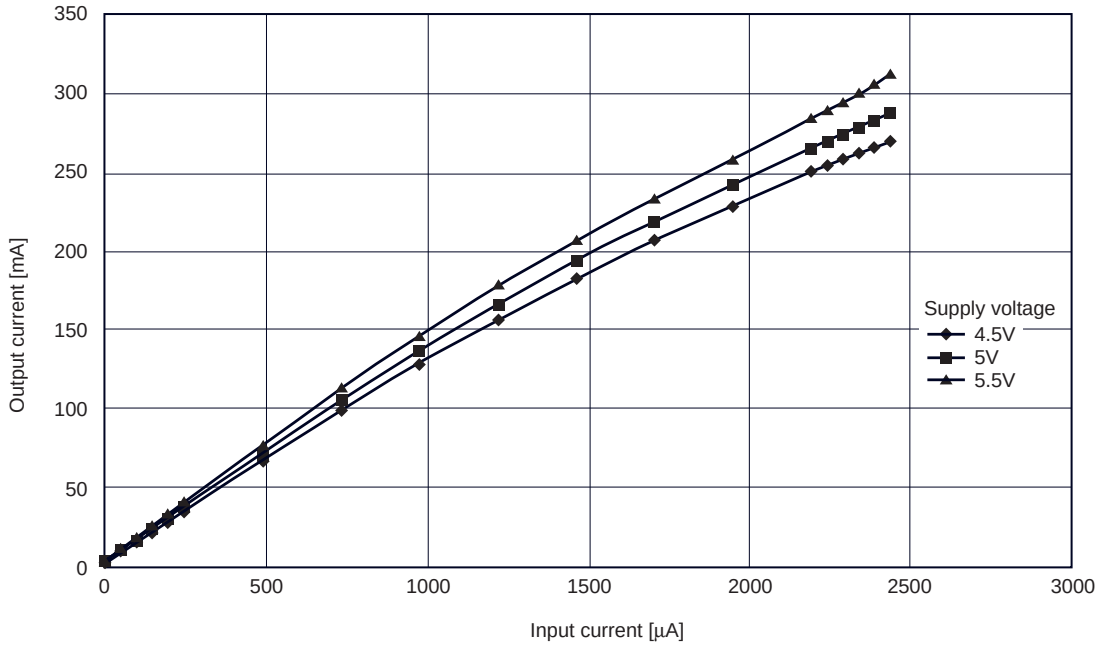
High frequency oscillator amplitude frequency dependence (OSCGA = 20Ω)



High frequency oscillator frequency vs. External resistance

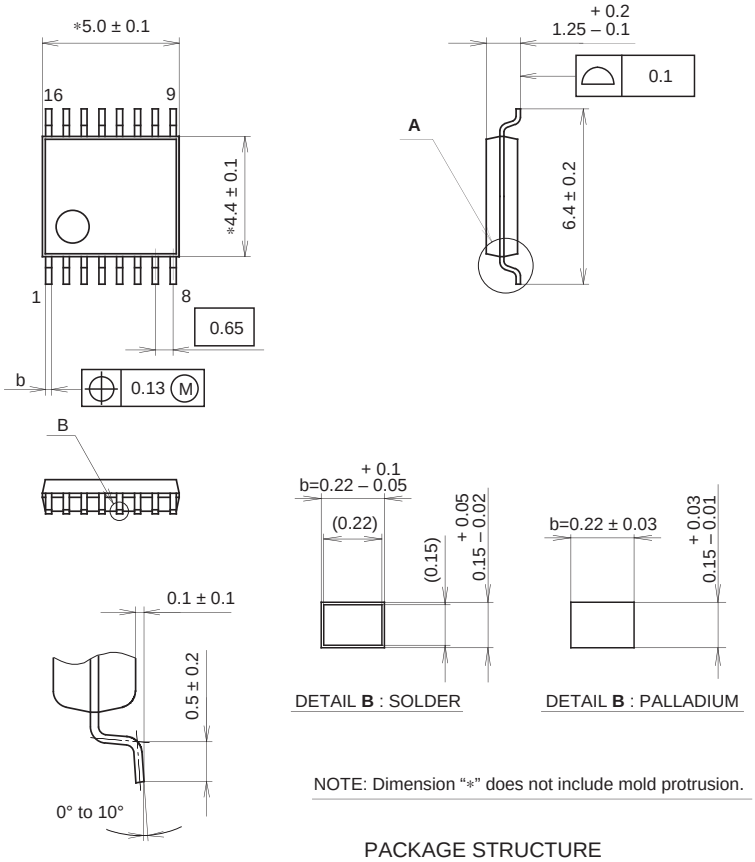


IIN3 input/output current characteristics



Package Outline Unit: mm

16PIN SSOP (PLASTIC)



DETAIL **B** : SOLDER

DETAIL **B** : PALLADIUM

DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-16P-L01
EIAJ CODE	SSOP016-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).