SONY

CXA2002R

2-channel Recording/Playback Amplifier

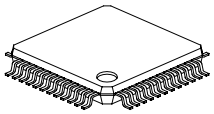
Description

The CXA2002R is a bipolar IC developed as recording/playback amplifiers for Hi8 VCRs.

Features

- Recording/playback system
  - Wideband recording/playback amplifier for Hi8 VCR
  - Supports electronic volume (EVR) control (3V)
- Recording system
  - Recording amplifier feedback dumping circuit and its EVR control function facilitates printed circuit board design.
  - Five-input (Y, chroma, AFM, ATF and PCM) mix amplifier and EVR control function of Y and low-band recording level
  - Ramp circuit for the recording amplifier output bias current
- Playback system
  - Playback amplifier feedback dumping circuit facilitates printed circuit board design.
  - Middle-band compensation circuit (middle tune) and independent adjustments of the center frequency, Q and boost by EVR
  - RFAGC and dropout detection circuits

48 pin LQFP (Plastic)



Application

8 mm VCR

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings

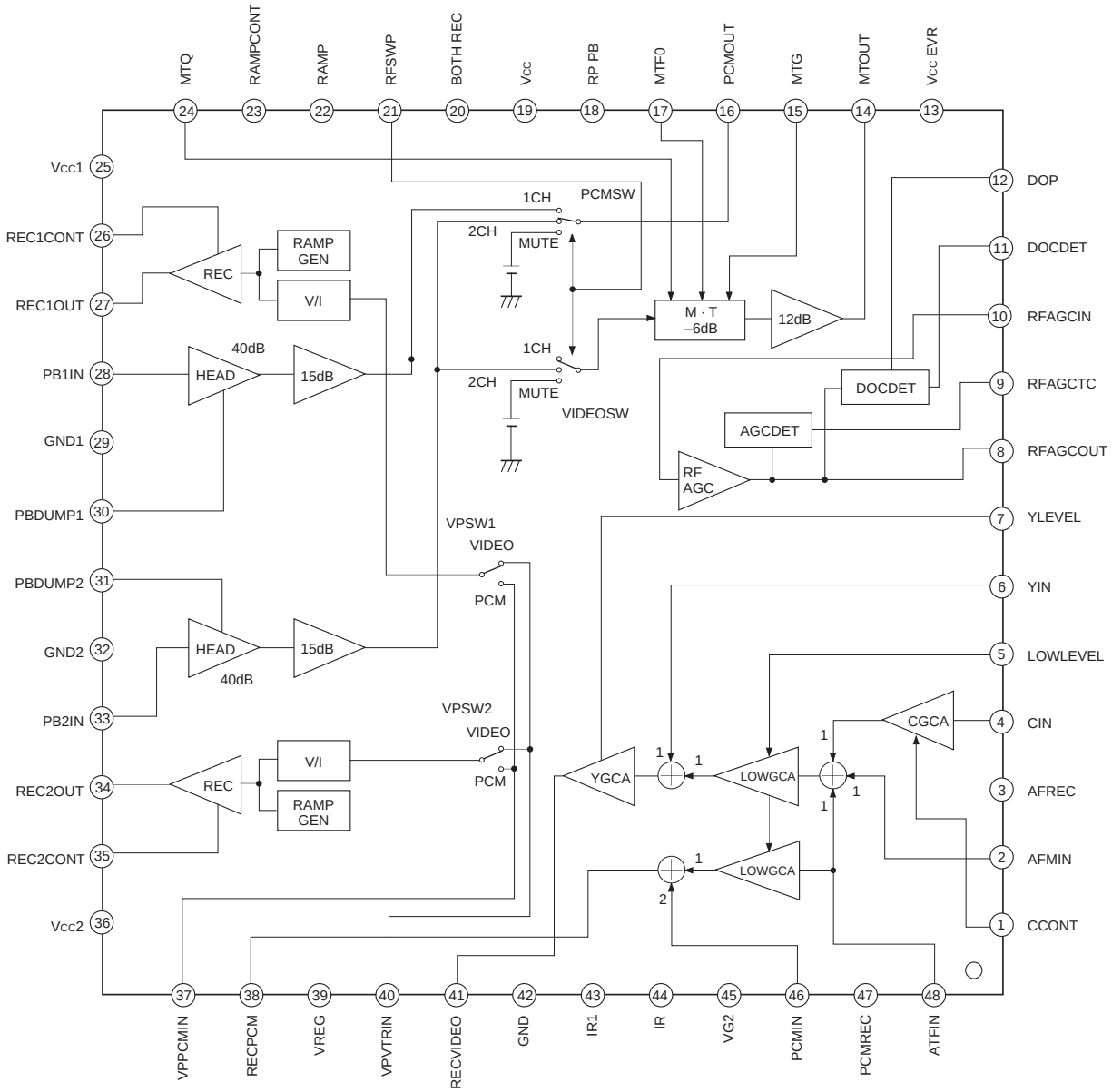
• Supply voltage	V_{CC}	7	V
• Operating temperature	Topr	–10 to +75	℃
• Storage temperature	Tstg	–65 to +150	℃
• Allowable power dissipation (when mounted on the printed circuit board)	P_D	1100	mW

Recommended Operating Condition

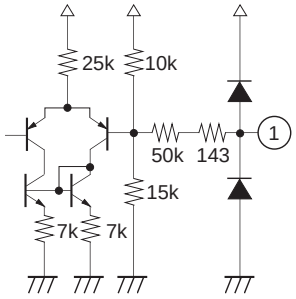
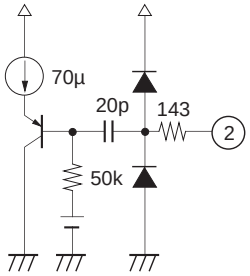
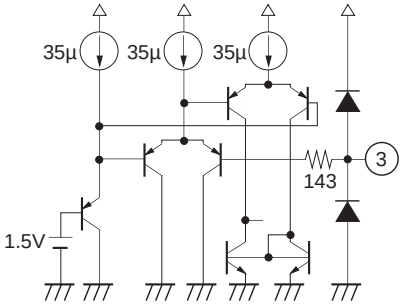
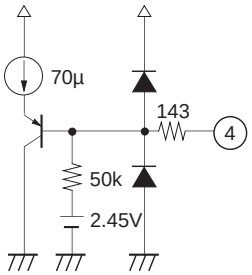
• Supply voltage	$4.75\ ^{+0.5}_{-0.25}$	V
• Vcc EVR voltage	3.15 ±0.15	V

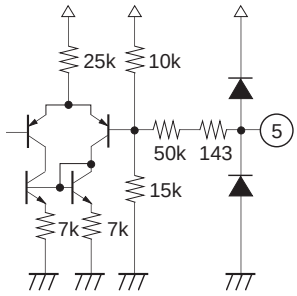
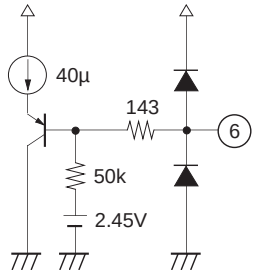
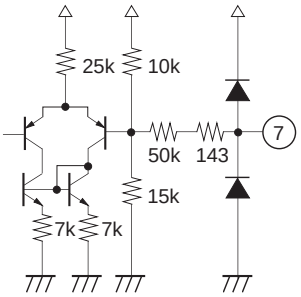
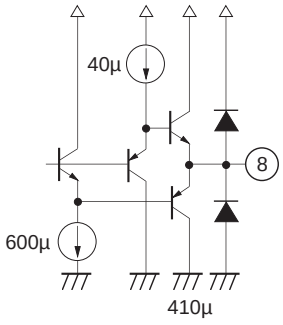
E95201-ST

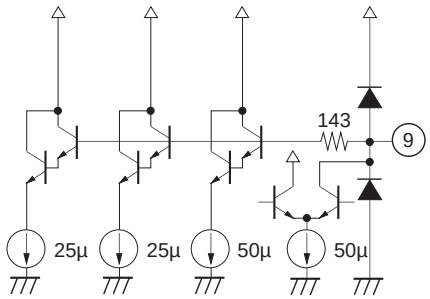
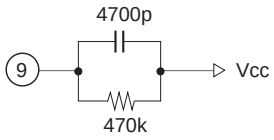
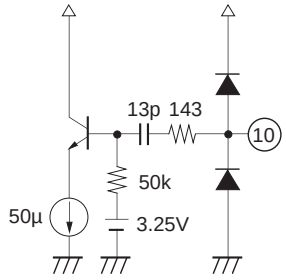
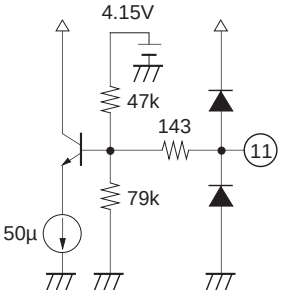
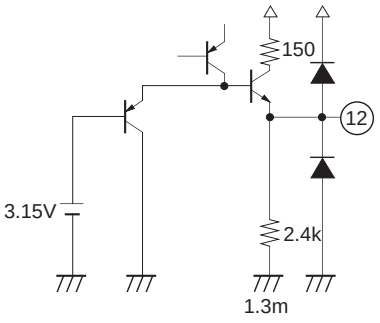
Block Diagram

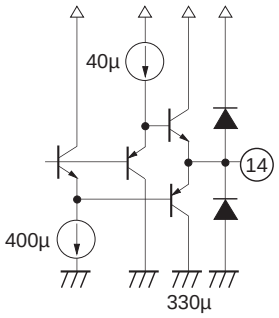
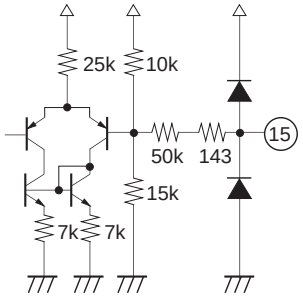
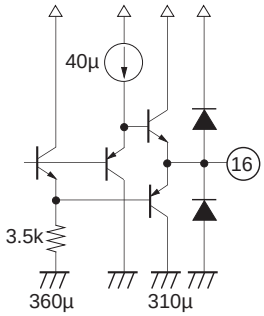
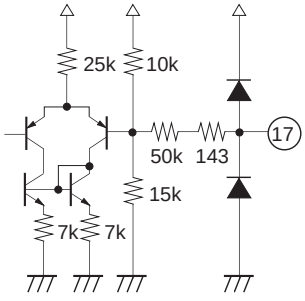


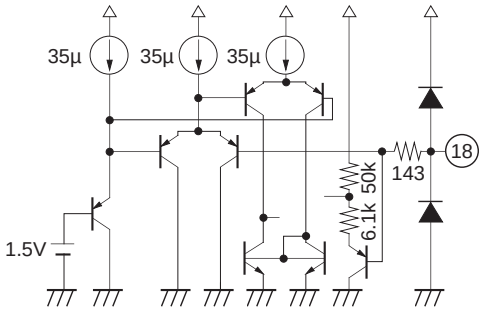
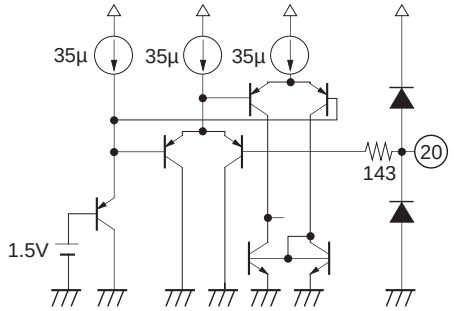
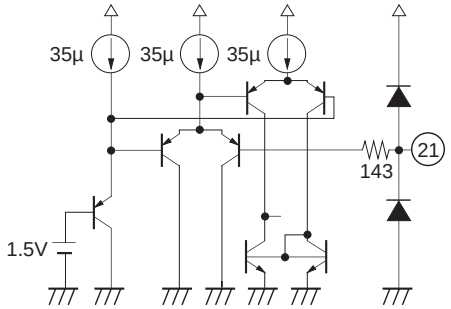
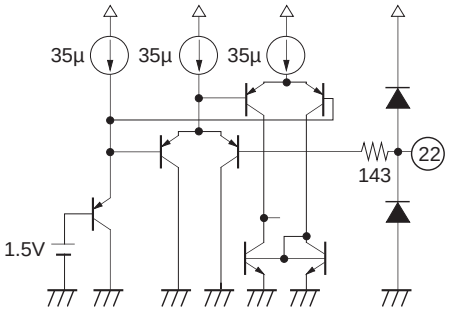
Pin Description

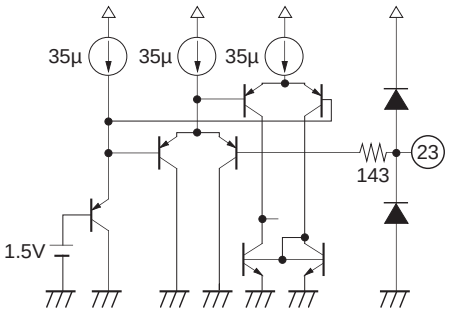
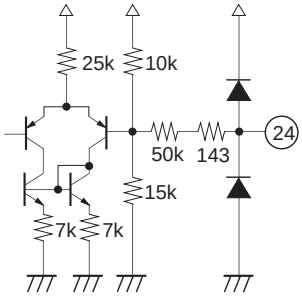
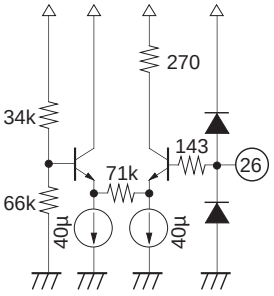
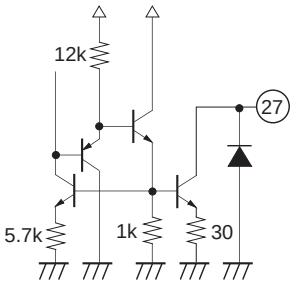
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	CCONT	—		EVR adjusting pin for the recording chroma level. Increasing the applied voltage reduces the gain.
2	AFMIN	—		Input pin for recording AFM. DC component is cut by built-in C. Input level: 125mVp-p (typ.)
3	AFREC	—		After-recording mode switchover pin (High: After-recording) H: 2.3V or above L: 0.6V or below
4	CIN	2.45		Recording chroma input pin. Input after cutting DC component with C. Input level: 300mVp-p (typ.)

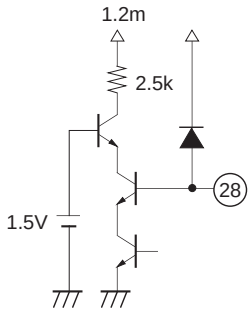
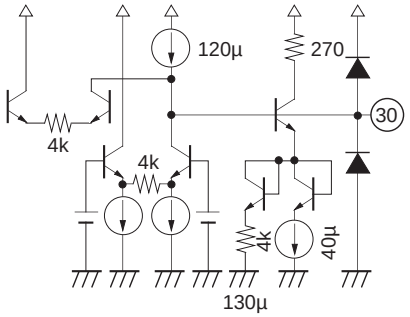
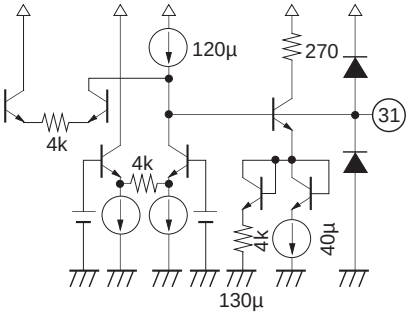
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
5	LOWLEVEL	—		EVR adjusting pin for recording RF. Increasing the applied voltage reduces the gain. Simultaneous adjustment of VIDEO and PCM paths. VIDEO path: C+AFM+ATF adjustment PCM path: ATF adjustment
6	YIN	2.45		Recording Y input pin. Input after cutting DC component with C. Input level: 500mVp-p (typ.)
7	YLEVEL	—		EVR adjusting pin for the recording Y signal level. Increasing the applied voltage reduces YLEV.
8	RFAGCOUT	2.8		Playback Y signal output pin. Output level: 410mVp-p (typ.)

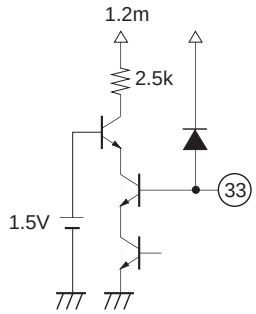
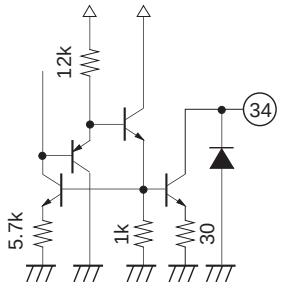
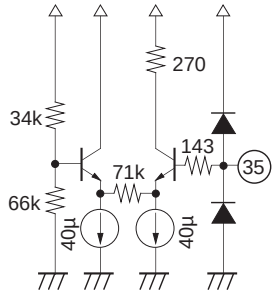
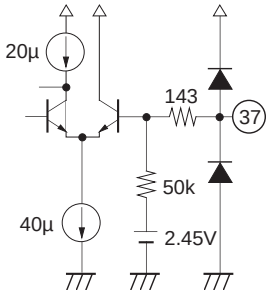
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9	RFAGCTC	—		 Pin to apply time constant of RFAGC. EVR adjustment of RFAGC gain is possible. (Adjustment range: 2.5V to 4.75V Gain: Small to Large)
10	RFAGCIN	—		RFAGC input pin for the playback Y signal. Playback VIDEO signal output to Pin 14 (MTOUT) is input again to Pin 10 (RFAGCIN) via external ATF TRAP, AFM TRAP and C TRAP. DC component is cut by built-in C.
11	DOCDET	2.5		Pin to determine the dropout detection level.
12	DOP	H: 3.15 L: 0		Output pin for the dropout detection signal. High upon dropout.

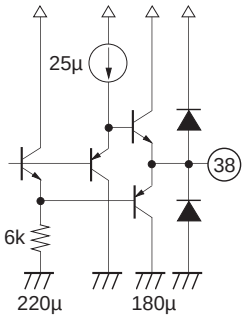
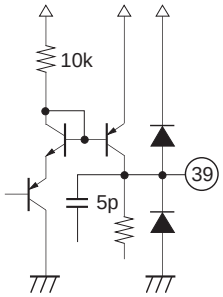
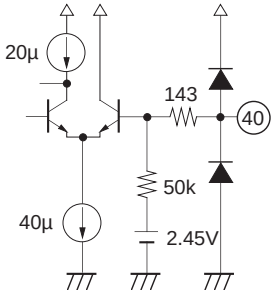
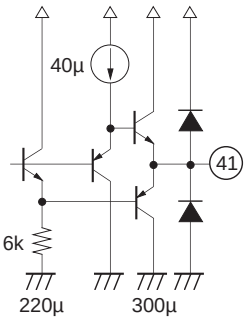
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
13	Vcc EVR	3.15		Power supply pin for EVR block.
14	MTOUT	2.4		Output pin for playback VIDEO signal. Y + C + AMF + ATF is output.
15	MTG	—		EVR adjusting pin for the middle-tune boost. Increasing the applied voltage reduces the boost.
16	PCMOUT	2		Output pin for playback PCM
17	MTF0	—		EVR adjusting pin to determine middle-tune fo. Increasing the applied voltage increases fo.

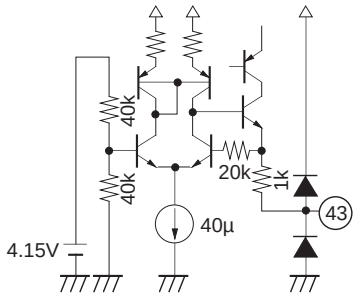
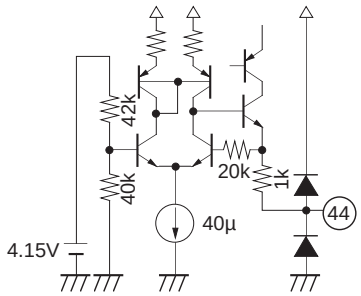
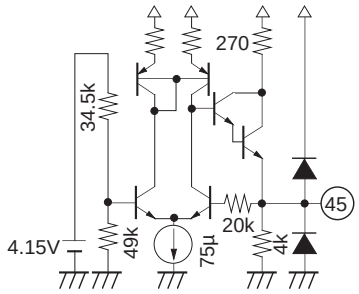
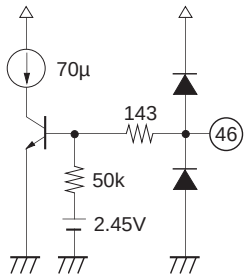
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
18	RP PB	—		REC/PB switchover pin High: PB 2.3V or above Low: REC 0.6V or below
19	V_{CC}	4.75		Power supply pin for components other than REC amplifier, PB amplifier and EVR.
20	BOTH REC	—		EACH REC/BOTH REC switchover pin. High: BOTH REC 2.3V or above Low: EACH REC 0.6V or below
21	RFSWP	—		RFSWP input pin. High: 2.3V or above Low: 0.6V or below
22	RAMP	—		Pin to turn ON/OFF the REC amplifier bias current during after-recording. The bias current turns ON when this pin goes high. High: 2.3V or above Low: 0.6V or below

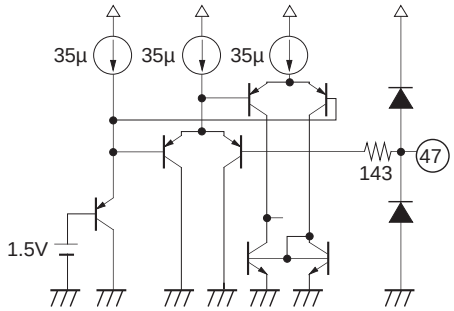
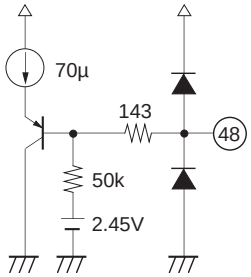
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
23	RAMPCONT	—		Ramp pulse rising slope switchover pin. Low: 32µA/µs 0.6V or below High: 17µA/µs 2.3V or above (The fall time is 32µA/µs in both cases.)
24	MTQ	—		EVR adjusting pin to determine middle-tune Q. Increasing the applied voltage increases Q.
25	Vcc1	4.75		Power supply pin for CH1 REC amplifier and PB amplifier.
26	REC1CONT	—		EVR adjusting pin for the CH1 recording dumping level. Reducing the applied voltage strengthens dumping.
27	REC1OUT	—		CH1 recording output pin. Open collector.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
28	PB1IN	0.7		CH1 playback input pin.
29	GND1	0		GND pin for CH1 REC amplifier and PB amplifier.
30	PBDUMP1	2.5		Pin to determine the dumping of CH1 playback by external resistance. Increasing resistance strengthens dumping.
31	PBDUMP2	2.5		Pin to determine the dumping level of CH2 playback by external resistance. Increasing resistance strengthens dumping.
32	GND2	0		GND pin for CH2 REC amplifier and PB amplifier.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
33	PB2IN	0.7		CH2 playback input pin.
34	REC2OUT	—		CH2 recording output pin. Open collector.
35	REC2CONT	—		EVR adjusting pin for the CH2 recording dumping. Reducing the applied voltage strengthens dumping.
36	Vcc2	4.75		Power supply pin for CH2 REC amplifier and PB amplifier.
37	VPPCMIN	2.45		VPSW input pin for recording PCM path. The Pin 38 signal is input after cutting its DC component with external C.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
38	RECPCM	2.4		Output pin for the recording PCM path. The recording PCM signal and the recording ATF signal are mixed and output.
39	VREG	4.15		4.15V regulator output pin.
40	VPVTRIN	2.45		VPSW input pin for the recording VIDEO path. The Pin 41 signal is input after cutting its DC component with external C.
41	RECVIDEO	2.4		Output pin for the recording VIDEO path. The recording (Y + C + AFM + ATF) mix signal is output.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
42	GND	0		GND pin for all components other than REC amplifier and PB amplifier.
43	IR1	1.9		Pin to determine REC amplifier gain. The reference current is produced by connecting 15kΩ between this pin and GND.
44	IR	1.9		Pin to produce the reference current for the middle tune, dropout detector and ramp. Connect 18kΩ between this pin and GND.
45	VG2	2.45		2.45V internal reference voltage source.
46	PCMIN	2.45		Recording PCM input pin. Input after cutting DC component with C. Input level: 300mVp-p (typ.)

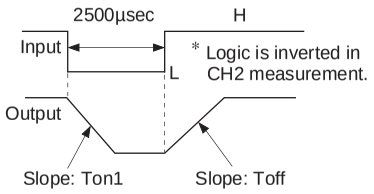
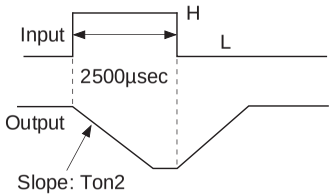
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
47	PCMREC	—		PCM recording switchover pin. PCM recording is performed when this pin goes high. High: 2.3V or above Low: 0.6V or below
48	ATFIN	2.45		Recording ATF input pin. Input after cutting DC component with C. Input level: 125mVp-p (typ.)

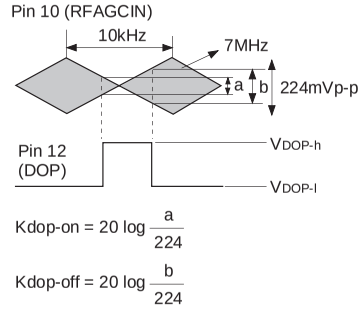
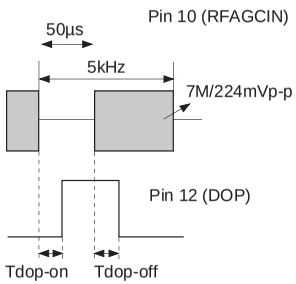
Electrical Characteristics

* See the Control Logic Truth Table for control logic conditions. (Vcc = 4.75V, VccEVR = 3.15V, Ta = 25°C. See the Electrical Characteristics Measurement Circuit.)

No.	Item	Symbol	Measurement conditions				Measure-ment point, ammeter name	Measurement method	Min.	Typ.	Max.	Unit
			Input condition			Control logic						
			Input pin	Level	Fre-quency							
1	Current consumption for recording	I_{REC}	—	—	—	A	IVCC1+ IVCC2	IC internal consumption current (including REC amplifier output bias current) during switched recording.	33	47	61	mA
2	Current consumption for playback	I_{PB}	—	—	—	G	IVCC1+ IVCC2	IC internal current during playback.	26	37	48	mA
3	Current consumption for after-recording	I_{AFREC}	—	—	—	I	IVCC1+ IVCC2	IC internal current (including REC amplifier output bias current) during after-recording.	45	64	83	mA
4	VREG pin voltage	V_{REG}	—	—	—	A	39	Measure the pin voltage.	3.95	4.15	4.35	V
5	VG2 pin voltage	V_{G2}	—	—	—	A	45	Measure the pin voltage.	2.30	2.45	2.60	V
	Recording system											
6	Y signal GCA min. gain	G_{Ymin}	6	500mVpp	300kHz	A	41	Pin 7 (YLEVEL) = 3.15V	—	–23.2	–14.1	dB
7	Y signal GCA center gain	G_{Ycen}	6	500mVpp	300kHz	A	41	Adjust Pin 7 (YLEVEL) so that Pin 41 (RECVIDEO) output level becomes 200mVp-p → V_{YLEV}	—	–8.0	—	dB
8	Y signal GCA max. gain	G_{Ymax}	6	200mVpp	300kHz	A	41	Pin 7 (YLEVEL) = 0.0V	–3.6	–1.3	—	dB
9	Y signal GCA frequency response (center gain)	V_{FY}	6	500mVpp	14MHz, 300kHz	A	41	14MHz level/300kHz level Pin 7 (YLEVEL) = V_{YLEV}	–1.5	–0.5	+0.5	dB
10	Y signal GCA secondary distortion (center gain)	D_Y	6	500mVpp	7MHz	A	41	Pin 7 (YLEVEL) = V_{YLEV}	—	–55	—	dB
11	Low-band signal GCA (VIDEO path) min. gain	G_{Ivmin}	2	125mVpp	1.7MHz	A	41	Pin 5 (LOWLEVEL) = 3.15V Pin 7 (YLEVEL) = VYLEV	—	–30.4	–26.0	dB
12	Low-band signal GCA (VIDEO path) center gain	G_{Ivcen}	2	125mVpp	1.7MHz	A	41	Adjust Pin 5 (LOWLEVEL) so that Pin 41 (RECVIDEO) output level becomes 12.5mVp-p → V_{ILEV} Pin 7 (YLEVEL) = V_{YLEV}	—	–20	—	dB
13	Low-band signal GCA (VIDEO path) max. gain	G_{Ivmax}	2	125mVpp	1.7MHz	A	41	Pin 5 (LOWLEVEL) = 0.0V Pin 7 (YLEVEL) = V_{YLEV}	–14.0	–11.6	—	dB
14	AFM path secondary distortion	D_{AFM}	2	125mVpp	1.7MHz	A	41	Pin 5 (LOWLEVEL) = 0.0V Pin 7 (YLEVEL) = V_{YLEV}	—	–55	—	dB

No.	Item		Symbol	Measurement conditions				Measure-ment point, ammeter name	Measurement method	Min.	Typ.	Max.	Unit
				Input condition			Control logic						
				Input pin	Level	Fre-quency							
15	ATF (VIDEO path) max. gain		GVATF	48	125mVpp	100kHz	A	41	Pin 5 (LOWLEVEL) = 0.0V Pin 7 (YLEVEL) = VYLEV	–14.0	–11.6	—	dB
16	ATF (PCM path) min. gain		GPATF1	48	125mVpp	100kHz	A	38	Pin 5 (LOWLEVEL) = 3.15V	—	–30.7	–26.0	dB
17	ATF (PCM path) max. gain		GPATF2	48	125mVpp	100kHz	A	38	Pin 5 (LOWLEVEL) = 0.0V	–14.0	–11.9	—	dB
18	Chroma signal GCA min. gain		Gcmin	4	300mVpp	300kHz	A	41	Pin 5 (LOWLEVEL) = VILEV Pin 7 (YLEVEL) = VYLEV Pin 1 (CCONT) = 3.15V	—	–26.4	–21.6	dB
19	Chroma signal GCA center gain		Gccen	4	300mVpp	300kHz	A	41	Adjust Pin 1 (CCONT) so that Pin 41 (RECVIDEO) output level becomes 50mVp-p→VCLEV Pin 5 (LOWLEVEL) = VILEV Pin 7 (YLEVEL) = VYLEV	—	–15.6	—	dB
20	Chroma signal GCA max. gain		Gcmax	4	300mVpp	300kHz	A	41	Pin 5 (LOWLEVEL) = VILEV Pin 7 (YLEVEL) = VYLEV Pin 1 (CCONT) = 0.0V	–13.3	–10.5	—	dB
21	Chroma signal GCA frequency response (center gain)		VFC	4	300mVpp	2MHz 300kHz	A	41	Pin 5 (LOWLEVEL) = VILEV Pin 7 (YLEVEL) = VYLEV Pin 1 (CCONT) = VCLEV 2MHz level/300kHz level	–0.5	0	+0.5	dB
22	Chroma signal GCA secondary distortion (center gain)		DC	4	300mVpp	750kHz	A	41	Pin 5 (LOWLEVEL) = VILEV Pin 7 (YLEVEL) = VYLEV Pin 1 (CCONT) = VCLEV	—	–50	—	dB
23	PCM signal path gain		GP	46	300mVpp	300kHz	A	38		–4.5	–3.7	–2.9	dB
24	PCM signal path frequency response		VFP	46	300mVpp	14MHz 300kHz	A	38	14MHz gain/300kHz gain	–0.8	0.0	+0.8	dB
25	PCM signal path secondary distortion		DP	46	300mVpp	7MHz	A	38		—	–55	—	dB
26	REC amplifier output bias current	1ch	IB1	—	—	—	B	IB1	Measure DC currents. Pin 26 (REC1CONT), Pin 35 (REC2CONT) = 3.3V	14.55	18.8	23.05	mA
		2ch	IB2				A	IB2					

No.	Item		Symbol	Measurement conditions				Measure-ment point, ammeter name	Measurement method	Min.	Typ.	Max.	Unit
				Input condition			Control logic						
				Input pin	Level	Fre-quency							
27	REC amplifier output current	1ch	I_{R1}	40	200mVpp	1MHz	B	27	Pin 26 (REC1CONT), Pin 35 (REC2CONT) = 3.3V Output level (Vp-p)/51 (Ω)	18.1	20.7	23.3	mApp
		2ch	I_{R2}				A	34					
28	REC amplifier frequency response	1ch	V_{FR1}	40	200mVpp	10MHz 1MHz	B	27	10MHz level/1MHz level	—	–0.2	—	dB
		2ch	V_{FR2}				A	34					
29	Ramp rising slope 1	1ch	Ton1	21	See the Measurement method.		B	27		—	32	—	µA/µs
		2ch					A	34					
30	Ramp falling slope	1ch	Toff				B	27		—	32	—	µA/µs
		2ch					A	34					
31	Ramp rising slope 2	1ch	Ton2	22	See the Measurement method.		K	27		—	17	—	µA/µs
		2ch					H	34					
	Playback system												
32	Head amplifier MTOUT gain	1ch	G_{V1}	28	200µVpp	300kHz	H	14	Pin 15 (MTG) = 3.15V	58.0	61.5	65.0	dB
		2ch	G_{V2}	33			G						
33	Head amplifier PCMOUT gain	1ch	G_{P1}	28	200µVpp	300kHz	G	16		57.7	61.2	64.7	dB
		2ch	G_{P2}	33			H						
34	RFAGC standard output		V_{AGC1}	10	224mVpp	7MHz	G	8	Measure the output level, applying a time constant to Pin 9 (RFAGCTC).	340	410	480	mVpp
35	RFAGC cover-range high		V_{AGC2}	10	56mVpp	7MHz	G	8		315	380	—	mVpp
36	RFAGC cover-range low		V_{AGC3}	10	896mVpp	7MHz	G	8		—	420	490	mVpp

No.	Item	Symbol	Measurement conditions			Measure-ment point, ammeter name	Measurement method	Min.	Typ.	Max.	Unit
			Input condition								
			Input pin	Level	Fre-quency	Control logic					
37	Dropout detection ON level	Kdop-on	See the Measurement method (figure to the right).			G	12	Apply a time constant to Pin 9 (RFAGCTC).  $Kdop\text{-}on = 20 \log \frac{a}{224}$ $Kdop\text{-}off = 20 \log \frac{b}{224}$	–15.0	–12.0	–9.0	dB
38	Dropout detection OFF level	Kdop-off				G	12		–9.5	–6.5	–3.5	
39	Dropout pulse low level	Vdop-l				G	12		0	0.01	0.2	V
40	Dropout pulse high level	Vdop-h				G	12		2.9	3.15	3.4	
41	Dropout ON detection time	Tdop-on	See the Measurement method (figure to the right).			G	12		—	1.1	—	µs
42	Dropout OFF detection time	Tdop-off				G	12		—	2	—	

Control Logic Truth Table

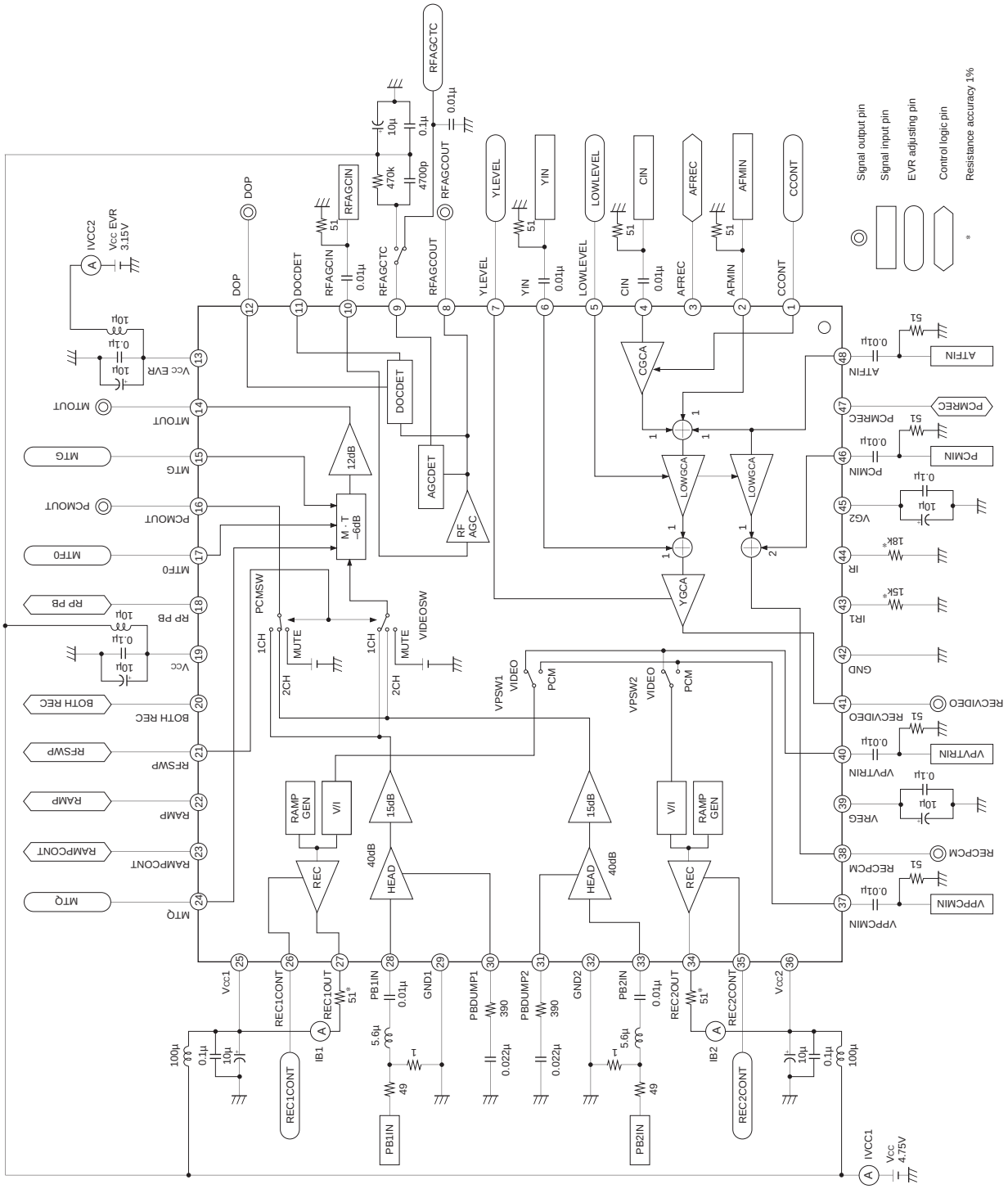
Input condition and operation / Control logic conditions	Control logic input condition							Operation of each section under respective input condition										Operation	Mode
								Recording				Playback							
	18 RP PB	20 BOTH REC	21 RFSWP	22 RAMP	23 RAMPCONT	47 PCMREC	3 AFREC	41 RECVIDEO	38 RECPCM	27 REC1OUT	34 REC2OUT	PB1chAmp	PB2chAmp	16 PCMOUT	14 MTOUT	8 RFAGCOUT	Dropout detector		
A	L	L	L	L	L	L	L	V	*	Δ	V	x	x	x	x	x	x	VIDEO EACH REC	REC
B	L	L	H	L	L	L	L	V	*	V	Δ	x	x	x	x	x	x	↓	
C	L	H	L	L	L	L	L	V	*	V	V	x	x	x	x	x	x	VIDEO BOTH REC	
D	L	H	H	L	L	L	L	V	*	V	V	x	x	x	x	x	x	↓	
E	L	H	L	L	L	H	L	V	P	P	V	x	x	x	x	x	x	PCM REC	
F	L	H	H	L	L	H	L	V	P	V	P	x	x	x	x	x	x	↓	
G	H	L	L	L	—	L	L	x	x	x	x	O	O	CH1	CH2	O	O	PB	PB
H	H	L	H	L	—	L	L	x	x	x	x	O	O	CH2	CH1	O	O	↓	
I	H	L	L	H	L	H	H	x	P	P	x	x	O	Mute	Mute	Hold	O	After-recording	PCM after-recording
J	H	L	H	H	L	H	H	x	P	x	P	O	x	Mute	Mute	Hold	O	↓	
K	H	L	L	H	H	H	H	x	P	P	x	x	O	Mute	Mute	Hold	O	↓	
H	H	L	H	H	H	H	H	x	P	x	P	O	x	Mute	Mute	Hold	O	↓	

After-recording mode RAMPCONT = L : Recording bias current rising slope 32µA/µs (typ.)
RAMPCONT = H : Recording bias current falling slope 17µA/µs (typ.)

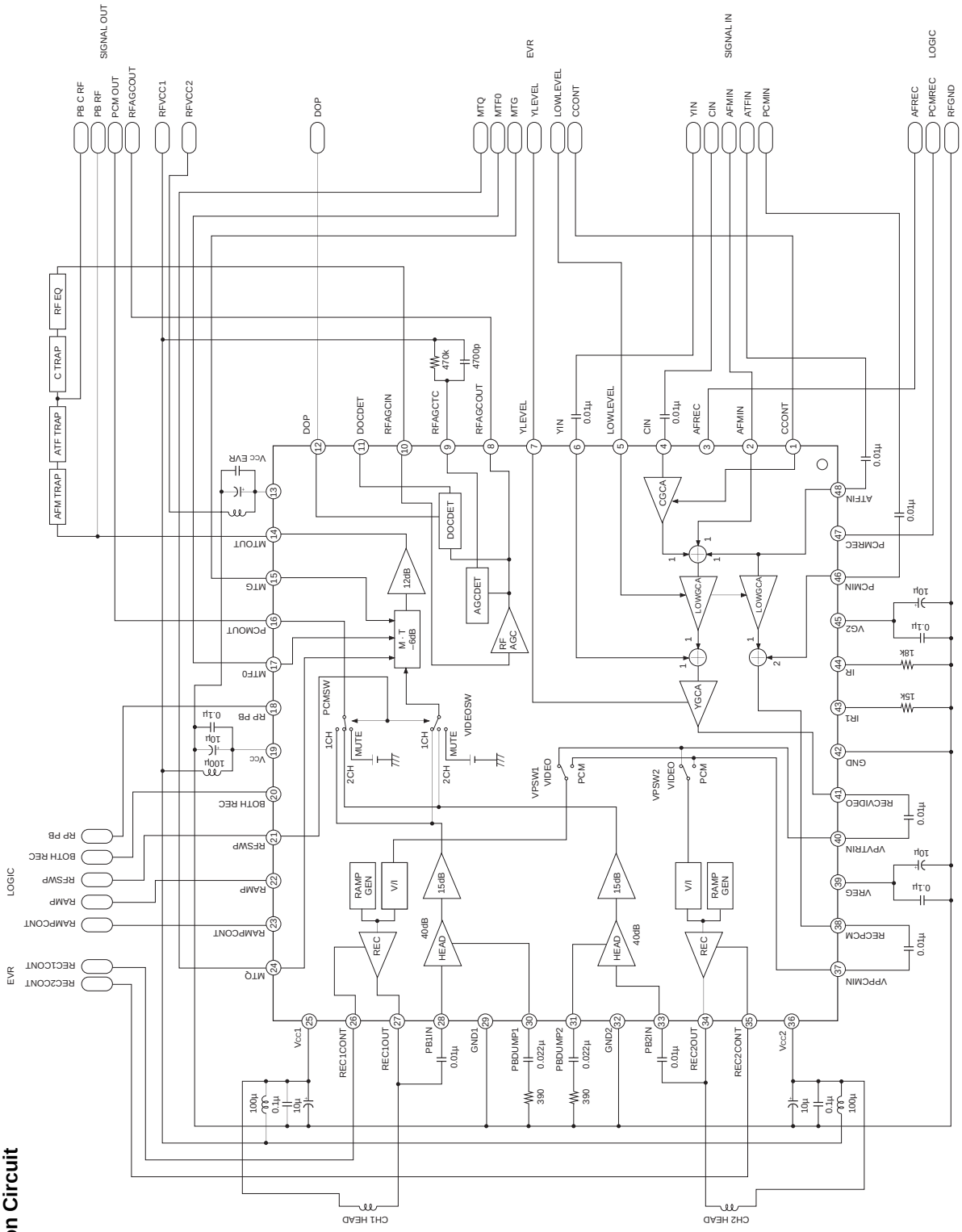
(Description of input conditions)
H : Control logic input voltage 2.3V or above
L : Control logic input voltage 0.6V or below
— : Indenpendent of H and L

(Description of operation mode)
O : Operating
x : Not operating
V : Video signal is selected.
P : PCM signal is selected.
CH1 : CH1 signal is output.
CH2 : CH2 signal is output.
* : Operating with no signal output
Δ : Operating with bias current turned off
Mute : Signal is muted.
Hold : Time constant is kept on hold.

Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

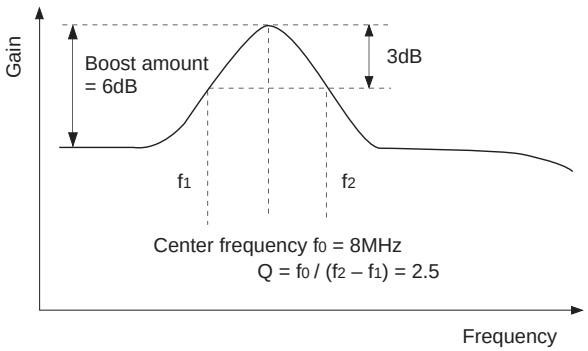
Description of Operation

<Mix amplifier + recording level adjustment>
Y, chroma, AFM, ATF and PCM signals are input at specified levels so that they are mixed internally to achive an appropriate current value at the head. The VIDEO path signal (Y + chroma + AFM + ATF) is output to Pin 41 (RECVIDEO) and the PCM path signal (PCM + ATF) to Pin 38 (RECPCM). The Y level is EVR-adjusted at Pin 8 (YLEVEL) and the low band (chroma, AFM, ATF) level at Pin 5 (LOWLEVEL). The low-band levels of the video path and the PCM path are interlocked in adjustment.

<SW + recording amplifier>
The VIDEO path signal and the PCM path signal, which underwent recording level adjustment, are switched at a correct timing, then converted to a current to drive the head.
A feedback dumping circuit is incorporated to inhibit head resonance, and the peaking can be adjusted by EVR at Pin 26 (REC1CONT), Pin 35 (REC2CONT).
During recording, the output capacitance is about 12pF including that of the head amplifier.

<Head amplifier>
The playback signal from the head is amplified with low noise and high gain. A feedback dumping circuit is incorporated to inhibit head resonance, and the peaking can be adjusted by external resistors connected to Pin 30 (PBDUMP1), Pin 31 (PBDUMP2).
During playback, the input capacitance is about 20pF including that of the recording amplifier.

<SW + middle tune>
This section switches the playback signals of CH1 and CH2 at the correct timing and outputs the playback VIDEO signal to Pin 14 (MTOUT) and the playback PCM signal to Pin 16 (PCMOUT). In the PCM after-recording mode, both playback VIDEO signal and playback PCM signal are muted during the PCM recording period.
The middle tune circuit corrects the frequency response of the playback VIDEO signal.
The center frequency can be adjusted by EVR at Pin 17 (MTF0), Q at Pin 24 (MTQ) and the boost at Pin 15 (MTG).
The figure to the right shows the center condition that sets f_0 = 8MHz, Q = 2.5 and the boost = 6dB. Each control characteristics shown in "Example of Representative Characteristics" is obtained when two of them are fixed to the center condition.



<RFAGC>
This circuit inputs the playback Y signal separated from the playback VIDEO signal using an external circuit and outputs it at a constant level of 410mVp-p. In the PCM after-recording mode, RFAGC gain is kept unchanged during PCM recording period.

<Dropout detection>
A dropout is detected in the playback Y signal, and a dropout pulse is output. The detection level is optimized using 224mVp-p input as a reference. If necessary, the detection level can be adjusted by inputting a DC voltage to Pin 11 (DOCDET). To make this adjustment, input a voltahe proportional to the output voltage of Pin 39 (VREG).

<Control logic block>
This IC exercises power-saving control of circuit blocks which are not in immediate need for operation. The IC also incorporates a logic circuit for controlling a number of SWs which change inputs and outputs at complicated timing.
The combinations of input and output in the basic operation are shown in the "Control Logic Truth Table".

<Reference voltage in the IC>
VG2 2.45V and VREG 4.15V are generated as a reference voltages used in the IC.
VG2 cannot be used outside the IC. VREG cannot also be used outside the IC except for adjusting the dropout detection level at Pin 11 (DOCDET).

Notes on Operation

1. This IC is characterized by high-voltage gain (about 61dB in the playback system). Pay attention to the following when using the IC.

   1) Use reinforced power supply and ground lines. Decouple the power supply pin with a coil and a capacitor. Connect the decoupling capacitor as close to the pin as possible.
   2) Use of a regulator power supply is recommended.
   3) Connecting a capacitive load to the output may cause oscillation.
   4) Take particular care not to make capacitive coupling between the head amplifier input and the playback output. Also be careful not to make capacitive coupling between the recording input and the recording amplifier output.
   5) Use of decoupling capacitors is recommended between the following DC voltage input pins and GND. When the control voltage source is at high impedance, aggravation of cross talk or oscillation is feared to occur.
      Pin 1 (CCONT), Pin 5 (LOWLEVEL), Pin 7 (YLEVEL)
      Pin 9 (RFAGCTC) [not when time constant is connected], Pin 11 (DOCDET)
      Pin 17 (MTF0), Pin 24 (MTQ), Pin 26 (REC1CONT)
      Pin 35 (REC2CONT)

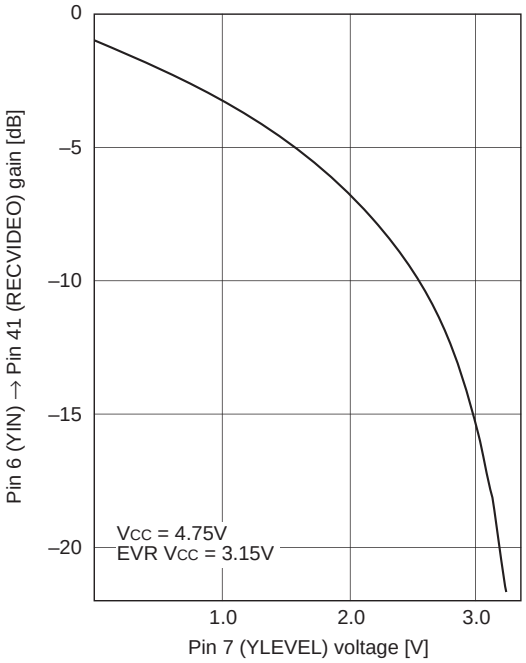
   6) When a decoupling capacitor is necessary for other pins (not power supply pin), it is recommended to connect each decoupling capacitor as close as to the pin as possible.

2. When Pin 13 (EVR Vcc) is used for 5V system ($4.75\ ^{+0.5V}_{-0.25V}$), the voltage of Pin 19 (Vcc) should be equal to or larger than that of Pin 13 (EVR Vcc).

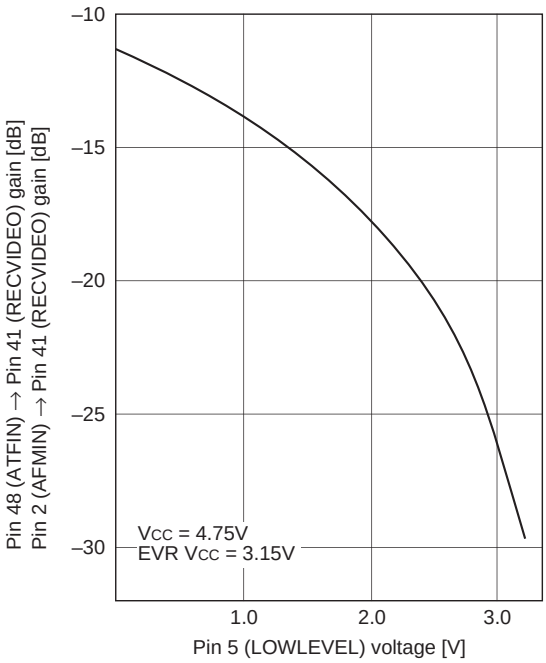
3. The voltage input to the EVR adjusting pin should be proportional to the EVR Vcc voltage. Control the input voltage in the range from 0V to 3.15V when EVR Vcc = 3.15V.
   For EVR adjustment at Pin 26 (REC1CONT) and Pin 35 (REC2CONT), control the input voltage in the range from 1.8V to 4.75V when Vcc = 4.75V, in proportion to the supply voltage Vcc; at Pin 9 (RFAGCTC), control the input voltage in the range from 2.5V to 4.75V.

Example of Representative Characteristics

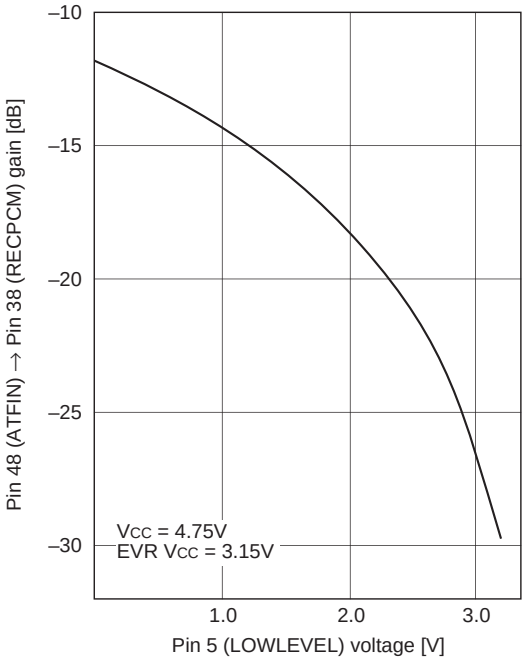
YGCA gain control



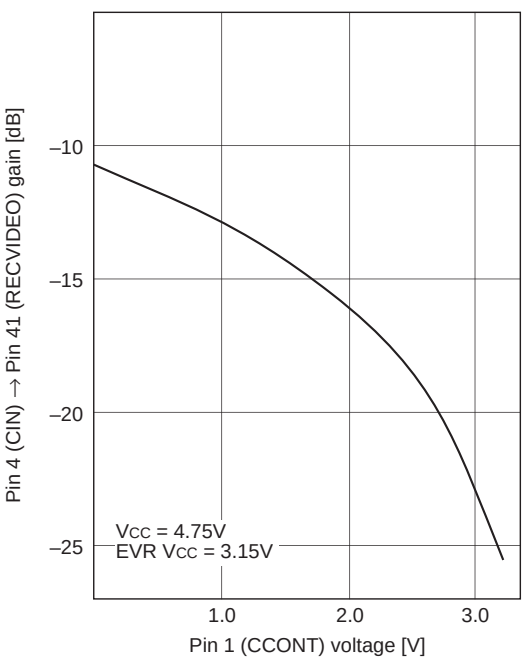
LOWGCA (VIDEO path) gain control



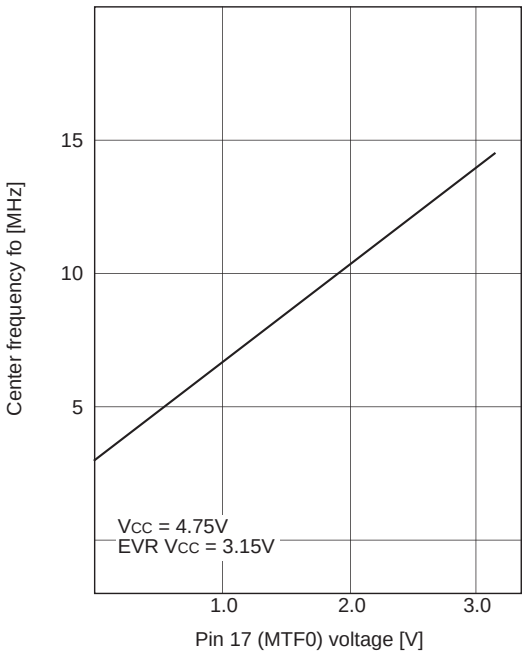
LOWGCA (PCM path) gain control



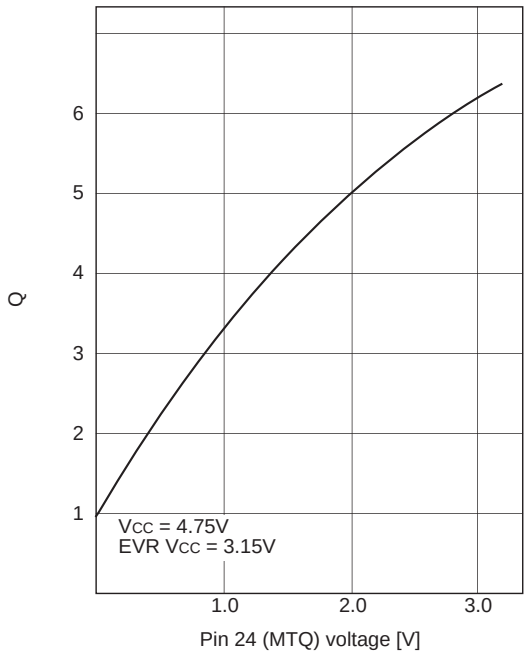
CGCA gain control



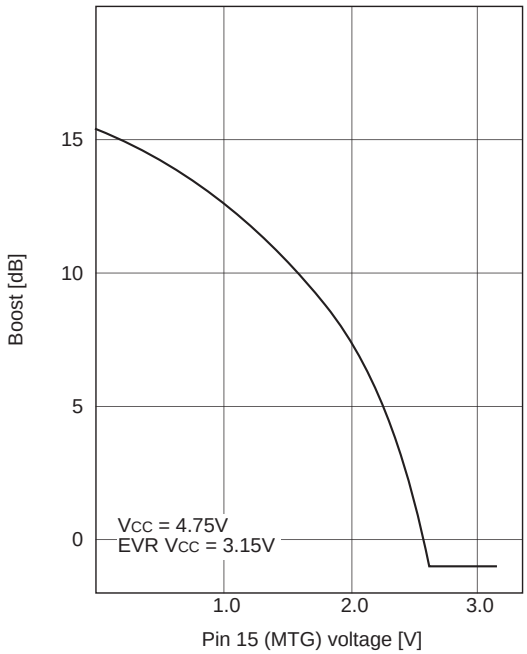
Middle tune fo control



Middle tune Q control

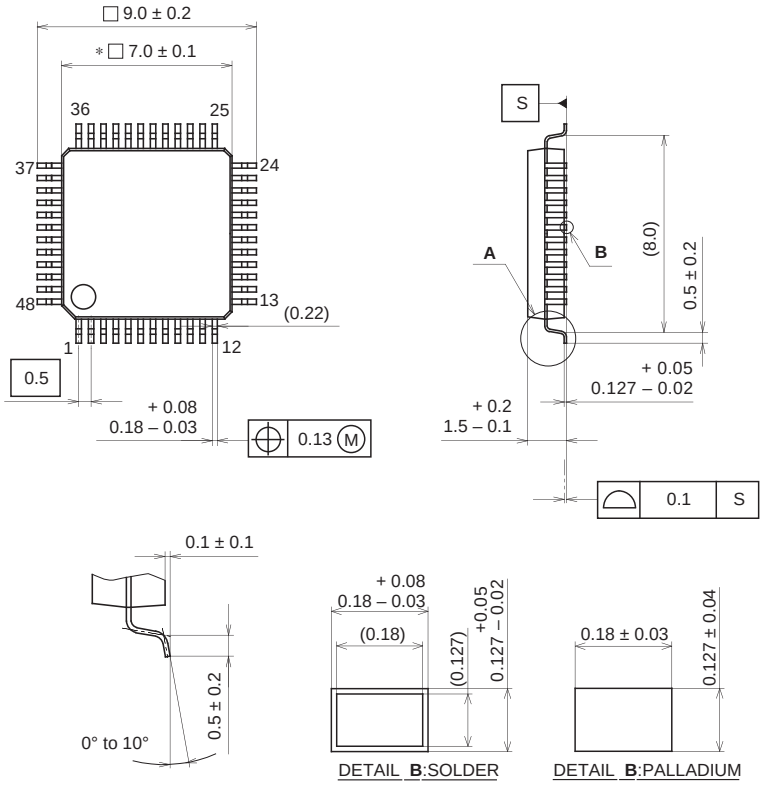


Middle tune boost control



Package Outline Unit : mm

48PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g