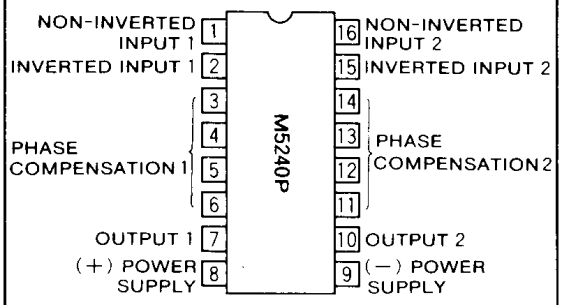
M5240P

DUAL LOW-NOISE J-FET INPUT OPERATIONAL AMPLIFIERS

DESCRIPTION

The M5240P is a semiconductor integrated circuit designed as a low-noise Bi-FET operational amplifier which adopts J-FETs in the input stage. The device comes in a 16-pin DIP and contains two circuits for yielding high sound quality, high input impedance, high slew rate and low distortion characteristics. It can be widely used as an operational amplifier in stereo equipment, tape decks, and as preamplifier for digital audio disc players and other similar products, mixer for public announcement or LM, high fidelity VCRs.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FEATURES

- Low noise ..... S/N=82dB(typ.)
  (shorted input, RIAA, IHF-A, PHONO 2.5mVrms)
- High slew rate ..... SR=40V/μs(typ.)
  (Variable by extermally connected RC due to external phase compensation type)
- High input impedance ..... R_i=1000MΩ(typ.)
- Low distortion rate ..... THD=0.001%(typ.)
  (f=1kHz, RIAA, V_O=5Vrms)
- Large load current and allowable current
  ..... I_{LP}=±50mA
  P_d=1W

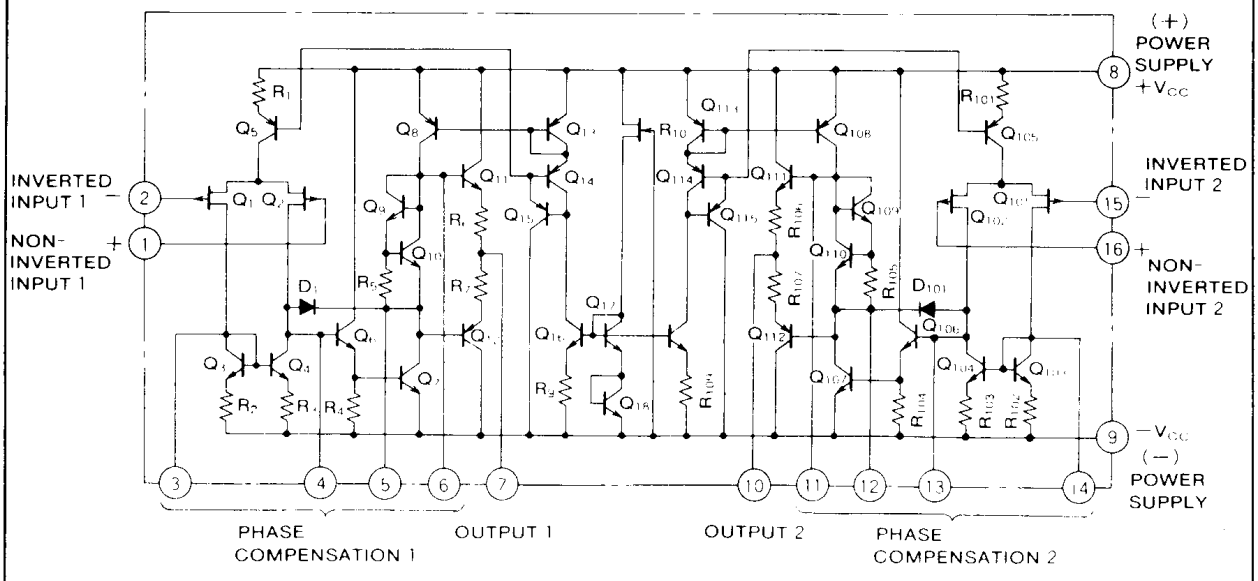
APPLICATION

Amplifier in stereo equipment, tape decks and digital audio disc players, mixer.

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... ±5~±15V
Rated supply voltage ..... ±15V

EQUIVALENT CIRCUIT



MITSUBISHI ELECTRIC

M5240P

DUAL LOW-NOISE J-FET INPUT OPERATIONAL AMPLIFIERS

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

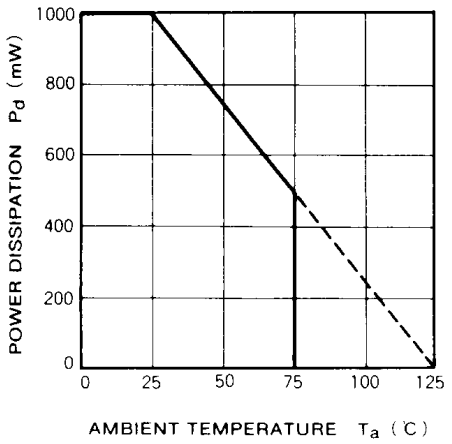
Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		±18	V
I_{LP}	Load current		±50	mA
V_{id}	Differential input voltage		±30	V
V_{ic}	Common input voltage		±15	V
P_d	Power dissipation		1000	mW
$K\theta$	Thermal derating	T_a≧25℃	10	mW/℃
T_{opr}	Ambient temperature		−20～+75	℃
T_{stg}	Storage temperature		−55～+125	℃

ELECTRICAL CHARACTERISTICS (T_a=25℃, V_{CC}=±15V)

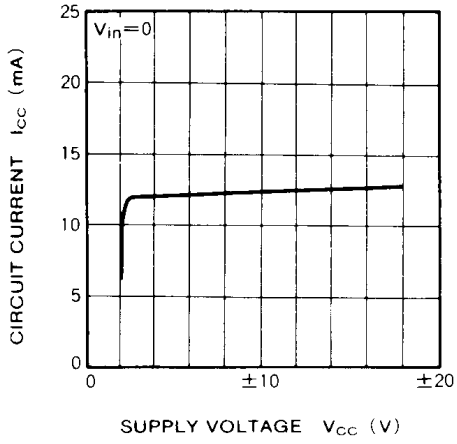
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_{in}=0		12.0	17.0	mA
V_{IO}	Input offset voltage	R_S≦10kΩ		5.0	15.0	mV
I_{IO}	Input offset current			25	1000	pA
I_{IB}	Input bias current			120	2000	pA
R_{in}	Input resistance			10^3		MΩ
G_{VO}	Open loop voltage gain	R_L≧2kΩ, V_O=±10V		110		dB
V_{OM}	Maximum output voltage	R_L≧10kΩ	±12	±14		V
		R_L≧2kΩ	±10	±13		
V_{CM}	Common input voltage width		±10	±12		V
CMRR	Common mode rejection ratio	R_S≦10kΩ	70	76		dB
SVRR	Supply voltage rejection ratio	R_S≦10kΩ		30	150	μV/V
P_d	Power dissipation			360	510	mW
SR	Slew rate	G_V=16.5dB		40		V/μs
f_T	Gain bandwidth product			18		MHz
e_n	Equivalent input refferred noise voltage	R_S=100Ω, BW=10Hz～30kHz		3.3		nV/√Hz
V_{NI}		R_g=2.2kΩ, RIAA EQ		1.2	2.5	μVrms
S/N	Signal-to-noise voltage ratio	R_g=47Ω, RIAA EQ, IHF-A		82		dB

TYPICAL CHARACTERISTICS

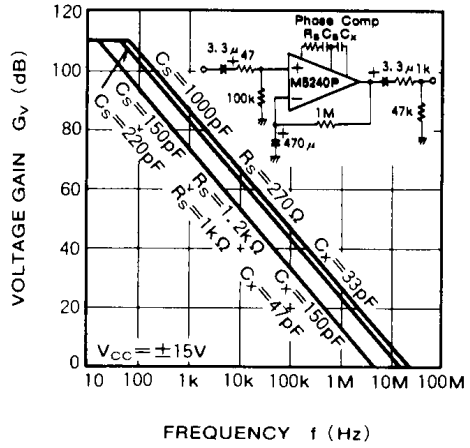
THERMAL DERATING (MAXIMUM RATING)



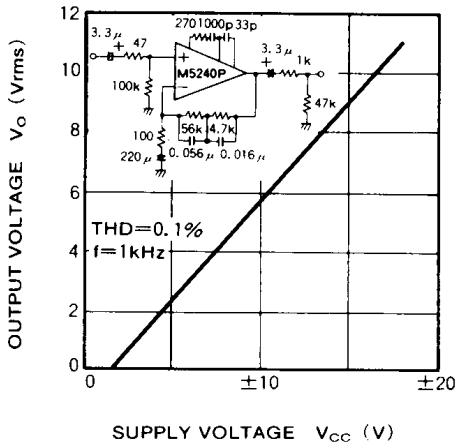
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



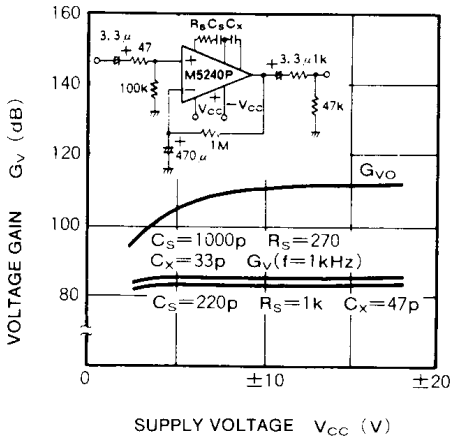
VOLTAGE GAIN VS. FREQUENCY RESPONSE



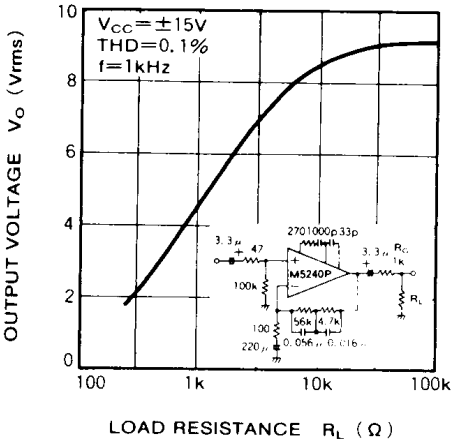
OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



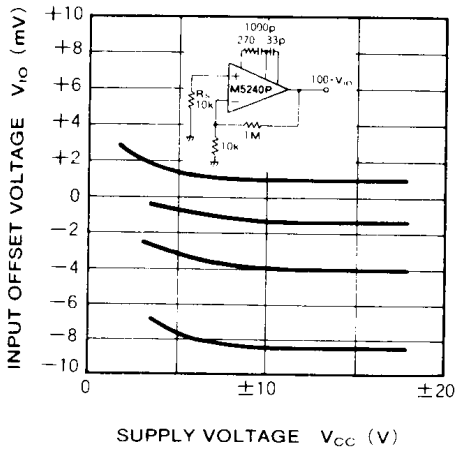
VOLTAGE GAIN VS. SUPPLY VOLTAGE



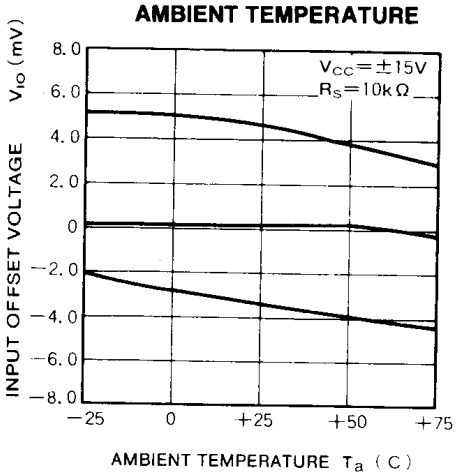
OUTPUT VOLTAGE VS. LOAD RESISTANCE



INPUT OFFSET VOLTAGE VS. SUPPLY VOLTAGE

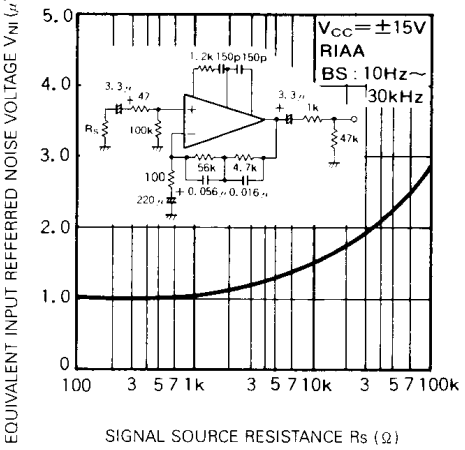


INPUT OFFSET VOLTAGE VS. AMBIENT TEMPERATURE

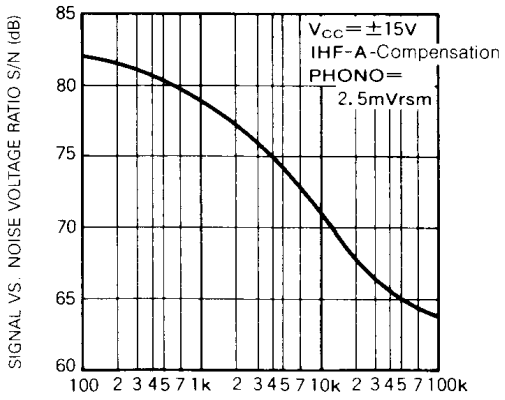


DUAL LOW-NOISE J-FET INPUT OPERATIONAL AMPLIFIERS

EQUIVALENT INPUT REFFERRED NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE

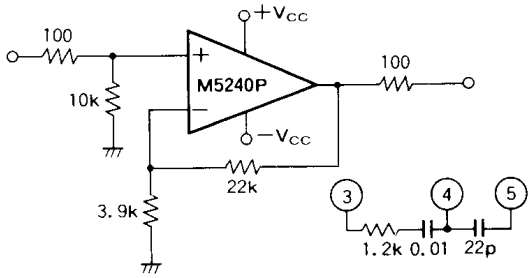


SIGNAL VS. NOISE VOLTAGE RATIO VERSUS SIGNAL SOURCE RESISTANCE



TYPICAL APPLICATION EXAMPLE

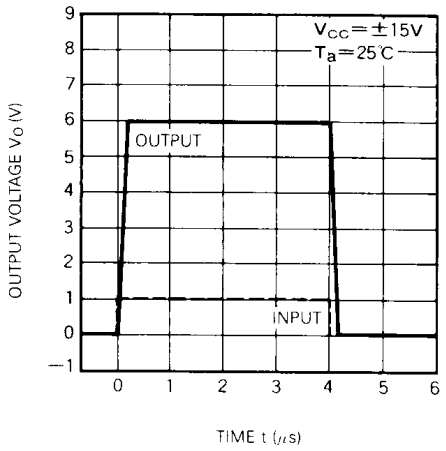
HIGH SLEW RATE FLAT AMP

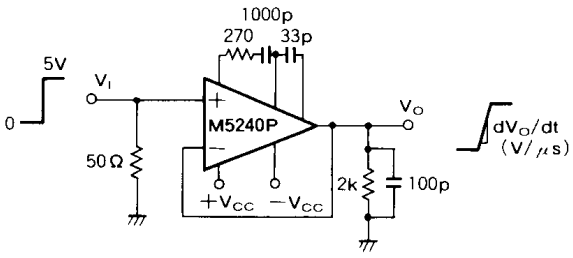


Vcc=±15
GV=16.5dB, FLAT
SR=40V/μs

Unit Resistance: Ω
Capacitance: F

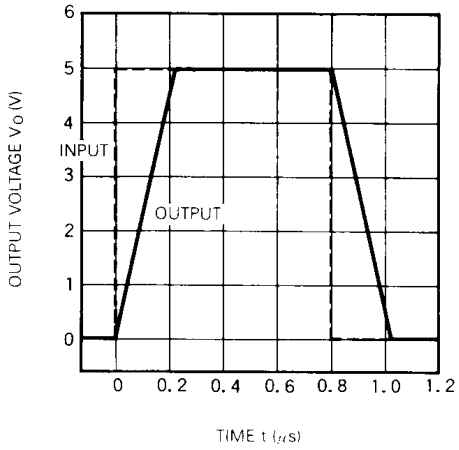
SLEW RATE (SR) CHARACTERISTICS





Vcc=±15V
SR=22V/μs

Unit Resistance: Ω
Capacitance: F



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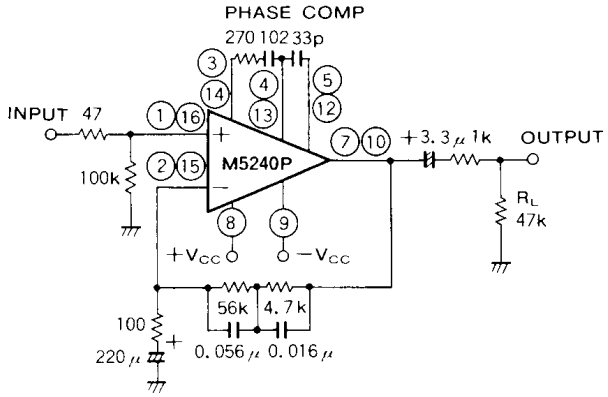
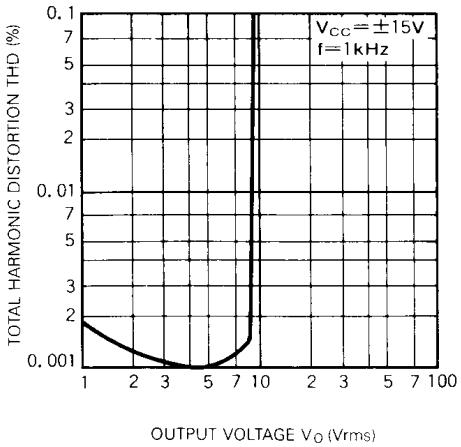
STEREO EQUALIZER AMP



TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



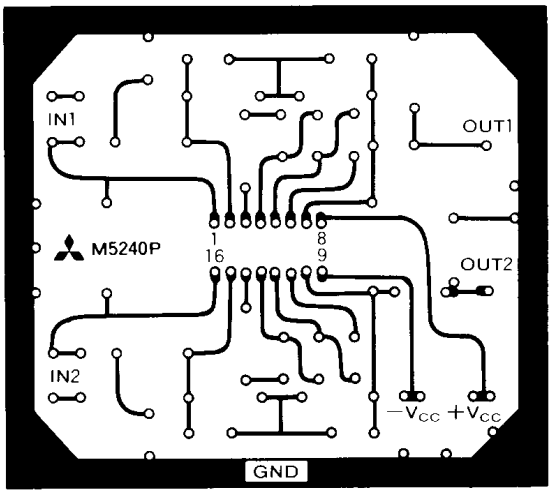
TYPICAL CHARACTERISTICS (V_{CC}=±15V, RIAA)

- G_V=35.6dB(f=1kHz)
- V_{NI}=1.2μVrms(R_g=2.2kΩ, BW=10Hz~30kHz)
- THD=0.001%(f=1kHz, V_O=5Vrms)
- S/N=82dB(IHF-A network, shorted input, input sensitivity 2.5mVrms)

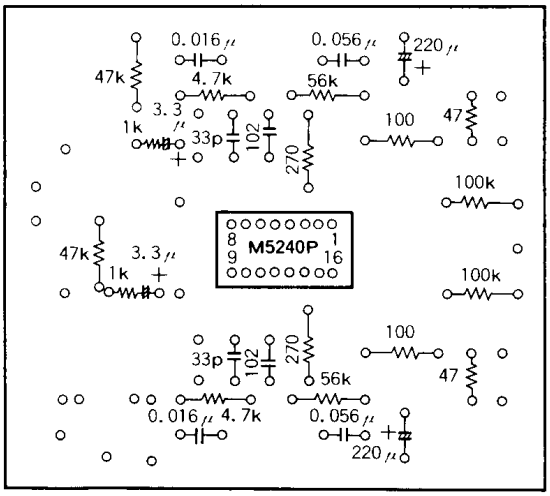
PRINTED CIRCUIT BOAD FOR CIRCUIT TESTING (TYPICAL APPLICATION CIRCUIT)

PRINTED CIRCUIT BOAD WIRING DIAGRAM

(COPPER FOIL SIDE)



(PARTS SIDE)



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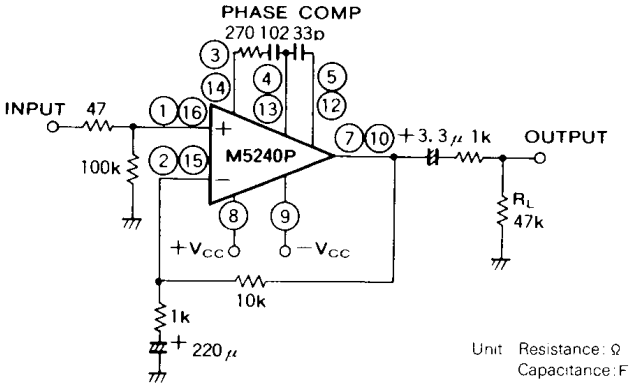
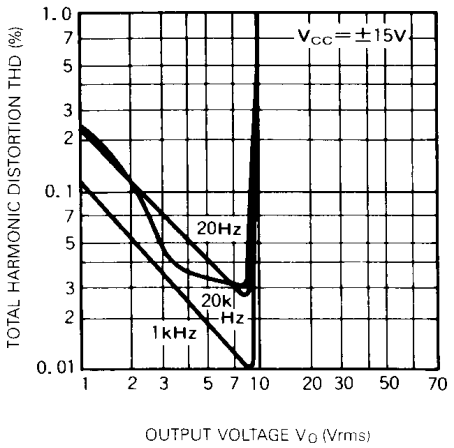
Gv=20dB FLAT AMP



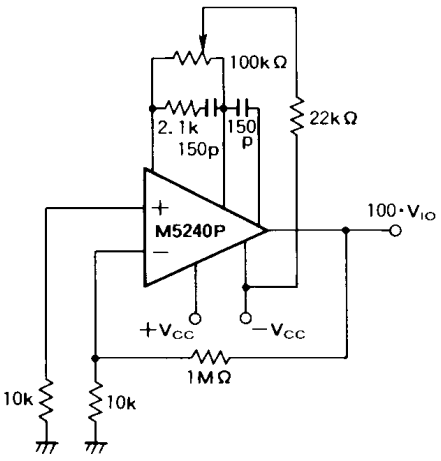
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE

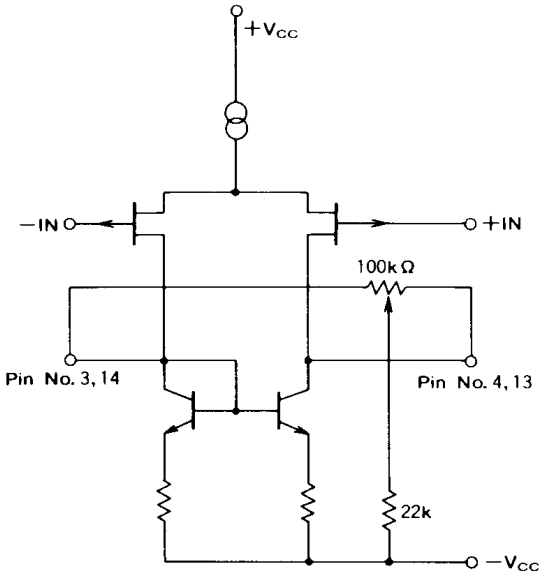


TYPICAL CHARACTERISTICS

- $V_{CC}=\pm15V$
- $G_V=20dB$(f=1kHz)
- $V_O=9.5Vrms$(f=1kHz, THD=0.1%)
- THD=0.01%(f=1kHz, $V_O=9Vrms$)

OFFSET COMPENSATION CIRCUIT





(CIRCUIT FOR EXPLANATION)