NanoAmp Solutions, Inc.
1982 Zanker Road, San Jose, CA 95112
ph: 408-573-8878, FAX: 408-573-8877
www.nanoamp.com

ES62UL256 Family

32Kx8 Bit Ultra-Low Power Asynchronous Static RAM

Overview

The ES62UXX256 is an integrated memory device containing a low power 256 Kbit Static Random Access Memory organized as 32,768 words by 8 bits. The device is fabricated using an advanced CMOS process and NanoAmp's high-speed/low-power circuit technology. This device is also designed for very low voltage operation making it quite suitable for battery powered devices having both very low operating and standby currents. The device pinout is compatible with other standard 32k x 8 SRAMs. The ES62UXX256 comes in two speed grades (45 and 25 nsec) and two very broad voltage ranges.

Features

- **Operating Voltage**
  1.5 to 3.6 Volts
- **Extended Temperature Range**
  -20^{o} to $+80^{o}$C
- **Fast Cycle Time**
  T_{ACC} < 25 nS @ 3V
- **Very Low Operating Current**
  I_{CC} < 0.8 mA typical at 2V, 1 Mhz
- **Very Low Standby Current**
  I_{SB} = 50 nA typical

FIGURE 1: Operating Envelope

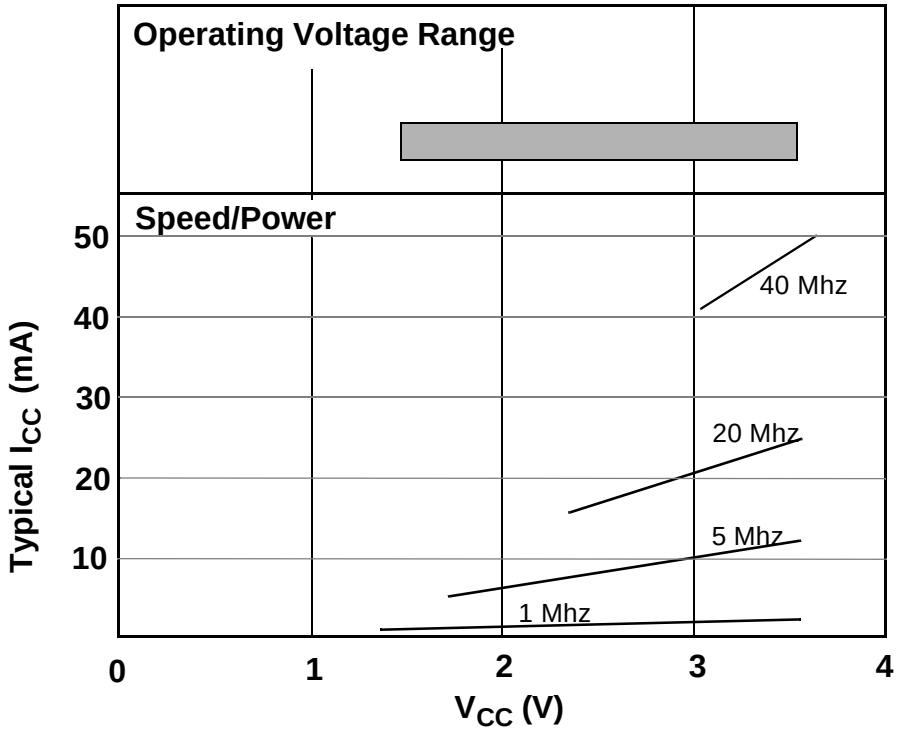
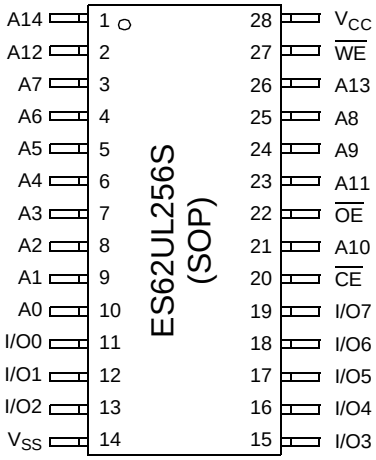


FIGURE 2: Pin Configurations



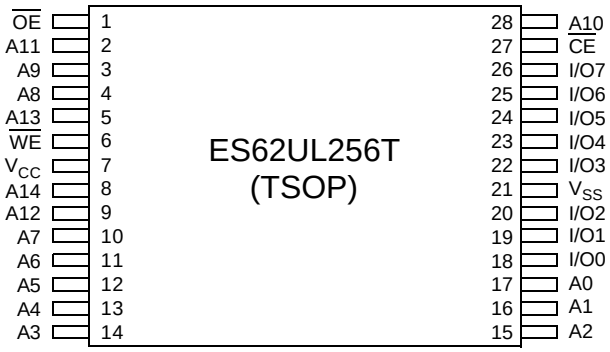


TABLE 1: Pin Functions

Pin Name	Pin Function	Pin Name	Pin Function
A0-A14	Address Inputs	$\overline{WE}$	Write Enable (Active Low)
I/O0 - I/O7	Data Inputs/Outputs	V_{CC}	Power
$\overline{CE}$	Chip Enable (Active Low)	V_{SS}	Ground
$\overline{OE}$	Output Enable (Active Low)		

FIGURE 3: Functional Block Diagram

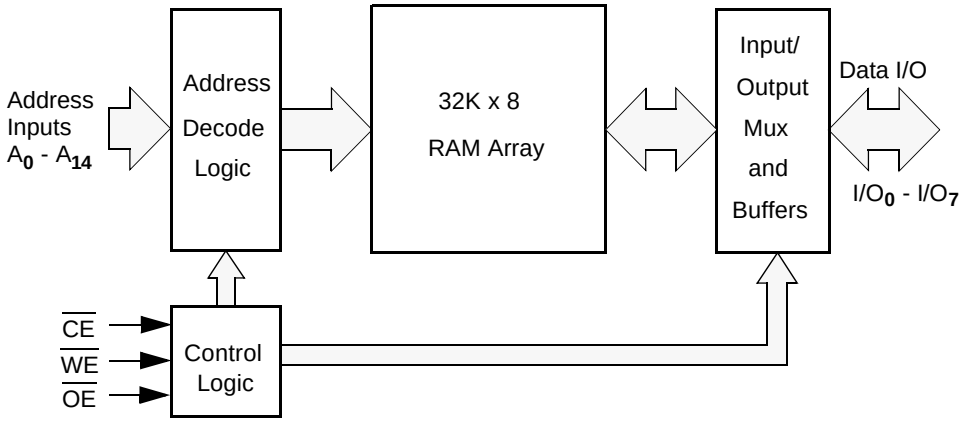


TABLE 2: Functional Description

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O_0-I/O_7	MODE	POWER
H	X	X	High Z	Standby	Standby
L	L	X	Data In	Write	Active - Standby*
L	H	L	Data Out	Read	Active - Standby*
L	H	H	High Z	Active	Active - Standby*

*The device will consume active power in this mode whenever addresses are changed

TABLE 3: Absolute Maximum Ratings*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.0	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	^oC
Operating Temperature	T_A	-20 to +80	^oC
Soldering Temperature and Time	T_{SOLDER}	260 ^oC, 10sec (Lead only)	^oC

*Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 4: Operating Characteristics (Over the Specified Temperature Range)

Item	Symbol	Test Conditions	Min/Max	L	Unit
Supply Voltage	V_{CC}		Min	1.5	V
			Max	3.6	
Data Retention Voltage	V_{DR}	$\overline{CE}$ = V_{CC}	Min	1.2	V
Input High Voltage	V_{IH}		Min	0.7V_{CC}	V
			Max	V_{CC}+0.3	
Input Low Voltage	V_{IL}		Min	–0.3	V
			Max	0.3V_{CC}	
Output High Voltage	V_{OH}	I_{OH} = 200 µA	Min	V_{CC}–0.2	V
Output Low Voltage	V_{OL}	I_{OL} = –200 µA	Max	0.2	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	Max	0.5	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{CC} or $\overline{CE}$ = V_{CC}	Max	0.5	µA
Operating Supply Current (Note 1)	I_{CC2}	V_{IN} = V_{CC} or 0V $\overline{CE}$ = V_{SS}	Typ	0.4 * f * V	mA
			Max	0.5 * f * V	
Max Standby Current (Note 2)	I_{SB}	V_{IN} = V_{CC} or 0V t_A = 55^oC	Max	1.0	µA
Typical Standby Current (Note 2)	I_{SB}	V_{IN} = V_{CC} or 0V t_A = 25 ^oC	Typ	0.05	µA

*Notes

Note 1. Operating current is a linear function of operating frequency and voltage. You may calculate operating current using the formula shown with operating frequency (f) expressed in Mhz and operating voltage (V) in volts. Example: The L device operating at 2 Mhz at 2.0 volts will draw a typical current of 0.4*2*2 = 1.6 mA.

Note 2. This device assumes a standby mode if $\overline{CE}$ is disabled (high). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling) regardless of the state of $\overline{CE}$. In order to achieve low standby current in the enabled mode (CE low), all inputs must be within 0.2 volts of either V_{CC} or V_{SS}.

TABLE 5: Capacitance

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V		5	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V		5	pF

TABLE 6: Timing Test Conditions (Over the Specified Temperature Range)

Item	
Input Pulse Level	$0.1V_{CC}$ to $0.9V_{CC}$
Input Rise and Fall Time	5nS
Input and Output Timing Reference Levels	$0.5V_{CC}$
Output Load	CL = 50pF

TABLE 7: Read Cycle Timing

Item	Symbol	Min/Max	1.5V	3.0-3.6V		Units
				-45	-25	
Read Cycle Time	t_{RC}	Min	200	45	25	ns
Address Access Time	t_{AA}	Max	200	45	25	ns
Chip Enable Access Time	t_{CE}	Max	200	45	25	ns
Output Enable to Valid Output	t_{OE}	Max	60	15	10	ns
Chip Enable to Low-Z output	t_{LZ}	Min	20	5	5	ns
Output Enable to Low-Z Output	t_{OLZ}	Min	20	5	5	ns
Chip Enable to High-Z Output	t_{HZ}	Min	0	0	0	ns
		Max	50	15	10	
Output Disable to High-Z Output	t_{OHZ}	Min	0	0	0	ns
		Max	50	15	10	
Output Hold from Address Change	t_{OH}	Min	20	5	5	ns

TABLE 8: Write Cycle Timing

Item	Symbol	Min/Max	1.5V	3.0-3.6V		Unit
				-45	-25	
Write Cycle Time	t_{WC}	Min	200	45	25	ns
Chip Enable to End of Write	t_{CW}	Min	100	35	20	ns
Address Valid to End of Write	t_{AW}	Min	100	35	20	ns
Address Set-Up Time	t_{AS}	Min	0	0	0	ns
Write Pulse Width	t_{WP}	Min	75	25	15	ns
Write Recovery Time	t_{WR}	Min	0	0	0	ns
Write to High-Z Output	t_{WHZ}	Min	0	0	0	ns
		Max	60	20	15	
Data to Write Time Overlap	t_{DW}	Min	60	25	15	ns
Data Hold from Write Time	t_{DH}	Min	0	0	0	ns
End Write to Low-Z Output	t_{OW}	Min	20	5	5	ns

FIGURE 4: Read Cycle Timing ($\overline{WE}$ = V_{IH})

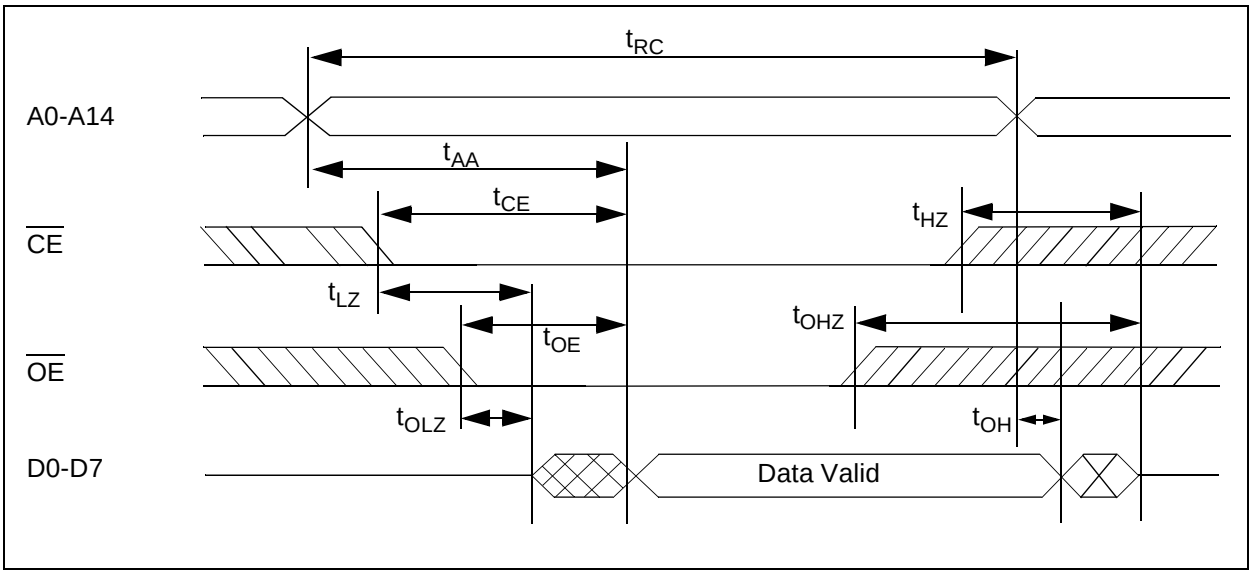


FIGURE 5: Write Cycle (1) Timing ($\overline{OE}$ clock)

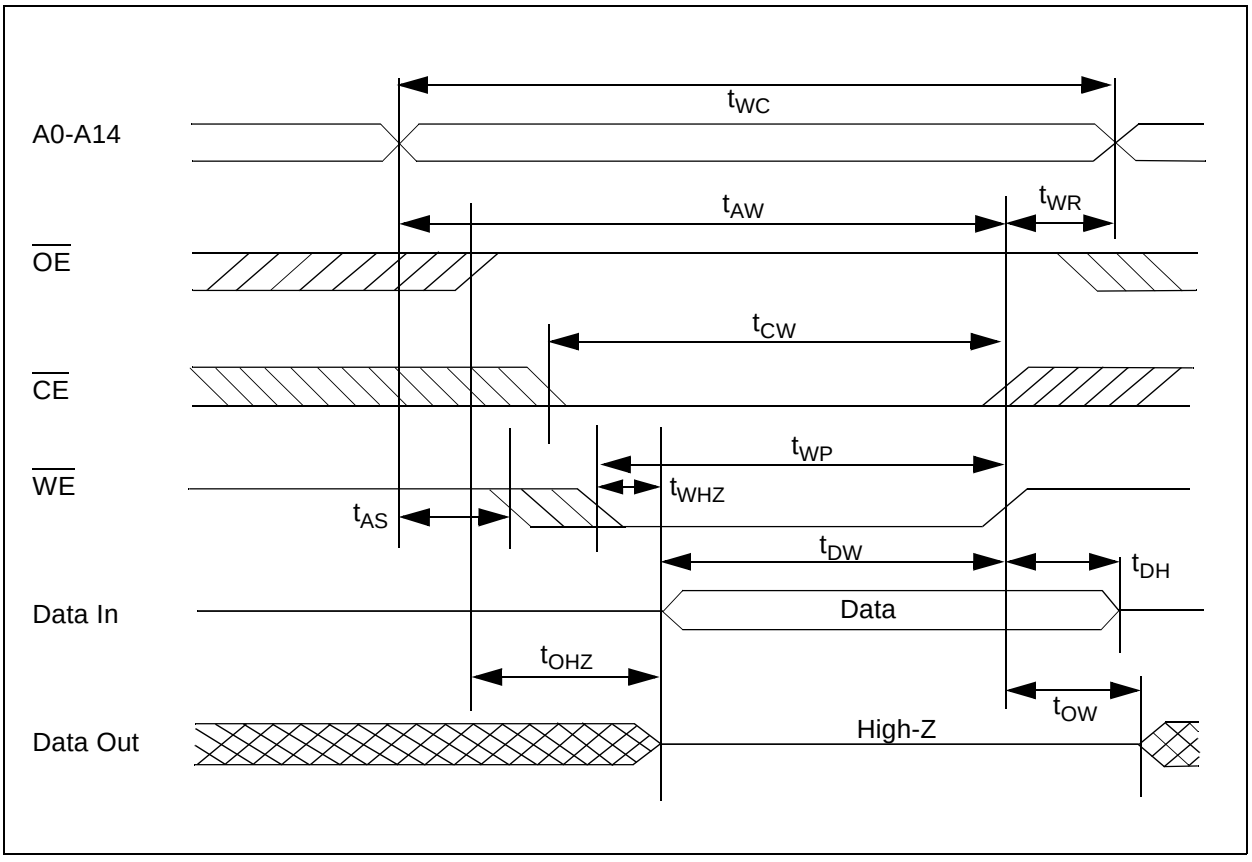


FIGURE 6: Write Cycle (2) Timing ($\overline{OE}$ fixed)

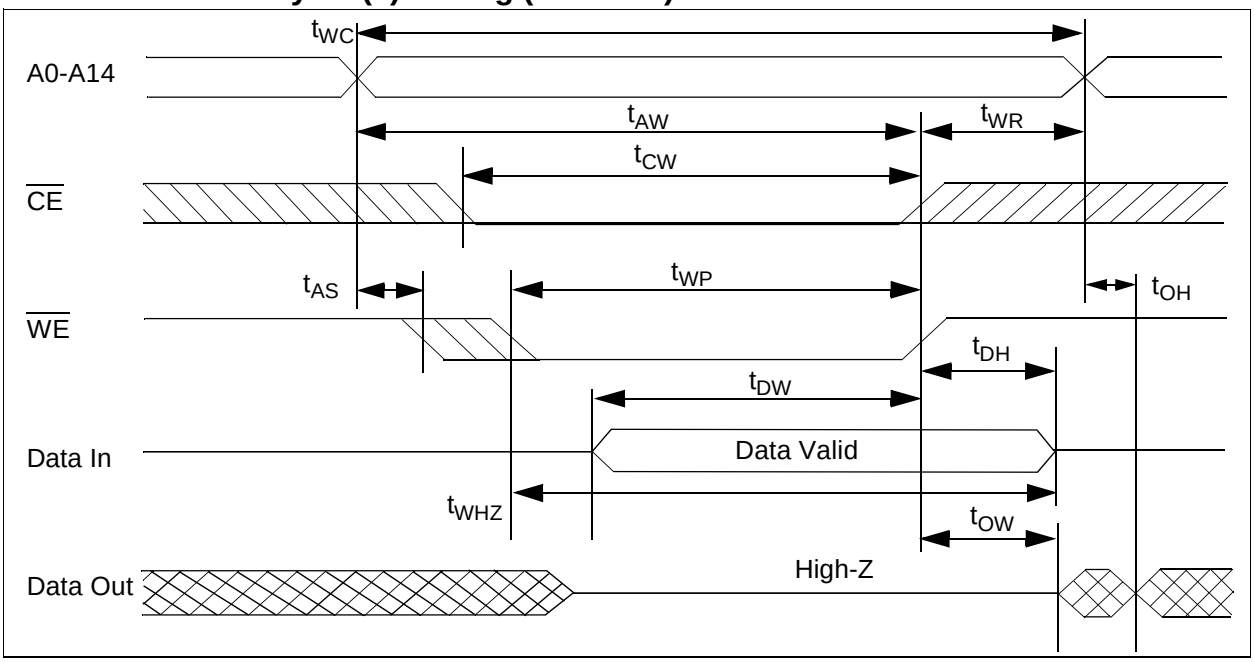


TABLE 9: Ordering Information

Part Number	Package	Temperature Range	Voltage Range	Speed (@ 3V+)
ES62UL256-45TC	28 pin TSOP	-20 to +80 ^{o}C	1.5 to 3.6 V	45 ns
ES62UL256-45SC	28 pin SOP	-20 to +80 ^{o}C	1.5 to 3.6 V	45 ns
ES62UL256-25TC	28 pin TSOP	-20 to +80 ^{o}C	1.5 to 3.6 V	25 ns
ES62UL256-25SC	28 pin SOP	-20 to +80 ^{o}C	1.5 to 3.6 V	25 ns

TABLE 10: Revision History

Revision #	Date	Change Description
01	Nov. 1, 1997	Initial Formal Release
02	Feb. 1, 1998	Corrected Temperature Range for Dynamic Testing
03	Apr. 23, 1999	Eliminated ULL family, Changed UL voltage range to 1.5 to 3.6