Am9150

1024x4 High-Speed Static R/W RAM

DISTINCTIVE CHARACTERISTICS

- 1024 x 4 organization
- High speed – 20 ns Max. access time
- Separate data inputs and outputs
- Memory reset function
- High density SLIM 24-pin 300-MIL package
- Three-state output buffers
- Single +5 V power supply ±10%
- Low-power version

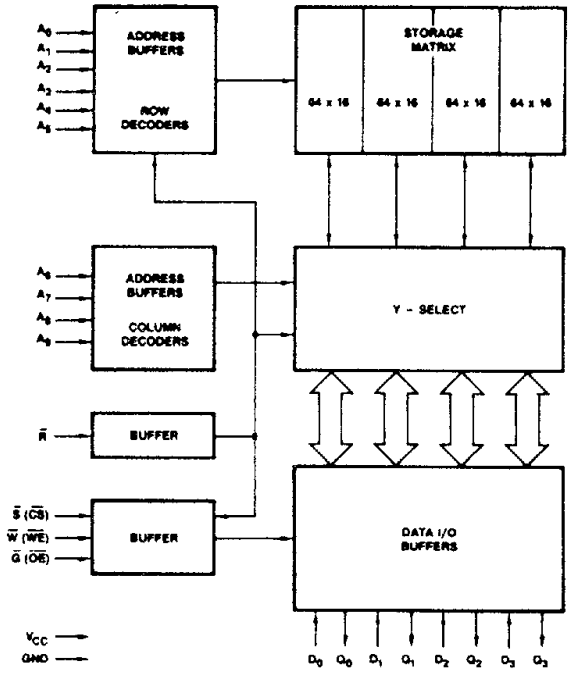
GENERAL DESCRIPTION

The Am9150 is a high-performance, static, n-channel, read/write, random-access memory organized as 1024 x 4. It features single 5 V supply operation, TTL-compatible input and output levels, and separate input and output pins for improved system performance and ease of use.

The Am9150 also incorporates a reset feature which will reset the entire contents of the memory to logical LOW in two cycle times by controlling $\overline{R}$ ($\overline{RESET}$) and $\overline{S}$ ($\overline{CS}$).

The Am9150 has four control signals $\overline{R}$, $\overline{S}$, $\overline{W}$ and $\overline{G}$. The $\overline{S}$ input controls read, write and reset operations of the device and provides for easy selection of an individual device when the outputs are tied together. The $\overline{W}$ ($\overline{WE}$) input controls the normal read and write operations, and the $\overline{G}$ ($\overline{OE}$) controls the state of the outputs.

BLOCK DIAGRAM



BD005261

MODE SELECT TABLE

Inputs				Outputs	Mode
$\overline{S}$	$\overline{W}$	$\overline{G}$	$\overline{R}$		
H	X	X	X	Hi-Z	Not Selected
L	H	X	L	Hi-Z	Reset*
L	L	X	H	Hi-Z	Write
L	H	L	H	$Q_0 - Q_3$	Read
L	X	H	H	Hi-Z.	Output Disable

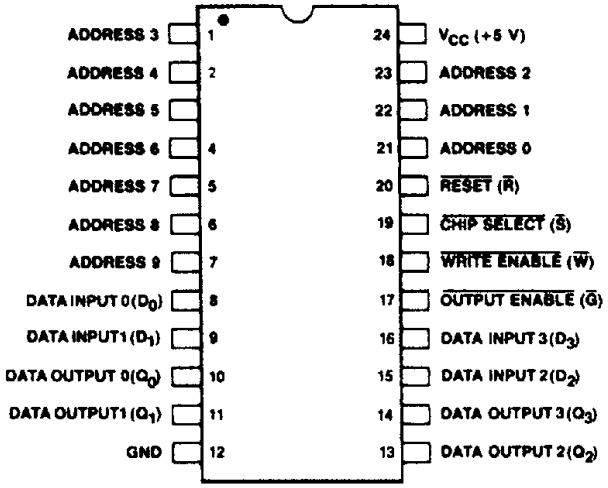
H = High
L = Low
X = Don't Care

*See Reset cycle description.

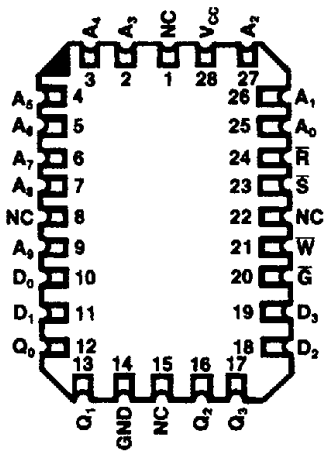
PRODUCT SELECTOR GUIDE

Part Number		Am9150-20	Am9150-25	Am9150-35	Am9150-45	Am91L50-25	Am91L50-35	Am91L50-45
Maximum Access Time (ns)		20	25	35	45	25	35	45
I_{CC} Max. (mA)	0°C to +70°C	180	180	180	180	130	130	130
	−55°C to +125°C	N/A	180	180	180	N/A	N/A	N/A

CONNECTION DIAGRAMS
Top View



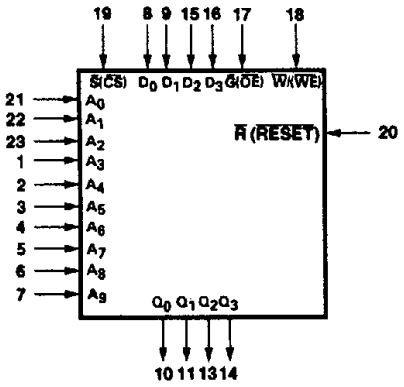
CD005963



CD005931

Note: Pin 1 is marked for orientation.

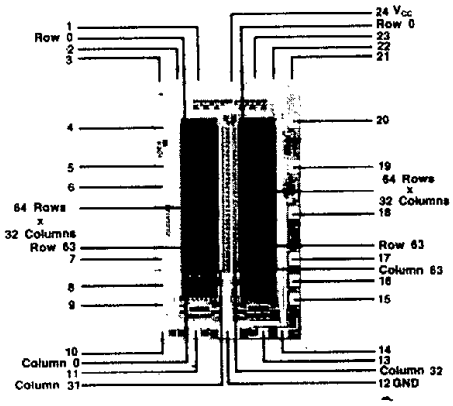
LOGIC SYMBOL
(DIP ONLY)



LS001821

Address Designators	
External	**Internal**
A_0	AX_0
A_1	AX_1
A_2	AX_2
A_3	AX_3
A_4	AX_4
A_5	AX_5
A_6	AY_0
A_7	AY_1
A_8	AY_2
A_9	AY_3

METALLIZATION AND PAD LAYOUT



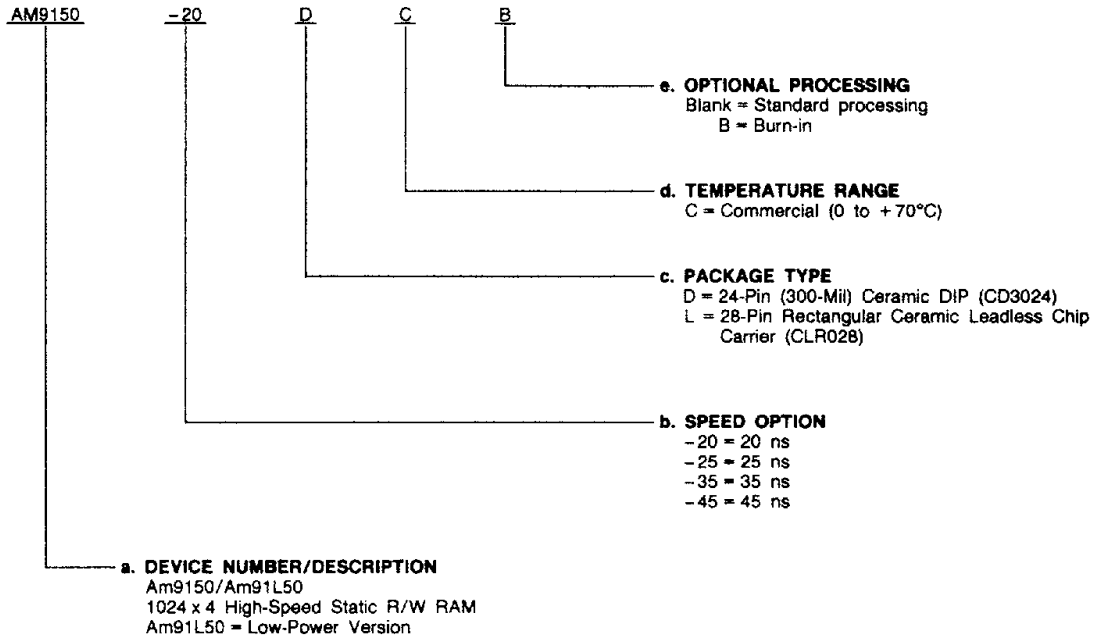
Die Size: 0.93″ x 0.163″

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM9150-20	DC, DCB, LC, LCB
AM9150-25	
AM9150-35	
AM9150-45	
AM91L50-25	
AM91L50-35	
AM91L50-45	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

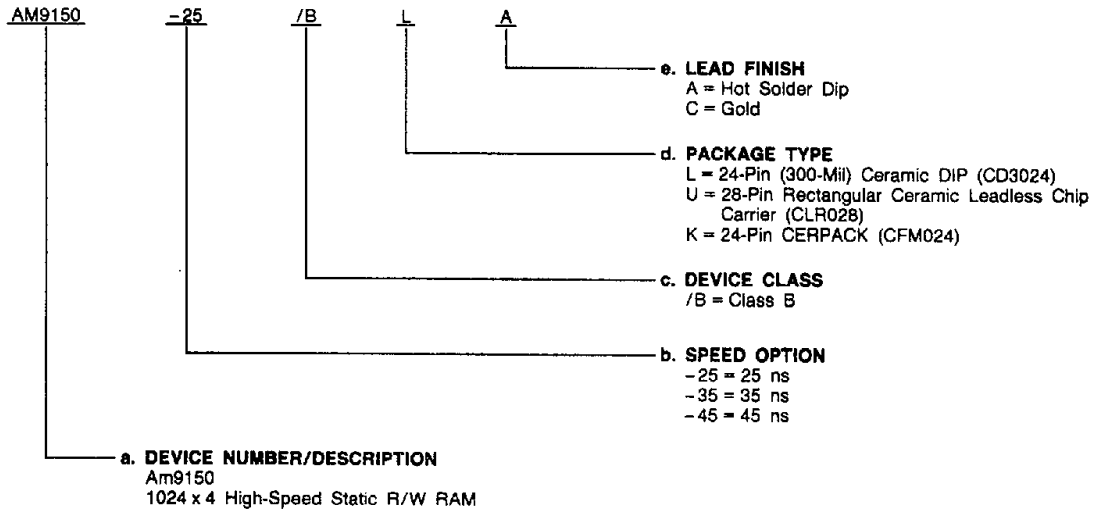
4

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

APL Products



Valid Combinations	
AM9150-25	/BLA /BUC /BKA
AM9150-35	
AM9150-45	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$A_0 - A_9$ Address (Inputs)
The 10 address inputs select one of the 1024 4-bit words in the RAM.

$\overline{S}$ Chip Select (Input; Active LOW)
An active-LOW input which selects the device for operation. When $\overline{S}$ is HIGH, the device is deselected and the outputs will be in a high-impedance state.

$\overline{W}$ Write Enable (Input; Active LOW)
$\overline{W}$ controls read and write operations. When $\overline{W}$ is HIGH and $\overline{G}$ is LOW, data will be present at the data outputs. When $\overline{W}$ is LOW, data present on the data inputs will be written into the selected memory location. The data outputs will be in a high-impedance state.

$\overline{R}$ RESET (Input; Active LOW)
An active-Low pulse on $\overline{R}$ while $A_0 - A_9$ are stable, $\overline{S}$ is LOW, and $\overline{W}$ and $\overline{G}$ are HIGH resets the whole memory.

$\overline{G}$ Output Enable (Input; Active LOW)
$\overline{G}$ controls the state of the data outputs in conjunction with $\overline{S}$ and $\overline{W}$.

$D_0 - D_3$ Data Input
Data inputs to the RAM.

$Q_0 - Q_3$ Data Output
Data outputs from the RAM. The data outputs will be in a high-impedance state when either $\overline{S}$ or $\overline{G}$ are HIGH or $\overline{W}$ is LOW.

V_{CC} Power Supply +5 Volts

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage with
Respect to Ground ..... −0.5 V to +7.0 V
Signal Voltages with
Respect to Ground ..... −3.5 V to +7.0 V
Power Dissipation (Package Limitation) ..... 1.2 W
DC Output Current ..... 20 mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +5.0 V ±10%

Military (M) Devices
Ambient Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +5.0 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Am9150 Min.	Am9150 Max.	Am91L50 Min.	Am91L50 Max.	Unit
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V		−4		−4		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V		12		12		mA
V_{IH}	Input HIGH Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input LOW Voltage			−2.5	0.8	−2.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	10	−10	10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−10	10	−10	10	µA
C_I	Input Capacitance	Test Frequency = 1.0 MHz T_A = 25°C, All Pins at 0 V, V_{CC} = 5 V (Note 8)			5		5	pF
C_O	Output Capacitance				7		7	
I_{CC}	V_{CC} Operating Supply Current	Max V_{CC} $\overline{S}$ ≤ V_{IL} Output Open	COM'L.		180		130	mA
			MIL.		180		N/A	
I_{OS}	Output Short Circuit Current	GND ≤ V_O ≤ V_{CC} (Notes 7, 8)		±50	±300	±50	±300	mA

Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the "instant-ON" case temperature.
3. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5 V.
4. The internal write time of the memory is defined by the overlap of $\overline{S}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing is referenced to the rising edge of the signal that terminates the write. $\overline{R}$ must be HIGH.
5. Transition is measured at 1.5 V on the inputs to V_{OH} − 500 mV and V_{OL} + 500 mV on the outputs using the load shown in B. under Switching Test Circuits.
6. $\overline{W}$ and $\overline{R}$ are HIGH for read cycle.
7. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
8. This parameter is not tested, but guaranteed by characterization.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol Standard	Parameter Symbol Alternate	Parameter Description		Am9150-20 Min.	Am9150-20 Max.	Am9150-25 Am91L50-25 Min.	Am9150-25 Am91L50-25 Max.	Am9150-35 Am91L50-35 Min.	Am9150-35 Am91L50-35 Max.	Am9150-45 Am91L50-45 Min.	Am9150-45 Am91L50-45 Max.	Unit
READ CYCLE													
1	TAVAV	t_{RC}	Read Cycle Time (Note 6)		20		25		35		45		ns
2	TAVQV	t_{AA}	Address Access Time			20		25		35		45	ns
3	TSLQV	t_{ACS}	Chip Select Access Time			10		15		20		25	ns
4	TGLQV	t_{OE}	Output Enable Access Time			10		15		20		25	ns
5	TSLQX	t_{CLZ}	Chip Select LOW to Output in Low-Z (Notes 5, 8)		0		0		0		0		ns
6	TSHQZ	t_{CHZ}	Chip Select HIGH to Output in Hi-Z (Notes 5, 8)		0	15	0	20	0	25	0	30	ns
7	TGLQX	t_{OLZ}	Output Enable LOW to Output in Low-Z (Note 5, 8)		0		0		0		0		ns
8	TGHQZ	t_{OHZ}	Output Enable HIGH to Output in Hi-Z (Notes 5, 8)		0	15	0	20	0	25	0	30	ns
9	TAXQX	t_{OHA}	Output Hold after Address Change	COM'L.	3		3		3		3		ns
				MIL.	1		1		1		1		
WRITE CYCLE													
10	TAVAV	t_{WC}	Write Cycle Time (Note 4)		20		25		35		45		ns
11	TSLWH	t_{CW}	Chip Select LOW to Write Enable HIGH		10		15		20		30		ns
12	TAVWH	t_{AW}	Address Valid to End of Write		15		20		30		40		ns
13	TAVWL	t_{AS}	Address Valid to Beginning of Write		5		5		5		5		ns
14	TWLWH	t_{WP}	Write Pulse Width		10		15		20		30		ns
15	TWHAX	t_{WR}	Address Hold after End of Write		5		5		5		5		ns
16	TDVWH	t_{DW}	Data in Valid to Write Enable HIGH		10		15		20		30		ns
17	TWHDX	t_{DH}	Data Hold after End of Write		5		5		5		5		ns
18	TWLQZ	t_{WZ}	Write Enable LOW to Output in Hi-Z (Notes 5, 8)		0	15	0	20	0	25	0	30	ns
19	TWHQX	t_{OW}	Write Enable HIGH to Output in Low-Z (Notes 5, 8)		0		0		0		0		ns
RESET CYCLE													
20	TAVAV	t_{RRC}	Reset Cycle Time		40		50		70		90		ns
21	TAVRL	t_{RSA}	Address Valid to Beginning of Reset		0		0		0		0		ns
22	TWHRL	t_{RSW}	Write Enable HIGH to Beginning of Reset		0		0		0		0		ns
23	TSLRL	t_{RSCS}	Chip Select LOW to Beginning of Reset		0		0		0		0		ns
24	TRLRH	t_{RP}	Reset Pulse Width		20		20		30		40		ns
25	TRHSX	t_{RHCS}	Chip Select Hold after End of Reset		0		0		0		0		ns
26	TRHWL	t_{RHW}	Write Enable Hold after End of Reset		20		30		40		50		ns
27	TRHAX	t_{RHA}	Address Hold after End of Reset		20		30		40		50		ns
28	TRLQZ	t_{RHZ}	Reset LOW to Output in Hi-Z (Notes 5, 8)		0	15	0	20	0	25	0	35	ns
29	TRHQX	t_{RLZ}	Reset HIGH to Output in Low-Z (Notes 5, 8)		0		0		0		0		ns

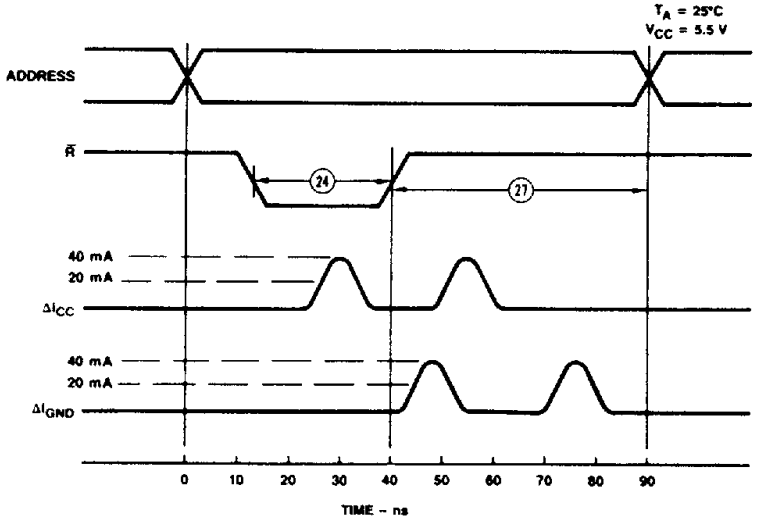
Notes: See notes following DC Characteristics table.

RESET CYCLE

The reset cycle is initiated by $\overline{R}$ going LOW for a time $\geq t_{RP}$, and is terminated by holding $\overline{R}$ HIGH for a time $\geq t_{RHA}$. The addresses to the device must be stable during the RESET cycle time. The entire contents of the RAM will be reset to ZERO regardless of the address chosen during the cycle. The control $\overline{S}$ must be $\leq V_{IL}$ maximum, and $\overline{W}$ must be $\geq V_{IH}$ minimum and it is recommended that $\overline{G}$ be $\geq V_{IH}$ minimum.

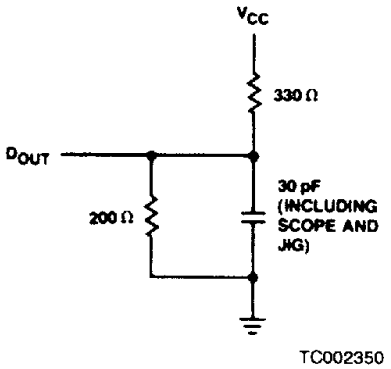
The reset cycle is normally associated with current spikes, both at V_{CC} and GND as shown in the graph. To attenuate the current spikes, an external bypass capacitor (high frequency, 0.1 μF) for each Am9150 socket is recommended.

Typical I_{CC} and I_{GND} During a Reset Cycle



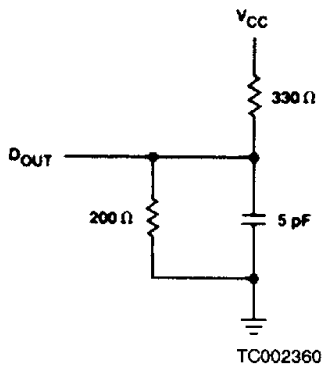
WF009920

SWITCHING TEST CIRCUITS



TC002350

A.



TC002360

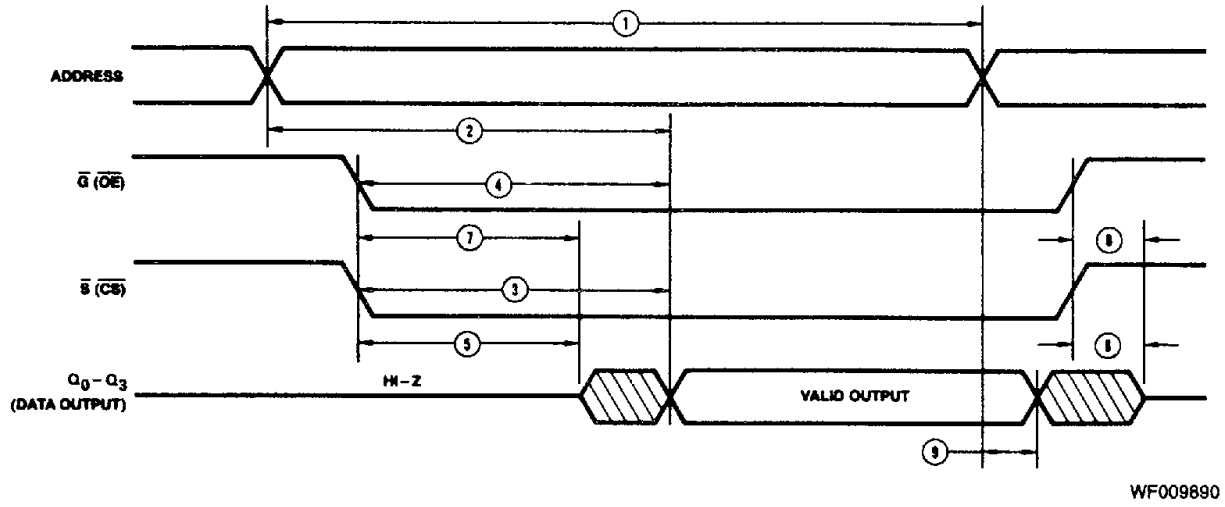
B.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⋈	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

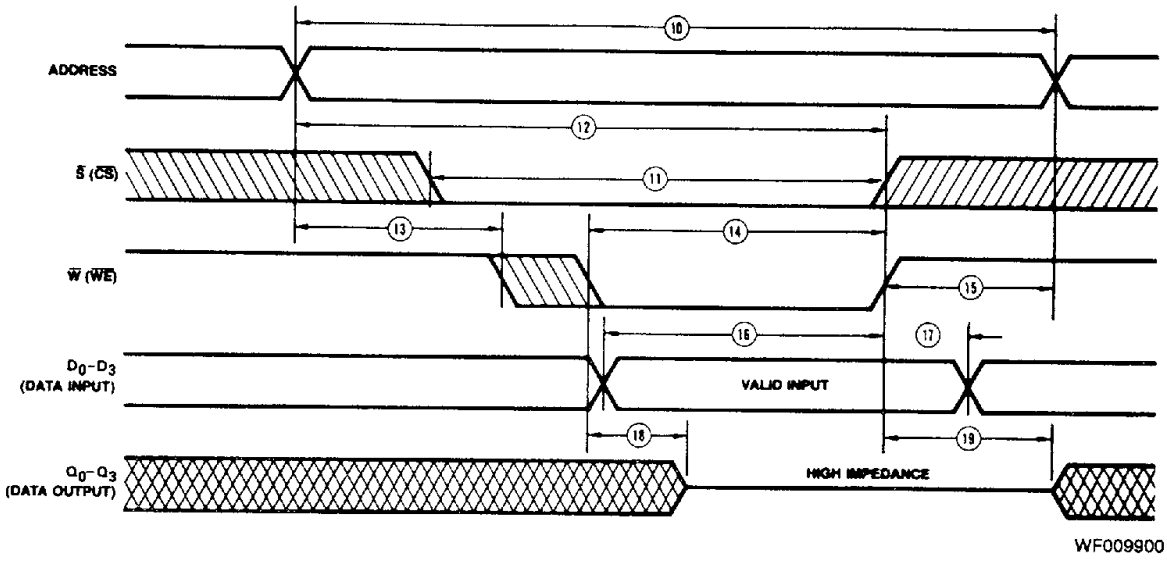
KS000010



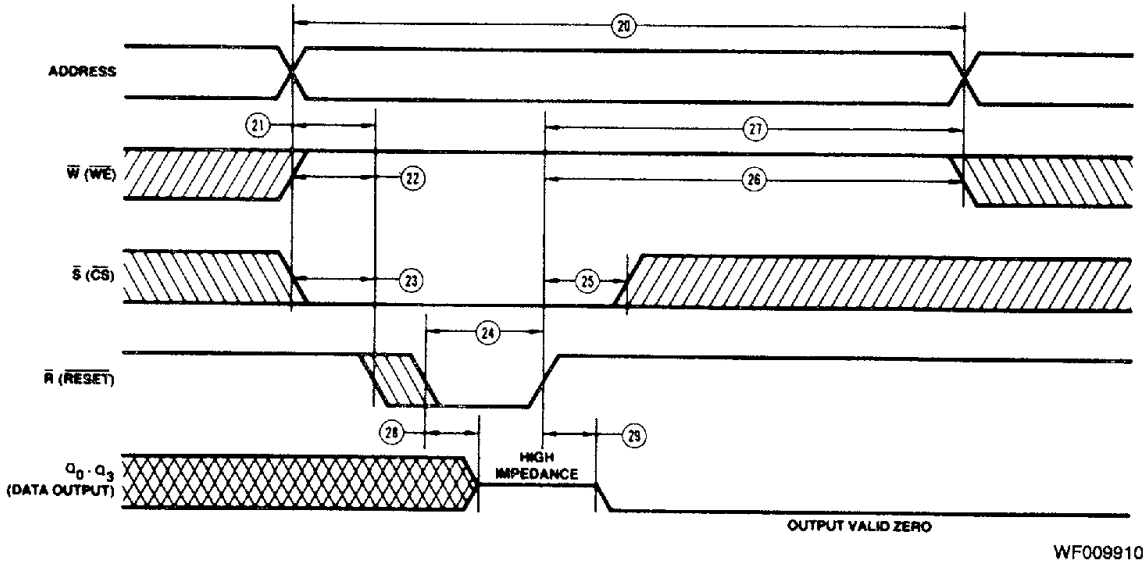
WF009890

Read Cycle

SWITCHING WAVEFORMS (Cont'd.)



Write Cycle



Reset Cycle

4