FOCUS enhancements
superior video conversion technology

FS450, FS451
i-Net TV Interface Video Processor

Features

- Flexible clock, data, and electrical interfaces allows glue-less digital interface to Intel 82810, National Geode and most other graphic controller chips ("GCC")
- Capable of operating as clock master, pseudo-master, and slave and supports both single and differential master clocks
- Programmable 2D scaling †
  - Variable horizontal up and down scale
  - Variable vertical downscale
  - Output format can be tuned to the exact dimensions of the TV
- Advanced 2-D flicker filter †
- Supports Multiple Progressive Input Resolutions
  - 640x480 to 1024x768
- Multiple Output Standards
  - NTSC, NTSC-EIAJ, PAL-B/D/G/H/I/M/N
  - Composite, S-Video, RGB SCART
  - Composite Y-Notch and C-Bandpass Filters
- Genlock the GCC and incoming Video
  - Provides the pixel clock to the GCC generated from a single 27MHz clock
  - Provides frame synchronization output signal for other video components
- CCIR 656 outputs
- CCIR 656 input to the encoder
- 10-bit output D/A converters
- Macrovision 7 compliant (FS451 only)
- I^2C‡ compatible port controls
- High level programming interface
- 100 pin PQFP package
- 3.3V operation

†Note: Covered under US Patent # 5,862,268 and/or patents pending.

‡Note: I^2C is a registered trademark of Philips Corporation. The FS450 SIO bus is similar but not identical to Philips I^2C bus.

Description

The i-Net TV FS450 is a fourth generation video scan converter. It accepts many input resolutions, rates and formats and converts them to NTSC or PAL standards compliant with SMPTE-170M and CCIR-656 standards. The chip has a programmable down scaler to fit the incoming resolution to the output display format. The CCIR 656 ports allow external interface to other video chips. The sync control block generates frame reset for genlocking other video components. Required external components are minimal: a single 27 MHz oscillator or crystal and passive parts.

Digital progressive RGB inputs are downscaled or upscaled to the CCIR-656 horizontal pixel count and converted to the 656 format. Vertical scaling and flicker filtering are done in 656 format.

The Flicker Filter is an advanced 2 dimensional filter that enhances text quality. Flicker Filter and Sharpness parameters are programmable.

A digital video encoder that generates analog Y/C and Composite Video outputs is part of the FS450. For the composite output in NTSC, Y-Notch and C-Bandpass filters are available. For RGB and YUV outputs, the encoder may be bypassed via a YUV to RGB transcoder for SCART compatible video.

Scaling and clock parameters are automatically programmed by the driver, so the system remains genlocked with resolution changes. The input parameters to the automatic scaling are TV viewable area, PAL or NTSC, and the GCC CRT Control Registers' settings.

The FS451's encoder incorporates Macrovision 7 anti-copy protection technology.

All parameters can be read and written via the I^2C compatible serial port.

Power is derived from +3.3V digital and analog supplies. The package is 100-lead Quad Flat Pack (PQFP).

Applications

- Internet Set Top Boxes
- PC video out (TV Ready PCs)
- Cable/DVD Player Set Top Boxes
- Web Appliances
- Information Appliances
- Video Kiosks

Typical System Architectural Block Diagram

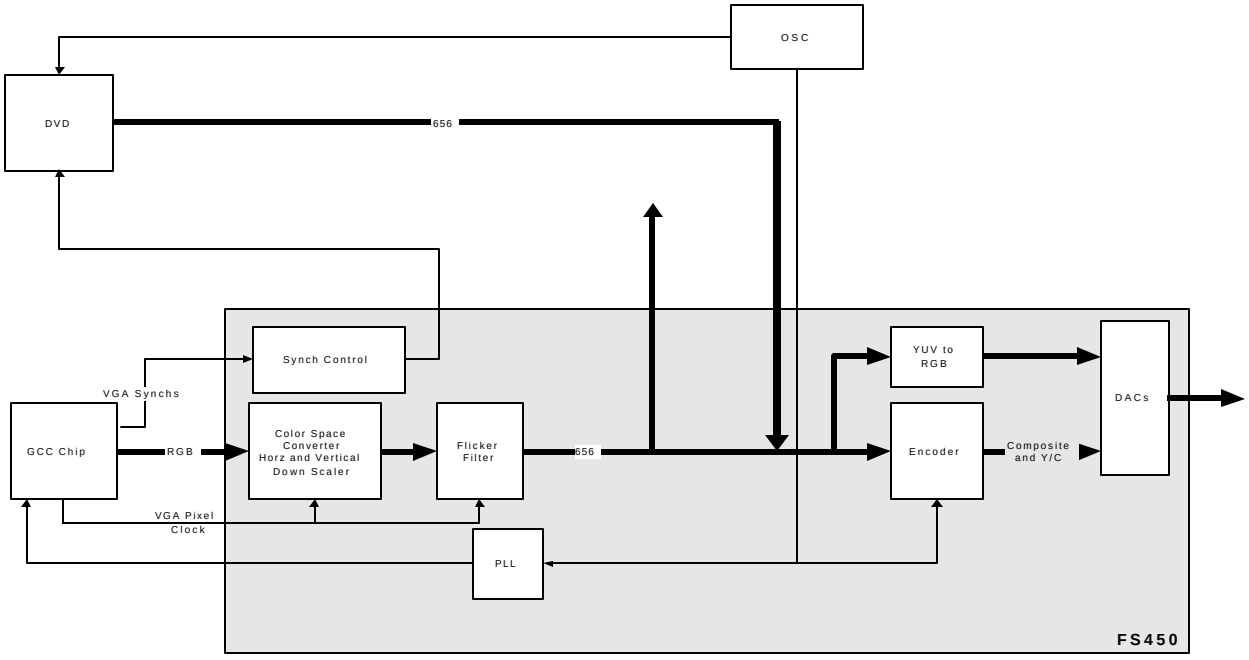

Figure 1: Typical System Block Diagram

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2. Architectural Overview

The FS450 i-Net TV Video Interface Processor provides NTSC or PAL TV out for Intel's 82810 Video Co-processor and many other 3D graphic controller ("GCC") chips. It accepts digital RGB in, converts it to CCIR 656 digital video, provides interfaces to external 656 digital DVD systems, windowing hardware, alpha blenders, et al and outputs very high quality RGB, YUV, S-Video, or Composite Video. The chip consists of the following major sections:

- Oscillators and PLLs
- Serial Control Port
- Sync Control
- Input and Output Frame Formats
- Color Space Converter & Scaler
- Flicker Filter
- Encoder
- YUV to RGB Converter

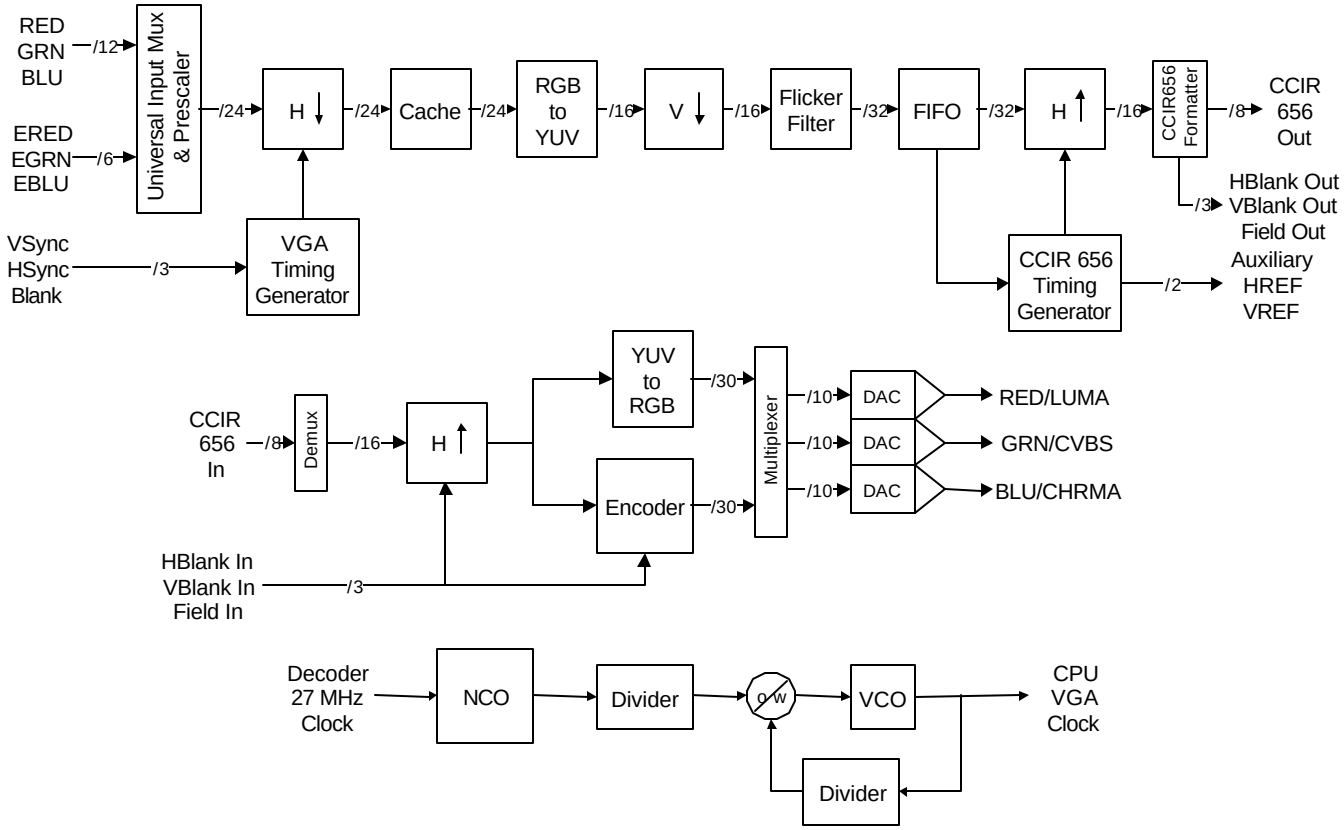


Figure 2: FS450 Functional Block Diagram

2.1 Oscillators and PLLs

The FS450 synthesizes a 27 to 85 MHz clock off of the 27 MHz Television clock and supplies this clock (VGA_CKOUT) to the GCC. This clock is buffered and returned to the FS450 (VGA_CKIN) synchronous to the RGB data and Sync information. This clock has a 1½ Hz resolution and must be adjusted so the GCC scaled input data rate exactly matches the CCIR 656 data output rate.

The VG_CKOUT Phase Lock Loop (PLL) synthesizer uses Numerically Controlled Oscillator (NCO) to fine adjust the 27MHz oscillator to a clock precisely matched to the digital RGB data coming from the GCC. Additionally, the PLL itself can be controlled by programming the numerator (M) and denominator (N) of the PLL itself. The combination of the PLL synthesizer and NCO are used to precisely match the input to the output.

2.2 Serial Control Port

FS450 setup is programmed by registers that are accessible via the $I^2C^{\ddagger}$ compatible serial port (SIO). Status and Revision ID can also be read from the registers.

‡Note: I^2C is a registered trademark of Philips Corporation. The FS450 SIO bus is similar but not identical to Philips I^2C bus.

2.3 Sync Control

The FS450 operates in a slave mode, pseudo-master mode or full master mode. In pseudo-master mode, the GCC graphic controller derives the VGA pixel clock, horizontal sync, and vertical sync from VGA_CLKOUT supplied by the FS450. The syncs are used inside the FS450 to capture the computer video and are regenerated to supply to external devices such as genlocked video from a DVD player or tuner. In full master mode, the FS450 supplies to the GCC horizontal and vertical sync in addition to the VGA pixel clock.

2.4 Input and Output Frame Formats

The FS450 does not contain a frame memory. Therefore, the FS450 output frame rate must be synchronous to the input frame rate. To accomplish this, the active video portion in the output stream must overlay the corresponding active video time in the input stream. Several registers on the FS450 control this timing as illustrated in the following figures:

VGA_VSYNC	VGA_HSYNC	IHO	A	B	IHO + IHW
IVO	Blank	Blank	Blank	Blank	Blank
C	Blank	Black	Black	Black	Blank
D	Blank	Black	**Active Video**	Black	Blank
IVO + IVW	Blank	Black	Black	Black	Blank
	Blank	Blank	Blank	Blank	Blank

Figure 3: GCC Frame Format

IHO = OHO / Hscale
IHW = OHW / Hscale
IVO = OVO / Vscale
IVW = OVW / Vscale

The output frame timing is determined by the CCIR601 and 656 specifications. Input parameters IHO, IVO, and IHW must be set correctly so that when the image is scaled to the 656 output frame, the timing requirements are met. Parameters A, B, C, and D are determined by the amount of underscan the user wants on the target television screen.

656_VSYNC	656_HSYNC	OHO	A^	B^	OHO + OHW
OVO	Blank	Blank	Blank	Blank	
C^	Blank	Black	Black	Black	
D^	Blank	Black	**Active Video**	Black	
OVO + OVW	Blank	Black	Black	Black	
	Blank	Blank	Blank	Blank	

Figure 4: CCIR 601/656 Field Format

OHO = 139 NTSC, 145 PAL
OHW = 720
OVO = 20 NTSC, 23 PAL
OVW = 487 NTSC, 576 PAL

2.5 Color Space Converter and Scaler

The digital RGB from the GCC is horizontally compressed, stored into a line buffer cache. As the data is pulled from the line buffer cache, it is converted to 656 YUV and compressed vertically.

2.6 Flicker Filter

The FS450 flicker filter provides significantly more control over the display characteristics than a typical 3 line average flicker filter. The FS450's flicker filter consists of both horizontal (Sharpness) and vertical (Flicker) controls. Thus, it is called a 2D flicker filter. Both the Sharpness and Flicker registers can be programmed over a wide range to allow the user to tradeoff flicker and sharpness for readability and reduced eye fatigue.

2.7 Encoder

The FS450 contains a high quality 2x oversampled video encoder. The 656 luma information is up-sampled from 13.5 MHz sample rate to 27 MHz with a 19 tap filter which offers excellent flatness to 6MHz and 50 dB image aliasing suppression. Chrominance information is up-sampled from 6.75MHz sample rate to 27 MHz with four user selectable bandwidths. The encoder has programmable width and frequency luma notch filter.

The encoder subcarrier is programmable in frequency and phase and with the independence of color format, vsync, and number of lines allows for the support of the many video standards, including all South American variations. The FS450 video encoder outputs NTSC M, J and PAL B, D, G, H, I, M, N, Combination N formats with 10 bits of resolution. Both Composite and S-Video outputs are available simultaneously.

2.8 YUV to RGB Converter

As an alternative to encoded PAL or NTSC, the user may select analog RGB outputs. Each channel of RGB has 10 bits of resolution.

3. Typical System Configurations

There are 3 "typical" system configurations envisioned for the FS450:

1) GCC ⇒ TV output only;
2) GCC or DVD output switched ⇒ TV;
3) Multiple digital video sources blended ⇒ TV.

3.1 GCC Þ TV Output Only

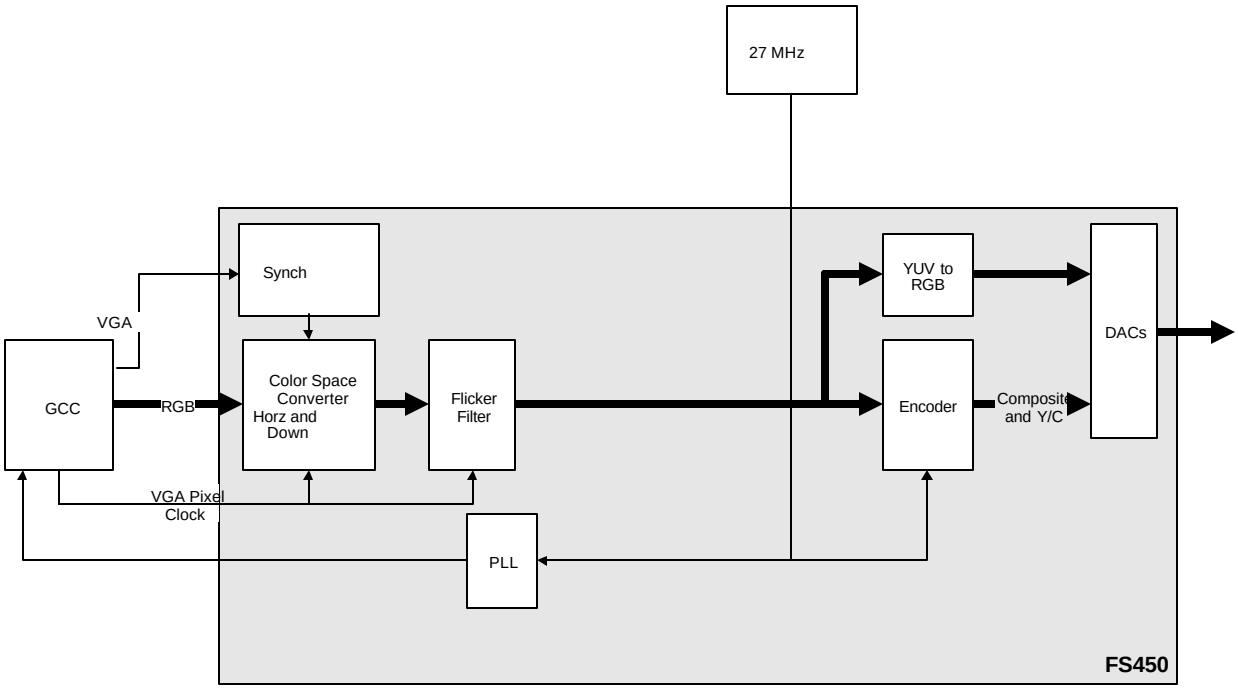


Figure 5: GCC Þ TV Output Only

3.2 GCC or DVD Output Switched Þ TV

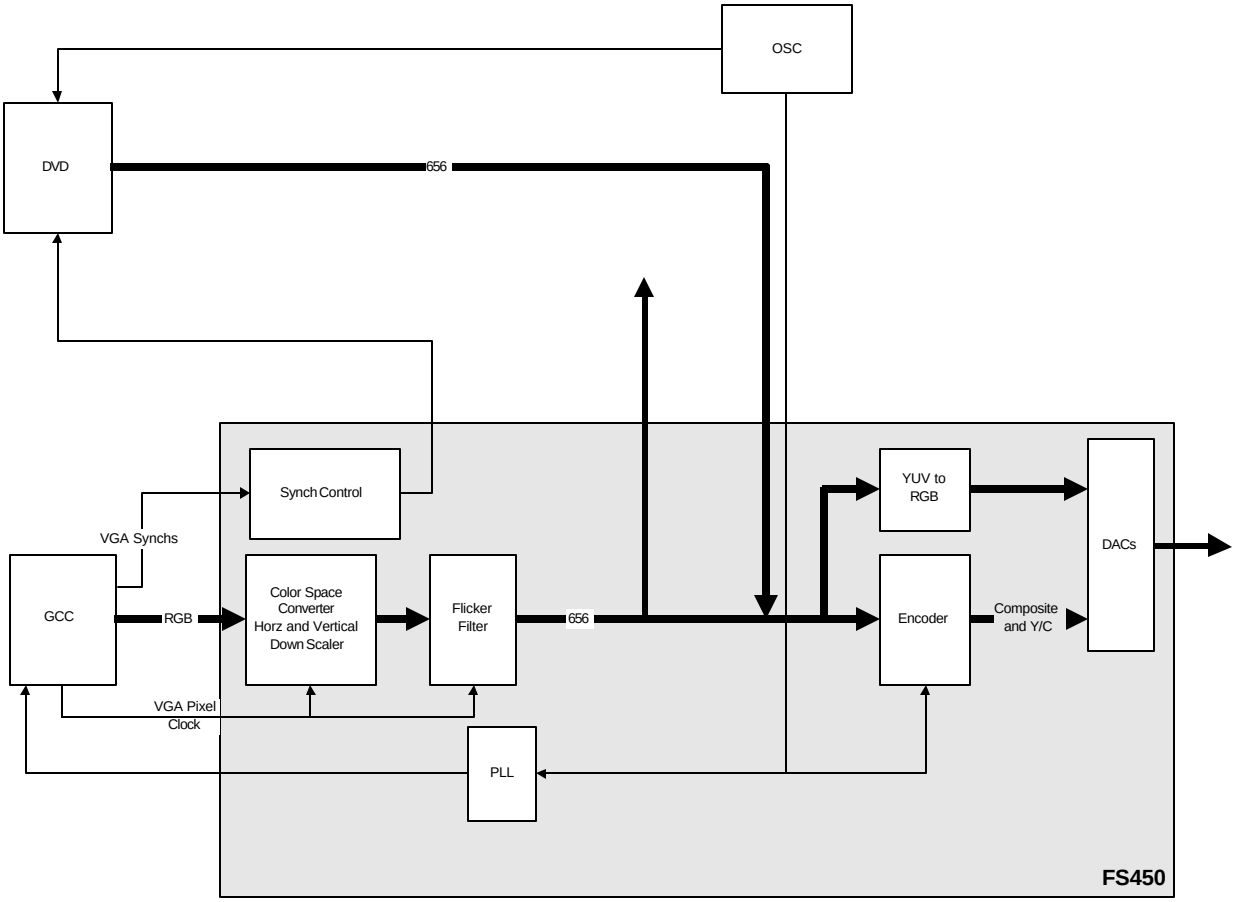


Figure 6: GCC or DVD output switched Þ TV

3.3 Multiple Digital Video Sources Blended Þ TV

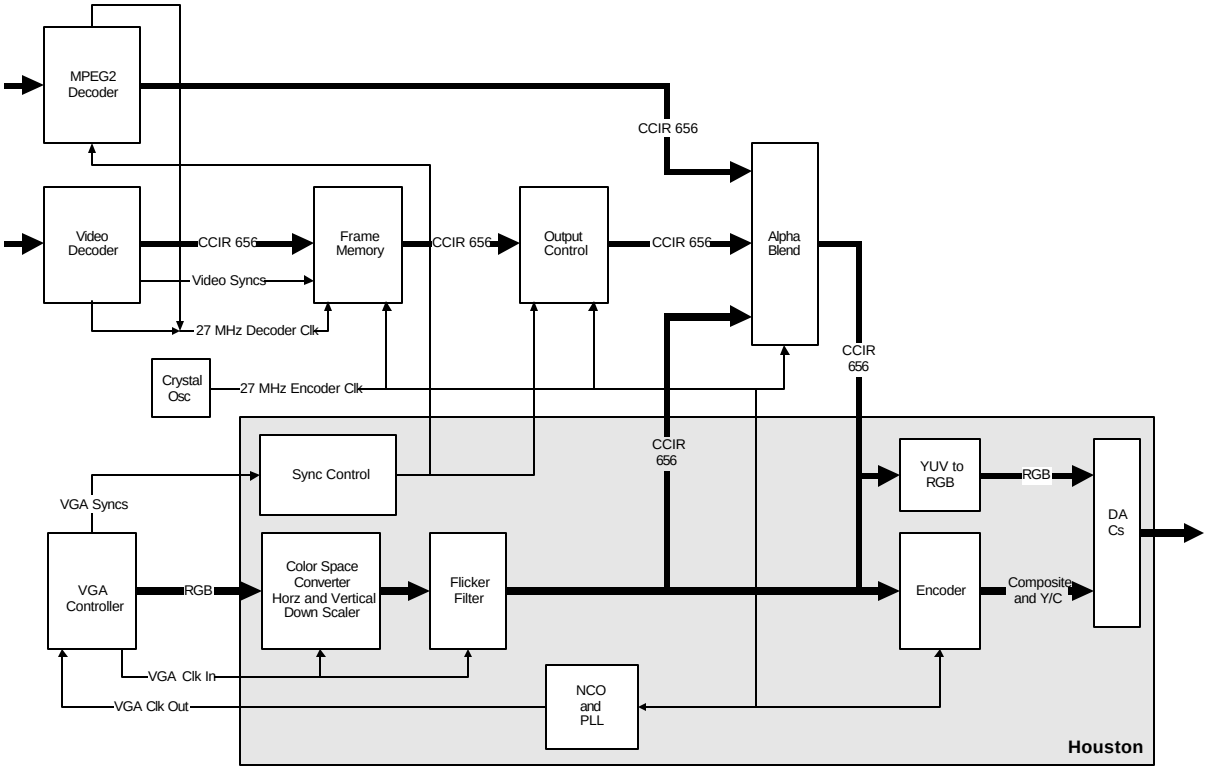
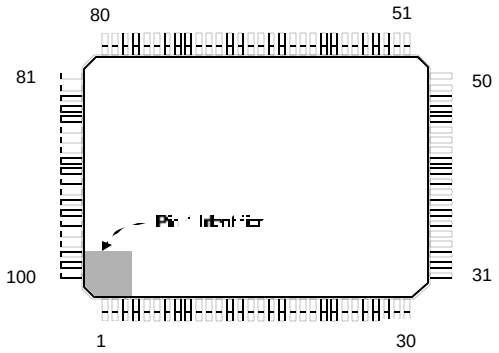


Figure 7: Multiple digital video sources blended Þ TV

4. Pin Assignments



Pin		Name	Pin		Name	Pin		Name	Pin		Name
1.	R	TV_CKIN	31.	P	VGA_CKOUT	51.	R	P_2	81.	O	$V656\_OUT_4$
2.	O	XTAL	32.	R	V_{SS}	52.	R	P_3	82.	R	V_{DD}
3.	R	V_{DDOSC}	33.	R	V_{DD}	53.	R	P_4	83.	O	$V656\_OUT_5$
4.	R	V_{SSOSC}	34.	O	Reserved (open)	54.	R	P_5	84.	O	$V656\_OUT_6$
5.	G	Reserved (GND)	35.	O	Reserved (open)	55.	R	GTL_REF	85.	O	$V656\_OUT_7$
6.	N	Reserved (open)	36.	S	E_5	56.	R	V_{DD}	86.	R	V_{SS}
7.	R	V_{SSDA}	37.	O	E_4	57.	R	P_6	87.	S	FIELD_IN
8.	R	V_{REF}	38.	R	V_{SS}	58.	R	P_7	88.	S	VBNK_IN
9.	R	R_{REF}	39.	O	VGA_CKOUTTL	59.	R	P_8	89.	S	HBNK_IN
10.	R	V_{DDDA}	40.	O	E_3	60.	R	P_9	90.	R	V_{DD}
11.	R	C_{BYPASS}	41.	O	E_2	61.	R	V_{SS}	91.	S	$V656\_IN_0$
12.	O	Y/Red	42.	O	E_1	62.	R	P_{10}	92.	S	$V656\_IN_1$
13.	R	V_{DDDA}	43.	O	E_0	63.	R	P_{11}	93.	S	$V656\_IN_2$
14.	R	V_{SSDA}	44.	R	BLANK	64.	R	VGA_NCKIN	94.	S	$V656\_IN_3$
15.	O	CVBS/Green	45.	R	V_{DD}	65.	R	VGA_PCKIN	95.	R	V_{SS}
16.	R	V_{DDDA}	46.	R	VSYNC_IN	66.	R	V_{DD}	96.	S	$V656\_IN_4$
17.	O	C/Blue	47.	R	HSYNC_IN	67.	O	AVREF	97.	S	$V656\_IN_5$
18.	R	V_{DDDA}	48.	R	P_0	68.	O	VSYNC_OUT	98.	S	$V656\_IN_6$
19.	O	CSYNC	49.	R	P_1	69.	O	AHREF	99.	S	$V656\_IN_7$
20.	N	Reserved (open)	50.	R	V_{SS}	70.	R	V_{SS}	100.	N	Reserved (open)
21.	N	Reserved (open)				71.	O	HSYNC_OUT			
22.	R	V_{DDPA}				72.	O	FIELD_OUT			
23.	R	SCLK				73.	O	VBNK_OUT			
24.	R	SDATA				74.	R	V_{DD}			
25.	R	$SA_{10/7}$				75.	O	HBNK_OUT			
26.	R	SA_0				76.	O	$V656\_OUT_0$			
27.	R	V_{SSPA}				77.	O	$V656\_OUT_1$			
28.	R	RESET				78.	R	V_{SS}			
29.	G	Reserved (GND)				79.	O	$V656\_OUT_2$			
30.	G	Reserved (GND)				80.	O	$V656\_OUT_3$			

Table 1: FS45x Pin Assignments

R = Signal Required
O = Signal if used, else no connect
S = Signal if used, else ground
G = Always Ground
N = Always No Connect

4.1 FS450 Û GCC Pin Mapping

The following table maps the FS450/1 pins to the host GCC controller chip. Please contact your FOCUS representative to obtain the most up-to-date reference schematics before initiating a design.

FS450 Pin #	FS450/1 Pin Name	Intel 82810 Pin Name UIM_MOD=0	National Cx5530 MediaGX UIM_MOD=3	nVidia Riva TNT Pin Name UIM_MOD=1	S3 Savage Pin Name UIM_MOD=1
31	VGA_CKOUT	TVCLKIN			
39	VGA_CKOUTTL		TVCLK	TVCLKIN	TVCLK
65	VGA_PCKIN	CLKOUT0			
64	VGA_NCKIN	CLKOUT1	FP_CLK	TVCLKOUT	TVCLKR
47	HSYNC_IN	TVHSYNC	FP_HSYNC_OUT		TVHS
46	VSYNC_IN	TVVSYNC	FP_VSYNC_OUT		TVVS
71	HSYNC_OUT			TVHSYNC	
68	VSYNC_OUT			TVVSYNC	
44	BLANK	BLANK			BLANK
48	P_0	LTVDATA0	FP_DATA6	TVD0	TVDAT0
49	P_1	LTVDATA1	FP_DATA7	TVD1	TVDAT1
51	P_2	LTVDATA2	FP_DATA8	TVD2	TVDAT2
52	P_3	LTVDATA3	FP_DATA9	TVD3	TVDAT3
53	P_4	LTVDATA4	FP_DATA10	TVD4	TVDAT4
54	P_5	LTVDATA5	FP_DATA11	TVD5	TVDAT5
57	P_6	LTVDATA6	FP_DATA12	TVD6	TVDAT6
58	P_7	LTVDATA7	FP_DATA13	TVD7	TVDAT7
59	P_8	LTVDATA8	FP_DATA14	TVD8	TVDAT8
60	P_9	LTVDATA9	FP_DATA15	TVD9	TVDAT9
62	P_{10}	LTVDATA10	FP_DATA16	TVD10	TVDAT10
63	P_{11}	LTVDATA11	FP_DATA17	TVD11	TVDAT11
43	E_0		FP_DATA0		
42	E_1		FP_DATA1		
41	E_2		FP_DATA2		
40	E_3		FP_DATA3		
37	E_4		FP_DATA4		
36	E_5		FP_DATA5		
23	SCLK	LTVCL	DDC_SCL	SPSCL	SPCLK1
24	SDATA	LTVDA	DDC_SDA	SPSDA	SPD1

Table 2: FS450 to GCC Pin Mapping

5. Pin Descriptions

Pin Name	Pin Number	Type/Value	Pin Function Description
Clocks			
VGA_CKOUT	31	GTLP output (open drain)	**VGA Clock Output.** Clock to GCC TVCLKIN. Synthesized from TV_CKIN. 27 to 85 MHz range.
VGA_CKOUTTL	39	LVTTL output	**VGA Clock Output.** Clock to GCC TVCLKIN. Synthesized from TV_CKIN. 27 to 85 MHz range.
VGA_PCKIN	65	GTLP input	**VGA Clock Input Positive Edge.** Clock from GCC CLKOUT, buffered form of VGA_CKOUT. Used to latch rising edge RGB data.
VGA_NCKIN	64	GTLP input	**VGA Clock Input Negative Edge.** Clock from GCC CLKOUT, buffered form of VGA_CKOUT. Used to latch negative edge RGB data.
TV_CKIN	1	LVTTL input	**Television Clock Input.** Clock for the CCIR 656 I/O and the video encoder. 27 MHz.
XTAL	2	LVTTL output	**Television Clock XTAL Output.** Buffered version of TV_CKIN. For use with a 27 MHz crystal.
HSYNC_OUT	71	LVTTL output	**HSYNC Output.** Output from FS450 to GCC to support slave mode operation.
VSYNC_OUT	68	LVTTL output	**VSYNC Output.** Output from FS450 to GCC to support slave mode operation.
Global Controls and Reserved Pins			
RESET	28	TTL input (pull down)	**Reset.** Active Low. Resets internal state machines and initializes default register values.
Reserved	5,29,30	TTL input (ground)	**Reserved Inputs.** Connect to V_{SS}.
Reserved	6,20,21, 34,35,100	LVTTL output (leave open)	**Reserved Outputs.** Do not connect.
Digital RGB Inputs			
P11-P0	63,62,60,59,58,57,54,53,52,51, 49,48	GTLP input	**Digital GTLP port input.** Digital video input, multiplexed or non-multiplexed. Connects to GCC's digital video out.
E5-E0	36,37,40,41,42,43	GTLP input	**Digital GTLP port input.** Non-multiplexed extended digital video input. Connects to GCC's digital video out.
GTL_REF	55	GTLP REF	**Digital GTLP Reference input.** Voltage threshold reference for GTLP inputs. Reference is 1.0 volts.
HSYNC_IN	47	GTLP input	**Digital HSYNC VGA input.** Connects to GCC TVHSYNC.
VSYNC_IN	46	GTLP input	**Digital VSYNC VGA input.** Connects to GCC TVVSYNC.
BLANK	44	GTLP input	**Digital BLANK VGA input.** True outside of GCC active area. Connects to GCC BLANK#.

Pin Name	Pin Number	Type/Value	Pin Function Description
Video Outputs			
Y/Red	12	analog video	**Video output.** As programmed by Command Register OFMT bit: 0 Luminance component Y of S-video. 1 Red component of RGB.
CVBS/Green	15	analog video	**Video output.** As programmed by Command Register OFMT bit: 0 Composite video. 1 Green component of RGB.
C/Blue	17	analog video	**Video output.** As programmed by Command Register OFMT bit: 0 Chrominance component of S-video. 1 Blue component of RGB.
CSYNC	19	LVTTL output	**Composite sync output.** Active high digital composite sync for SCART video outputs.
Voltage Reference			
V_{REF}	8	+1.276 V	**Voltage reference input/output.** If unconnected, except for a 0.1µF capacitor to ground for noise decoupling, the internal 1.276 Volt band-gap reference will be supplied to the three D/A Converters. An external 1.276 Volt reference connected to the V_{REF} pin, will override the internal voltage reference.
R_{REF}	9	390/780Ω	**Reference resistor.** Connected between R_{REF} and ground, this resistor sets the current range of the D/A converters. Use 390Ω for a 37.5Ω load and 780Ω for a 75Ω load.
C_{BYPASS}	11	0.1 µF	**Bypass Capacitor.** A 0.1µF capacitor must be connected between C_{BYPR} and V_{DDDA} to reduce noise at the D/A outputs.
CCIR 656 Input Port			
$V656\_IN_{7-0}$	99,98,97,96,94,93,92,91	TTL input (pull down)	**Digital CCIR 656 port input.** 8 bits wide. Y, Cr, Cb multiplexed digital input port
HBNK_IN	89	TTL input (pull down)	**Digital TV Horizontal Blank input.** Horizontal Blank for use with the V656_IN ports.
VBNK_IN	88	TTL input (pull down)	**Digital TV Vertical Blank input.** Vertical Blank for use with the V656_IN ports.
FIELD_IN	87	TTL input (pull down)	**Digital TV Field input.** Field bit for use with the V656_IN ports.

Pin Name	Pin Number	Type/Value	Pin Function Description
CCIR 656 Output Port			
$V656\_OUT_{7-0}$	85,84,83,81,80,79,77,76	LVTTL output	**Digital CCIR 656 port output.** 8 bits wide. Y, Cr, Cb multiplexed digital output port
HBNK_OUT	75	LVTTL output	**Digital TV Horizontal Blank output.** Horizontal Blank for use with the V656_OUT ports.
VBNK_OUT	73	LVTTL output	**Digital TV Vertical Blank output.** Vertical Blank for use with the V656_OUT ports.
FIELD_OUT	72	LVTTL output	**Digital TV Field output.** Field bit for use with the V656_OUT ports.
AHREF	69	LVTTL output	**Digital Auxiliary Horizontal Reference output.** Horizontal Sync for external hardware. Programmable advance or retard.
AVREF	67	LVTTL output	**Digital Auxiliary Vertical Reference output.** Vertical Sync for external hardware. Programmable advance or retard.
Serial Port			
SA10/7	25	TTL input (pull down)	**Serial address length select.** Selects the length of the serial address: SA10/7 = H: 10-bits SA10/7 = L: 7-bits
SA_0	26	TTL input (pull down)	**Serial data address bit 0.** . Selects the serial bus address: SA_0 = H: 0x6A, 276 SA_0 = L: 0x4A, 224
SDATA	24	TTL I/0 (open drain)	**Serial data.** Data line of the serial port. Connect to GCC LTVDA.
SCLK	23	TTL Input	**Serial clock.** Clock line of the serial port. Connect to GCC LTVCL.
Power and Ground			
V_{DDPA}	22	+3.3 V	**VGA_CKOUT Phase-locked loop Power**. Filtered +3.3 volt power for VGA_CKOUT phase locked loop.
V_{DDOSC}	3	+3.3 V	**TV Crystal Oscillator Power**. Filtered +3.3 volt power for TV XTAL oscillator.
V_{DD}	33,45,56,66,74,82,90	+3.3 V	**Digital Power.** 3.3 volt power for digital section of chip.
V_{DDDA}	10,13,16,18	+3.3 V	**D/A Converter Power.** Filtered +3.3 volt power for 10 bit video D/A converters.
V_{SSPA}	27	0 V	**VGA_CKOUT phase-locked loop ground.**
V_{SSOSC}	4	0 V	**TV Crystal Oscillator ground.**
V_{SS}	32,38,50,61,70,78,86,95	0 V	**Digital ground.** +3.3 volt power return.
V_{SSDA}	7,14	0 V	**D/A Converter Ground.**

6. Control Register Definitions

6.1 Control Register Map

Function				
Reg.	**Bit #**	**Name**	**Type**	**Reset Value**
Input Horizontal Offset				
0	7-0	IHO_{7-0}	R/W	00
1	2-0	IHO_{10-8}	R/W	00
Input Vertical Offset				
2	7-0	IVO_{7-0}	R/W	00
3	2-0	IVO_{10-8}	R/W	00
Input Horizontal Width				
4	7-0	IHW_{7-0}	R/W	D0 (720.)
5	1-0	IHW_{9-8}	R/W	02
Vertical Scaling Coefficient				
6	7-0	VSC_{7-0}	R/W	00
7	7-0	VSC_{15-8}	R/W	00
Horizontal Down/Up Scaling Coefficients				
8	7-0	$HDSC_{7-0}$	R/W (Down)	00
9	7-0	$HUSC_{7-0}$	R/W (Up)	00
Command Register				
C	7-0	CR_{7-0}	R/W	00
D	7-0	CR_{15-8}	R/W	10
Status Port				
E	7-0	SP_{7-0}	R	00
F	-	-	R	00
Numerator of NCO Low Word				
10	7-0	$NCON_{7-0}$	R/W	00 (131,072.)
11	7-0	$NCON_{15-8}$	R/W	00
Numerator of NCO High Word				
12	7-0	$NCON_{23-16}$	R/W	02
13	-	-		
Denominator of NCO Low Word				
14	7-0	$NCOD_{7-0}$	R/W	00 (524,288.)
15	7-0	$NCOD_{15-8}$	R/W	00
Denominator of NCO High Word				
16	7-0	$NCOD_{23-16}$	R/W	08
17	-	-		
Auxiliary Pixel Offset				
18	7-0	APO_{7-0}	R/W	00
19	1-0	APO_{9-8}	R/W	00
Auxiliary Line Offset				
1A	6-0	ALO_{6-0}	R/W	00
1B	-	-	R/W	00
Auxiliary Field Offset				
1C	0	AFO	R/W	00
1D	-	-		00
HSync Pulse Width				
1E	7-0	$HSOUTWID_{7-0}$	R/W	00
1F	2-0	$HSOUTWID_{10-8}$	R/W	00

Function				
Reg.	**Bit #**	**Name**	**Type**	**Reset Value**
HSync Starting Edge				
20	7-0	$HSOUTST_{7-0}$	R/W	00
21	2-0	$HSOUTST_{10-8}$	R/W	00
HSync Ending Edge				
22	7-0	$HSOUTEND_{7-0}$	R/W	00
23	2-0	$HSOUTEND_{10-8}$	R/W	00
Flicker Filter Sharpness				
24	4-0	SHP_{4-0}	R/W	00
25	-	-	-	00
Flicker Filter				
26	4-0	FLK_{4-0}	R/W	00
27	-	-	-	00
Part Revision				
32	7-0	REV_{7-0}	R/W	01
33	7-0	REV_{15-8}	R/W	00
Misc Register				
34	7-0	$MISC_{7-0}$	R/W	00
35	7-0	$MISC_{15-8}$	R/W	80
FIFO Status Port Full/FIFO Status Port Empty				
36	7-0	$FIFOF_{7-0}$	R/W	00
37	7-0	$FIFOE_{7-0}$	R/W	00
FIFO Latency				
38	7-0	$FIFOL_{7-0}$	R/W	00
39	7-0	$FIFOL_{15-8}$	R/W	00
VSync Pulse Width				
3A	7-0	$VSOUTWID_{7-0}$	R/W	00
3B	2-0	$VSOUTWID_{10-8}$	R/W	00
VSync Starting Edge				
3C	7-0	$VSOUTST_{7-0}$	R/W	00
3D	2-0	$VSOUTST_{10-8}$	R/W	00
VSync Ending Edge				
3E	7-0	$VSOUTEND_{7-0}$	R/W	00
3F	2-0	$VSOUTEND_{10-8}$	R/W	00

Function				
Reg.	**Bit #**	**Name**	**Type**	**Reset Value**
Chroma Frequency				
40	7-0	CHR_FREQ_{31-24}	R/W	21 (569,408,543.)
41	7-0	CHR_FREQ_{23-16}	R/W	F0
42	7-0	CHR_FREQ_{15-8}	R/W	7C
43	7-0	CHR_FREQ_{7-0}	R/W	1F
Chroma Phase, Miscellaneous Bits 45				
44	7-0	CHR_PHASE_{7-0}	R/W	00
45	1,0	MISC45	R/W	00
Miscellaneous Bits 46, 47				
46	7-0	MISC46	R/W	05
47	3-0	MISC47	R/W	00
HSync Width, Burst Width				
48	7-0	$HSYNC\_WID_{7-0}$	R/W	7E (126.)
49	6-0	$BURST\_WID_{6-0}$	R/W	44 (68.)
Backporch Width, CB Burst Level				
4A	7-0	$BPORCH_{7-0}$	R/W	76 (118.)
4B	7-0	CB_BURST_{7-0}	R/W	3B (59.)
CR Burst Level, Miscellaneous Bits 4D				
4C	7-0	CR_BURST_{7-0}	R/W	00
4D	1-0	MISC4D	R/W	00
Black Level				
4E	7-0	$BLACK\_LVL_{9-2}$	R/W	86 (282.)
4F	1-0	$BLACK\_LVL_{1-0}$	R/W	02
Blank Level				
50	7-0	$BLANK\_LVL_{9-2}$	R/W	3C (240.)
51	1-0	$BLANK\_LVL_{1-0}$	R/W	00
Number Lines				
57	7-0	$LINE\_FRAME_{9-2}$	R/W	83 (525.)
58	1-0	$LINE\_FRAME_{1-0}$	R/W	01
White Level				
5E	7-0	$WHITE\_LVL_{9-2}$	R/W	C8 (800.)
5F	1-0	$WHITE\_LVL_{1-0}$	R/W	00
Cb Gain				
60	7-0	CB_GAIN_{7-0}	R/W	22 (137.)
61	-	-	R/W	01
Cr Gain				
62	7-0	CR_GAIN_{7-0}	R/W	22 (137.)
63	-	-	R/W	01
Chroma Tint Adjustment				
64	-	-	R/W	00
65	7-0	$TINT_{7-0}$	R/W	00
Status Port				
68	-	-	R/W	00
69	4-0	$BREEZE\_WAY_{4-0}$	R/W	16 (22.)
Status Port				
6C	5-0	$FRNT\_PORCH_{5-0}$	R/W	20 (32.)
6D	-	-	R/W	00

Function				
Reg.	**Bit #**	**Name**	**Type**	**Reset Value**
ActiveLine				
71	7-0	$ACTIVELINE_{10-3}$	R/W	B4 (1440.)
72	2-0	$ACTIVELINE_{2-0}$	R/W	00
Chroma Phase				
73	7-0	$FIRST\_LINE_{7-0}$	R/W	15 (21.)
Miscellaneous Bits 74, Sync Level				
74	7-0	MISC74	R/W	02
75	7-0	$SYNC\_LVL_{7-0}$	R/W	48 (72.)
VBI Blank Level				
7C	7-0	$VBIBLNK\_LVL_{9-2}$	R/W	4A (296.)
7D	1-0	$VBIBLNK\_LVL_{1-0}$	R/W	00
Reset, Encoder Version				
7E	0	SOFT_RST	R/W	1
7F	7-0	ENC_VER_{7-0}	R	20
Miscellaneous Bits 80, WSS Clock Frequency (upper)				
80	6-0	MISC80	R/W	7
81	7-0	WSS_CLK_{11-4}	R/W	2F (759.)
WSS Clock Frequency (lower), WSS Data Field 1 (upper)				
82	3-0	WSS_CLK_{3-0}	R/W	07
83	7-0	WSS_DAT1_{19-12}	R/W	00
WSS Data Field 1 (lower)				
84	7-0	WSS_DAT1_{11-4}	R/W	00
85	3-0	WSS_DAT1_{3-0}	R/W	00
WSS Data Field 0 (upper)				
86	7-0	WSS_DAT0_{19-12}	R/W	00
87	7-0	WSS_DAT0_{11-4}	R/W	00
WSS Data Field 0 (lower), WSS Line 1 Delay				
88	3-0	WSS_DAT0_{3-0}	R/W	00
89	7-0	WSS_LINF1_{7-0}	R/W	00
WSS Level (lower)				
8A	7-0	WSS_LINF0_{7-0}	R/W	00
8B	7-0	WSS_LVL_{9-2}	R/W	FF (1023.)
WSS Level (upper), Miscellaneous Bits 8D				
8C	1-0	WSS_LVL_{1-0}	R/W	03
8D	4-0	$MISC8D_{4-0}$	R/W	00

6.2 Control Register Definitions

In the following definitions, range is defined as:

{min value : [max value]}

Please note that registers 0-3F use the little endian numbering scheme while registers 40-8D use the big endian numbering scheme.

6.2.1 IHO - Input Horizontal Offset

Input Horizontal Offset Low (0)

7	6	5	4	3	2	1	0
IHO_7	IHO_6	IHO_5	IHO_4	IHO_3	IHO_2	IHO_1	IHO_0

Input Horizontal Offset High (1)

7	6	5	4	3	2	1	0
0	0	0	0	0	IHO_{10}	IHO_9	IHO_8

Reg	Bit#	Bit Name	Description
1, 0	2-0, 7-0	IHO_{10-0}	**Input horizontal offset bits [10-0].** Horizontal displacement of the image in pixels from the leading edge of horizontal sync. IHO is an unsigned number.

Range: {0 : [Total Pixels/Line]-1}

6.2.2 IVO - Input Vertical Offset

Input Vertical Offset Low (2)

7	6	5	4	3	2	1	0
IVO_7	IVO_6	IVO_5	IVO_4	IVO_3	IVO_2	IVO_1	IVO_0

Input Vertical Offset High (3)

7	6	5	4	3	2	1	0
0	0	0	0	0	IVO_{10}	IVO_9	IVO_8

Reg	Bit#	Bit Name	Description
3, 2	2-0, 7-0	IVO_{10-0}	**Input vertical offset bits [10:0].** Vertical displacement of the image in lines from the leading edge of vertical sync plus a one line bias. IVO is an unsigned number.

Range: {0 : [Total Lines/Frame]-1}

6.2.3 IHW - Input Horizontal Width

Input Horizontal Width Low (4)

7	6	5	4	3	2	1	0
IHW_7	IHW_6	IHW_5	IHW_4	IHW_3	IHW_2	IHW_1	IHW_0

Input Horizontal Width High (5)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	IHW_9	IHW_8

Reg	Bit#	Bit Name	Description
5, 4	1-0, 7-0	IHW_{9-0}	**Input horizontal width [9:0].** Total number of active VGA pixels per line. IHW is an unsigned number.

Range: {0 : 970}

6.2.4 VSC – Vertical Scaling Coefficient

Vertical Scaling Coefficient (6)

7	6	5	4	3	2	1	0
VSC_7	VSC_6	VSC_5	VSC_4	VSC_3	VSC_2	VSC_1	VSC_0

Vertical Scaling Coefficient (7)

7	6	5	4	3	2	1	0
VSC_{15}	VSC_{14}	VSC_{13}	VSC_{12}	VSC_{11}	VSC_{10}	VSC_9	VSC_8

Reg	Bit#	Bit Name	Description
7, 6	7-0	VSC_{7-0}	**Vertical scaling coefficient bits [15:0].** Vertical down scaling factor = (1 + VSC/65,536). VSC is a two's complement number. If VSC => 0, then the image is not effected.

Range: { [-32,769]:0}

6.2.5 HDSC, HUSC – Horizontal Down/Up Scaling Coefficients

Horizontal Down Coefficient (8)

7	6	5	4	3	2	1	0
$HDSC_7$	$HDSC_6$	$HDSC_5$	$HDSC_4$	$HDSC_3$	$HDSC_2$	$HDSC_1$	$HDSC_0$

Horizontal Up Coefficient (9)

7	6	5	4	3	2	1	0
$HUSC_7$	$HUSC_6$	$HUSC_5$	$HUSC_4$	$HUSC_3$	$HUSC_2$	$HUSC_1$	$HUSC_0$

Reg	Bit#	Bit Name	Description
8	7-0	$HDSC_{7-0}$	**Horizontal down scaling coefficient bits [7:0].** Horizontal down scaling factor = (1 + VSC/128). HDSC is a two's complement number. If HDSC => 0, then the image is not effected.
9	7-0	$HUSC_{7-0}$	**Horizontal up scaling coefficient bits [7:0].** Horizontal up scaling factor = (1 + VSC/128). HDSC is a two's complement number. If HDSC <= 0, then the image is not effected.

HDSC Range: { [-63]:0 }

HUSC Range: { 0:127 }

6.2.6 CR - Command Register

Command Register (C)

7	6	5	4	3	2	1	0
FFO_CLR	CACQ_CLR	LP_EN	YCOFF	COMPOFF	NCO_EN	CLKOFF	SRESET

Command Register (D)

7	6	5	4	3	2	1	0
UIM_MOD_1	UIM_MOD_0	0	UIM_DEC	UIM_CLK	OFMT	STD_VMI	NTSC_PALIN

Reg	Bit#	Bit Name	Description
C	0	SRESET	**Soft Reset.** Resets the FS450.
C	1	CLKOFF	**Clock Off.** Turns off FS450 clock to minimize power.
C	2	NCO_EN	**Enable NCO Latch.** When this bit is set, transfers the NCO words from the I2C registers into the NCO. The NCO synthesizes the VGA clock from the 27MHz FS450 clock. This clock must be adjusted so the VGA scaled input data rate exactly matches the CCIR 656 data output rate.
C	3	COMPOFF	**Composite (CVBS) Output Off.** Turns off the CVBS output D/A.
C	4	YCOFF	**SVideo (YC) Outputs Off.** Turns off the YC output D/As.
C	5	LP_EN	**Loop Through Enable.** Enables the CCIR 656 data on the output port to loop directly to the input port (no external routing).
C	6	CACQ_CLR	**Counter Acquisition Flag Clear.** Setting this bit clears the Counter Acquisition Flag.
C	7	FFO_CLR	**FIFO Clear.** Setting this bit clears the FIFO depth registers and the FIFO State register.
D	0	NTSC_PALIN	**CCIR 656 PAL or NTSC Input.** Sets the number of lines written through the FIFO. When set, the number of lines is 576 for PAL, when clear, 487 lines for NTSC.
D	1	STD_VMI	**Standard or VMI 656 Input Control.** Select standard (external pins) horizontal/vertical blank and field codes or inserted CCIR 601/656 SAV/EAV (Start/End Active Video) embedded codes.
D	2	OFMT	**Output Format Control.** Switches between RGB or Composite/YC output. When set, the output is RGB.
D	3	UIM_CLK	**Universal Interface Mux Clock Mode.** If set, input pixels are clocked in on the falling edge of the P and N input clocks. If clear, input pixels are clocked on the rising and falling edge of N clock.
D	4	UIM_DEC	**Universal Interface Mux Decimator.** Turns on the horizontal prescaler divide by 2 to support XGA mode.
D	7,6	UIM_MOD_{1-0}	**Universal Interface Mode Select.** Selects the VGA interface mode (see table below).

Notes:

VMI 656 Input Control: If the Video Module Interface (VMI) mode is specified, SAV and EAV commands are inserted into the CCIR601 data stream to coordinate down stream data processing. The SAV and EAV Control words have the following format:

YC Data	D7	D6	D5	D4	D3	D2	D1	D0
Preamble C	1	1	1	1	1	1	1	1
Preamble Y	0	0	0	0	0	0	0	0
Status Word C	0	0	0	0	0	0	0	0
Status Word Y	1	F	V	H	P3	P2	P1	P0

Table 3: SAV and EAV Control Words

F = 0 during field 1, F = 1 during field 2
H = 0 for SAV, H = 1 for EAV
V = 1 during vertical blanking

P3 = V xor H
P2 = F xor H
P1 = F xor V
P0 = F xor V xor H

UIM_MOD Mapping: The UIM_MOD (Universal Input Mux, UIM) bits select the mode for P0-P11 and E0-E5. The intention is to support as many different 3D and GCC graphic controllers, CPU support chips and integrated CPUs as possible (collectively referred to in this data sheet as "GCC"). The following table shows the mapping in each mode for the digital RGB from the GCC to the appropriate port or extended port pin:

UIM_MOD	0	0	1	1	1	1	2	2	3	3	3
P/E Port	M888DL	M888DH	M888IL	M888IH	M565IL	M565IH	M555L	M555H	N666	N565	N555
P11	G3	R7	G4	R7	G2	R4	G2	X	R5	R4	R4
P10	G2	R6	G3	R6	G1	R3	G1	R4	R4	R3	R3
P9	G1	R5	G2	R5	G0	R2	G0	R3	R3	R2	R2
P8	G0	R4	B7	R4	B4	R1	B4	R2	R2	R1	R1
P7	B7	R3	B6	R3	B3	R0	B3	R1	R1	R0	R0
P6	B6	R2	B5	G7	B2	G5	B2	R0	R0	0	0
P5	B5	R1	B4	G6	B1	G4	B1	G4	G5	G5	G4
P4	B4	R0	B3	G5	B0	G3	B0	G3	G4	G4	G3
P3	B3	G7	G0	R2	0	0	X	X	G3	G3	G2
P2	B2	G5	B2	R1	0	0	X	X	G2	G2	G1
P1	B1	G4	B1	R0	0	0	X	X	G1	G1	G0
P0	B0	G3	B0	G1	0	0	X	X	G0	G0	0
E5	X	X	X	X	X	X	X	X	B5	B4	B4
E4	X	X	X	X	X	X	X	X	B4	B3	B3
E3	X	X	X	X	X	X	X	X	B3	B2	B2
E2	X	X	X	X	X	X	X	X	B2	B1	B1
E1	X	X	X	X	X	X	X	X	B1	B0	B0
E0	X	X	X	X	X	X	X	X	B0	0	0

Table 4: GCC Port Mapping (UIM_MOD)

1) All input bits are MSB justified
2) Shaded modes require zero padding at input port
3) For GCC to P/E Mapping, see Table 2

6.2.7 SP - Status Port

Status Port Low (E)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FIFO_ST	CACQ_ST

Status Port High (F)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Reg	Bit#	Bit Name	Description
E	0	CACQ_ST	**Cache Status.** Status of horizontal downscaler cache (=1 if over flowed).
E	1	FIFO_ST	**FIFO Status.** Output FIFO status (=1 if over/under flowed).

Notes:

FIFO Status:

FS450 does not have a frame memory. In FS450 the scaled input data rate and the output data rates are the same. The FIFO takes up the slack during the asynchronous horizontal blanking interval of the input and output. The FIFO depth (1024) is only slightly larger that the 720 output pixels required to form a CCIR 601 data stream. The extra pixels are used for data overrun protection.

At the coincidence of a Filtered Horizontal and Vertical Start, the input and output FIFO pointers are reset to the to beginning of the memory and data writes commence. Next, 24 output clock cycles after the Filtered Horizontal and Vertical Start occur, the CCIR 656 Timing Generator issues a FIFO Horizontal and Vertical Start. This causes the Horizontal Upscaler to issue a TV read and the FIFO starts to read data.

If a data overrun occurs, the offending FIFO's pointer is halted and black is output to the Horizontal Upscaler. Also, the FIFO data overrun flag is set.

6.2.8 NCON - Numerator of NCO Word

Numerator of NCO Word (10)

7	6	5	4	3	2	1	0
$NCON_7$	$NCON_6$	$NCON_5$	$NCON_4$	$NCON_3$	$NCON_2$	$NCON_1$	$NCON_0$

Numerator of NCO Word (11)

7	6	5	4	3	2	1	0
$NCON_{15}$	$NCON_{14}$	$NCON_{13}$	$NCON_{12}$	$NCON_{11}$	$NCON_{10}$	$NCON_9$	$NCON_8$

Numerator of NCO Word (12)

7	6	5	4	3	2	1	0
$NCON_{23}$	$NCON_{22}$	$NCON_{21}$	$NCON_{20}$	$NCON_{19}$	$NCON_{18}$	$NCON_{17}$	$NCON_{16}$

Numerator of NCO Word (13)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Reg	Bit#	Bit Name	Description
12, 11, 10	7-0,7-0,7-0	$NCON_{23-0}$	**Numerator of NCO Word [23:0].** Numerator of clock synthesizer to generate VGA input clock. NCON is a 24 bit unsigned number.

Range: {0 : NCOD/2}

The FS450 synthesizes a 27-85 MHz clock from the 27 MHz TV_CKIN and supplies this clock (VGA_CKOUT) to the GCC. This clock is buffered and returned to the FS450 (VGA_CKIN) synchronous to the RGB data and Sync information. This clock has a 1.5 Hz resolution and can be adjusted so the VGA scaled input data rate exactly matches the CCIR 656 data output rate.

Frequency VGA / Frequency 656 = # VGA Pixels / # 656 Pixels x # VGA Lines / # 656 Lines

Frequency VGA / Frequency 656 = NCON / NCOD x M / N

Example: for SVGA mode, typ. total pixels x lines ~ 1024 x 625; let M=512, N=128:

NTSC and PAL: NCON = 1024 x 625 = 640,000

6.2.9 NCOD - Denominator of NCO Word

Denominator of NCO Word (14)

7	6	5	4	3	2	1	0
$NCOD_7$	$NCOD_6$	$NCOD_5$	$NCOD_4$	$NCOD_3$	$NCOD_2$	$NCOD_1$	$NCOD_0$

Denominator of NCO Word (15)

7	6	5	4	3	2	1	0
$NCOD_{15}$	$NCOD_{14}$	$NCOD_{13}$	$NCOD_{12}$	$NCOD_{11}$	$NCOD_{10}$	$NCOD_9$	$NCOD_8$

Denominator of NCO Word (16)

7	6	5	4	3	2	1	0
$NCOD_{23}$	$NCOD_{22}$	$NCOD_{21}$	$NCOD_{20}$	$NCOD_{19}$	$NCOD_{18}$	$NCOD_{17}$	$NCOD_{16}$

Denominator of NCO Word (17)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Reg	Bit#	Bit Name	Description
16, 15, 14	7-0,7-0,7-0	$NCOD_{23-0}$	**Denominator of NCO Word [23:0].** Denominator of clock synthesizer to generate VGA input clock. NCOD is a 24 bit unsigned number.

Range: {NCON*2 : (2^{24}-1)}

The FS450 synthesizes a 27-85 MHz clock from the 27 MHz TV_CKIN and supplies this clock (VGA_CKOUT) to the GCC. This clock is buffered and returned to the FS450 (VGA_CKIN) synchronous to the RGB data and Sync information. This clock has a 1.5 Hz resolution and can be adjusted so the VGA scaled input data rate exactly matches the CCIR 656 data output rate.

Frequency VGA / Frequency 656 = # VGA Pixels / # 656 Pixels x # VGA Lines / # 656 Lines

Frequency VGA / Frequency 656 = NCON / NCOD x M / N

Example: for SVGA mode, typ. total pixels x lines ~ 1024 x 625; let M=512, N=128:

NTSC: NCOD = 858 x 525 x 512 / 128 = 1,801,800

PAL: NCOD = 864 x 625 x 512 / 128 = 2,160,000

6.2.10 APO, ALO, AFO - Auxiliary Pixel, Line, and Field Offsets

Auxiliary Pixel Offset Low (18)

7	6	5	4	3	2	1	0
APO_7	APO_6	APO_5	APO_4	APO_3	APO_2	APO_1	APO_0

Auxiliary Pixel Offset High (19)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	APO_9	APO_8

Auxiliary Line Offset (1A)

7	6	5	4	3	2	1	0
-	ALO_6	ALO_5	ALO_4	ALO_3	ALO_2	ALO_1	ALO_0

Not Used (1B)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Auxiliary Field Offset (1C)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	AFO_0

Not Used (1D)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Reg	Bit#	Bit Name	Description
19, 18	9-0	APO_{9-0}	**Auxiliary Pixel Offset [9:0].** Number of 27MHz cycles of delay/advance of the Auxiliary Video Reference signals. APO is a 10 bit signed number.
1A	6-0	ALO_{6-0}	**Auxiliary Line Offset [6:0].** Number of lines of delay/advance of the Auxiliary Video Reference signals. AFO is a 7 bit signed number.
1C	0	AFO	**Auxiliary Field Offset [0].** Inverts the field of the Auxiliary Video Reference signals.

APO Range: {-512 : 511}, **ALO Range:** {-64 : 63}, **AFO Range:** {0 : 1}

6.2.11 HSOUTWID, HSOUTST, HSOUTEND - HSync Out Width, Starting and Ending Edge

HSync Out Width Low (1E)

7	6	5	4	3	2	1	0
$HSOUTWID_7$	$HSOUTWID_6$	$HSOUTWID_5$	$HSOUTWID_4$	$HSOUTWID_3$	$HSOUTWID_2$	$HSOUTWID_1$	$HSOUTWID_0$

HSync Out Width High (1F)

7	6	5	4	3	2	1	0
0	0	0	0	0	$HSOUTWID_{10}$	$HSOUTWID_9$	$HSOUTWID_8$

HSync Out Starting Edge Low (20)

7	6	5	4	3	2	1	0
$HSOUTST_7$	$HSOUTST_6$	$HSOUTST_5$	$HSOUTST_4$	$HSOUTST_3$	$HSOUTST_2$	$HSOUTST_1$	$HSOUTST_0$

HSync Out Starting Edge High (21)

7	6	5	4	3	2	1	0
0	0	0	0	0	$HSOUTST_{10}$	$HSOUTST_9$	$HSOUTST_8$

HSync Out Ending Edge Low (22)

7	6	5	4	3	2	1	0
$HSOUTEND_7$	$HSOUTEND_6$	$HSOUTEND_5$	$HSOUTEND_4$	$HSOUTEND_3$	$HSOUTEND_2$	$HSOUTEND_1$	$HSOUTEND_0$

HSync Out Ending Edge High (23)

7	6	5	4	3	2	1	0
0	0	0	0	0	$HSOUTEND_{10}$	$HSOUTEND_9$	$HSOUTEND_8$

Reg	Bit#	Bit Name	Description
1F, 1E	10-0	$HSOUTWID_{10-0}$	**HSync Out Width [10:0].** Width of HSync Out during a frame.
21, 20	10-0	$HSOUTST_{10-0}$	**HSync Starting Edge [10:0].** Starting edge of HSync Out during a frame.
23, 22	10-0	$HSOUTEND_{10-0}$	**HSync Ending Edge [10:0].** Ending edge of HSync Out during a frame.

Range of HSOUTWID, HSOUTST, and HSOUTEND: {0 : 2048}

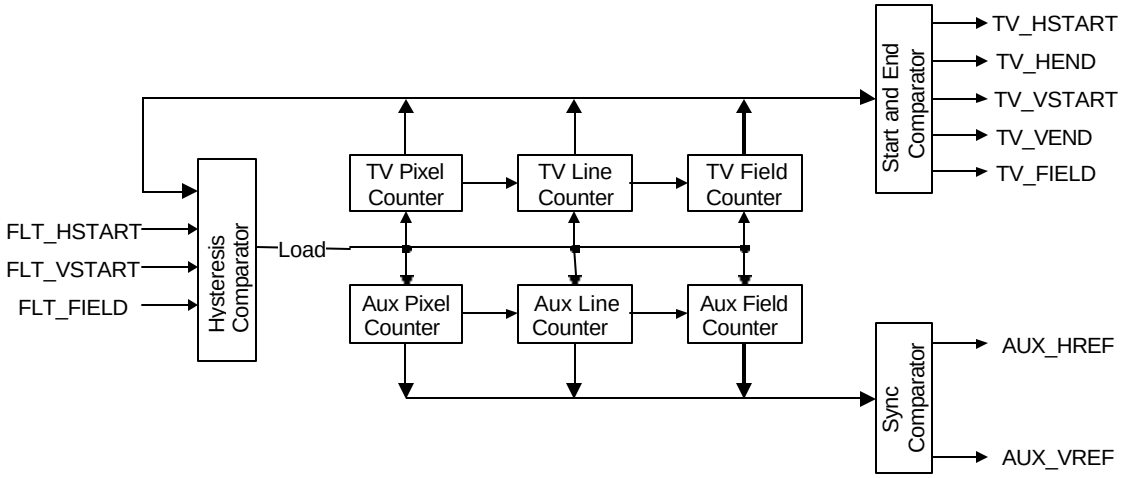


Figure 8: CCIR 656 Timing Block Diagram

The TV and Auxiliary Pixel/Line/Field Counters are freewheeling counters that are only loaded/reloaded during an error condition. If the value of the TV Pixel/Line/Field Counters are within 4 TV pixels of the ideal values during a Frame Start, no adjustment to the freewheeling counters are made. However, if the values exceeds 4 pixels (150 nsec) the ideal values, the TV Pixel/Line/Field Counters are reloaded and the TV Counter Acquisition Flag is set.

When the TV Pixel/Line/Field Counters are reloaded, the Auxiliary Pixel/Line/Field Counters are also reloaded. However, their load values are offset from the TV counter by the Auxiliary Pixel, Line, and Field Offset values stored in its I2C registers (APO, ALO, and AFO). From these counters the Auxiliary Horizontal and Vertical Syncs are formed. This feature allows a user to program advance timing signals to compensate for external hardware processing latency when doing a mix/overlay with FS450's CCIR 656 input and output.

The FIFO Latency register delays the Frame Start occurrence by 4x its value in 27MHz clock cycles. This delays the output 656 timing with respect to the input VGA timing and allows the FS450's FIFO to fill appropriately before a FIFO read is initiated.

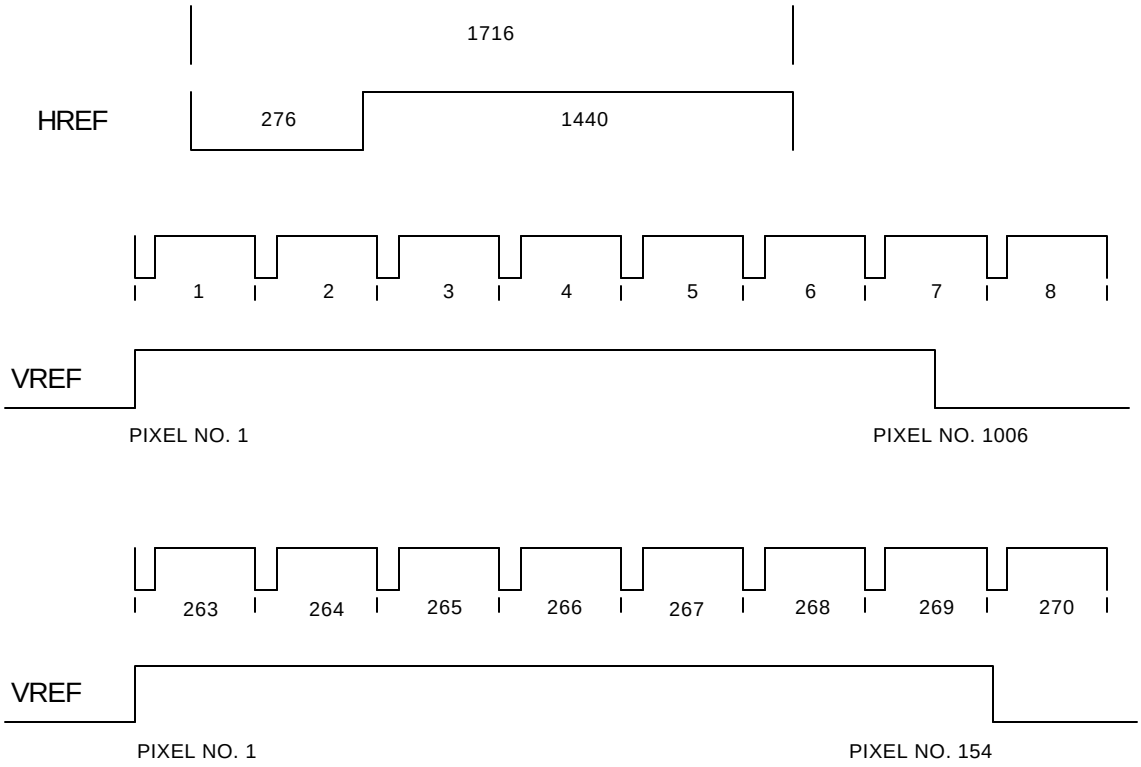


Figure 9: Auxiliary NTSC Reference Signals

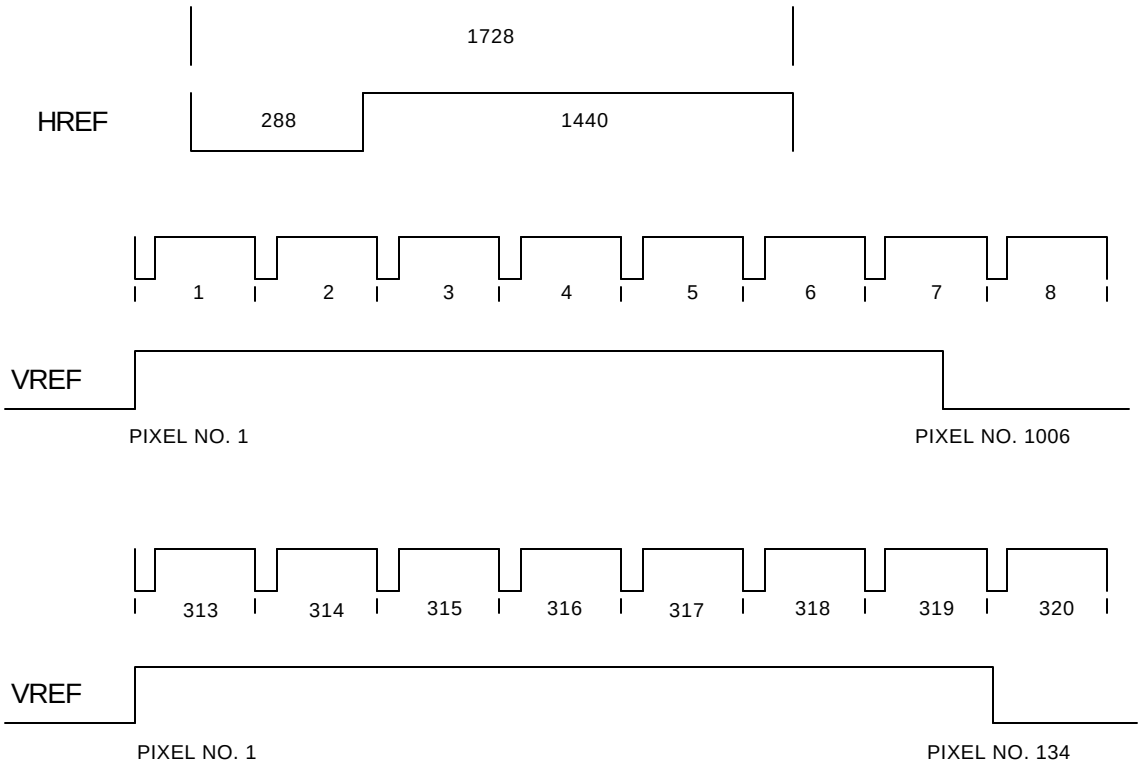


Figure 10: Auxiliary PAL Reference Signals

6.2.12 SHP, FLK - Sharpness and Flicker Filter

Sharpness Low (24)

7	6	5	4	3	2	1	0
0	0	0	SHP_4	SHP_3	SHP_2	SHP_1	SHP_0

Sharpness High (25)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Reg	Bit#	Bit Name	Description
24	4-0	SHP_{4-0}	**Flicker Filter Sharpness [4-0].** SHP accentuates the joint high vertical - high horizontal frequencies to sharpen edges. SHP is an unsigned number.

Range: {0 : 31} Provides 0 to 31/16 (6 dB) joint high horizontal and vertical frequency boost.

Flicker Filter Coefficient Low (26)

7	6	5	4	3	2	1	0
0	0	0	FLK_4	FLK_3	FLK_2	FLK_1	FLK_0

Flicker Filter Coefficient Low (27)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Reg	Bit#	Bit Name	Description
26	4-0	FLK_{4-0}	**Flicker Filter Coefficient [4:0].** Provides weighting factor for 3 line flicker filter. FLK is an unsigned number.

Range: {0 : 23}

Notes:
The FS450 Flicker Filter is more complex than a Three Line Average (TLA) flicker filter. The FS450 flicker filter includes a variable vertical filter response in addition to a sharpness function. Adjusting the FLK Coefficient modifies the vertical filter from no filtering (FLK = 0) to a Three Line Average (FLK = 16), giving the user the best choice in filtering options.

In addition to the variable vertical settings, the FS450 flicker filter has a sharpness function. This function is a two dimensional peaking function which accentuates the joint high vertical - high horizontal spatial frequencies (an "edge enhancer"). The three line variable two dimensional flicker filter is formed by summing the unit impulse function with a vertical flicker function scaled by FLK (Flicker Coefficient) and the peaking function which is scaled by SHP (Sharpness Coefficient). The FLK and SHP variables have 5 bits of resolutions, with a usable a range from 0 to 16/16 for FLK, and 0 to 31/16 for SHP.

6.2.13 REV - Revision Number

Part Number (32)

7	6	5	4	3	2	1	0
REV_7	REV_6	REV_5	REV_4	REV_3	REV_2	REV_1	REV_0

Revision Number (33)

7	6	5	4	3	2	1	0
REV_{15}	REV_{14}	REV_{13}	REV_{12}	REV_{11}	REV_{10}	REV_9	REV_8

Reg	Bit#	Bit Name	Description
33,32	15-0	REV_{15-0}	**Revision Number [15:0].** Identifies the revision for software ID purposes (Rev A = 0, Rev B = 1).

6.2.14 MISC - Miscellaneous Bits 34, 35 Register

Miscellaneous Bits Register (34)

7	6	5	4	3	2	1	0
0	0	NCO_LOAD_1	NCO_LOAD_0	0	0	0	0

Miscellaneous Bits Register (35)

7	6	5	4	3	2	1	0
GTLIO_PD	0	0	0	0	0	VGACKDIV	0

Reg	Bit#	Bit Name	Description
34	5,4	NCO_LOAD_{1-0}	**NCO Load Control Bits.** The PLL M and N dividers and the NCO Numerator (NCON) and denominator (NCOD) share the same address (separate memory). The NCO Load Control bits determine which registers are loaded when the NCON and NCOD registers are written (see table below). M uses the lower 11 bits of NCON, and N uses the lower 11 bits of NCOD.
35	1	VGACKDIV	**VGA Clock Divide.** Setting this bit divides the internal clock by 2 when the VGA input is in decimation (for XGA) mode.
35	7	GTLIO_PD	**GTL I/O Power Down.** Setting this bit puts all the GTL pins into power down mode.

Notes:

NCO_LOAD	Meaning
0	Load NCO Numerator and Denominator only.
1	Load M and N PLL Dividers only.
2	Load NCO Numerator and Denominator and set M=512, N=128.
3	Load M and N PLL Dividers and set NCO Numerator and Denominator both to 50.

Table 5: NCO_LOAD Control Bits

1) M is loaded with the desired value -2
2) N is loaded with the desired value -1
3) Using the 24 bit NCON and NCOD yields a very fine frequency resolution of 1.5 Hz but dithers the clock. The speed of the clock dither is sufficiently limited by the narrowband (around 5 kHz) PLL to prevent any problem with data transfers to the FS450. In fact, it provides an advantage for passing EMI certification and behaves much like off the shelf dithered clocks designed specifically for that purpose.
4) Using the 11 bit M/N ratio gives a frequency resolution of 13 kHz, but it has no dithering. This is ideal for dual VGA monitor and TV applications. Dithering the clock to a VGA controller makes the lines wiggle on the connected VGA monitor, making it difficult to read. This however limits the scaling possibilities, and close attention has to be paid to the factors of the VGA/TV pixels and lines so that they cancel down to 11 bit M and N numbers.
5) Both M/N and Numerator/Denominator can be used together, to generate a compromise performance.

6.2.15 FIFOL, FIFOH - FIFO Status Port Full/Empty

FIFO Status Port Full (36)

7	6	5	4	3	2	1	0
$FFOL_7$	$FFOL_6$	$FFOL_5$	$FFOL_4$	$FFOL_3$	$FFOL_2$	$FFOL_1$	$FFOL_0$

FIFO Status Port Empty (37)

7	6	5	4	3	2	1	0
$FFOH_7$	$FFOH_6$	$FFOH_5$	$FFOH_4$	$FFOH_3$	$FFOH_2$	$FFOH_1$	$FFOH_0$

Reg	Bit#	Bit Name	Description
36	7-0	$FFOL_{7-0}$	**FIFO Status Port Full [7:0].** Maximum number of FIFO memory locations underrun during the VGA image (multiply by 4 to get number of pixels corrupted). Unsigned number.
37	7-0	$FFOH_{7-0}$	**FIFO Status Port Empty [7:0].** Maximum number of FIFO memory locations used during a VGA frame (multiply by 4 to get number of pixels filled). Unsigned number.

Range: {0 : 255}

6.2.16 FFO_LAT - FIFO Latency

FIFO Latency Low (38)

7	6	5	4	3	2	1	0
FFO_LAT_7	FFO_LAT_6	FFO_LAT_5	FFO_LAT_4	FFO_LAT_3	FFO_LAT_2	FFO_LAT_1	FFO_LAT_0

FIFO Latency High High (39)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Reg	Bit#	Bit Name	Description
38	7-0	FFO_LAT_{7-0}	**FIFO Latency [7:0].** Number of output clock cycles between the initiation of VGA writes to the FIFO memory and the TV reads from it. Multiply by 4 to get the number of 27 MHz clock delays.

Range: {0 : 255}

6.2.17 VSOUTWID, VSOUTST, VSOUTEND - VSync Out Width, Starting and Ending Edge

VSync Out Width Low (3A)

7	6	5	4	3	2	1	0
$VSOUTWID_7$	$VSOUTWID_6$	$VSOUTWID_5$	$VSOUTWID_4$	$VSOUTWID_3$	$VSOUTWID_2$	$VSOUTWID_1$	$VSOUTWID_0$

VSync Out Width High (3B)

7	6	5	4	3	2	1	0
0	0	0	0	0	$VSOUTWID_{10}$	$VSOUTWID_9$	$VSOUTWID_8$

VSync Out Starting Edge Low (3C)

7	6	5	4	3	2	1	0
$VSOUTST_7$	$VSOUTST_6$	$VSOUTST_5$	$VSOUTST_4$	$VSOUTST_3$	$VSOUTST_2$	$VSOUTST_1$	$VSOUTST_0$

VSync Out Starting Edge High (3D)

7	6	5	4	3	2	1	0
0	0	0	0	0	$VSOUTST_{10}$	$VSOUTST_9$	$VSOUTST_8$

VSync Out Ending Edge Low (3E)

7	6	5	4	3	2	1	0
$VSOUTEND_7$	$VSOUTEND_6$	$VSOUTEND_5$	$VSOUTEND_4$	$VSOUTEND_3$	$VSOUTEND_2$	$VSOUTEND_1$	$VSOUTEND_0$

VSync Out Ending Edge High (3F)

7	6	5	4	3	2	1	0
0	0	0	0	0	$VSOUTEND_{10}$	$VSOUTEND_9$	$VSOUTEND_8$

Reg	Bit#	Bit Name	Description
3B, 3A	10-0	$VSOUTWID_{10-0}$	**VSync Out Width [10:0].** Width of VSync Out during a frame.
3D, 3C	10-0	$VSOUTST_{10-0}$	**VSync Starting Edge [10:0].** Starting edge of VSync Out during a frame.
3F, 3E	10-0	$VSOUTEND_{10-0}$	**VSync Ending Edge [10:0].** Ending edge of VSync Out during a frame.

Range of VSOUTWID, VSOUTST, and VSOUTEND: {0 : 2048}

6.2.18 CHR_FREQ - Chroma Subcarrier Frequency

CHR_FREQ (40)

7	6	5	4	3	2	1	0
CHR_FREQ_{31}	CHR_FREQ_{30}	CHR_FREQ_{29}	CHR_FREQ_{28}	CHR_FREQ_{27}	CHR_FREQ_{26}	CHR_FREQ_{25}	CHR_FREQ_{24}

CHR_FREQ (41)

7	6	5	4	3	2	1	0
CHR_FREQ_{15}	CHR_FREQ_{14}	CHR_FREQ_{13}	CHR_FREQ_{12}	CHR_FREQ_{11}	CHR_FREQ_{10}	CHR_FREQ_{9}	CHR_FREQ_{8}

CHR_FREQ (42)

7	6	5	4	3	2	1	0
CHR_FREQ_{15}	CHR_FREQ_{14}	CHR_FREQ_{13}	CHR_FREQ_{12}	CHR_FREQ_{11}	CHR_FREQ_{10}	CHR_FREQ_{9}	CHR_FREQ_{8}

CHR_FREQ (43)

7	6	5	4	3	2	1	0
CHR_FREQ_{7}	CHR_FREQ_{6}	CHR_FREQ_{5}	CHR_FREQ_{4}	CHR_FREQ_{3}	CHR_FREQ_{2}	CHR_FREQ_{1}	CHR_FREQ_{0}

Reg	Bit#	Bit Name	Description
40,41,42,43	all	CHR_FREQ_{31-0}	**Chroma Subcarrier Frequency.** Sets the subcarrier frequency, = subcarrier/27,000,000*2^32..

6.2.19 Chroma Phase, Miscellaneous Bits 45

Chroma Phase (44)

7	6	5	4	3	2	1	0
CHR_PHASE_7	CHR_PHASE_6	CHR_PHASE_5	CHR_PHASE_4	CHR_PHASE_3	CHR_PHASE_2	CHR_PHASE_1	CHR_PHASE_0

Miscellaneous Bit Register 45 (45)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CLRBAR	BYPYCLP

Reg	Bit#	Bit Name	Description
44	7-0	CHR_PHASE_{7-0}	**Pre-set Subcarrier Phase [7:0].** Value for pre-set subcarrier phase (only upper 8 bit programmable, lower 24 bits =0).
45	0	BYPYCLP	**Bypass Y Clamp.** Allows for non-standard range of Luma on Y-inputs. 0=Luma expected range [16:235], and clamped to this range. 1=Luma expected in range [0:255] and no clamping is performed.
45	1	CLRBAR	**Color Bar Mode.** Causes the YC inputs in the encoder to be ignored and forces a color bar pattern onto the input. The color bar pattern is a repeating sequence of 8 colors at 75% amplitude and 100% saturation.

6.2.20 Miscellaneous Bits Registers 46 and 47

Miscellaneous Bits Register 46

7	6	5	4	3	2	1	0
RGB_SETUP	RGB_SYNC_2	RGB_SYNC_1	RGB_SYNC_0	YC_DELAY_2	YC_DELAY_1	YC_DELAY_0	CVBS_EN

Miscellaneous Bits Register 47

7	6	5	4	3	2	1	0
0	0	0	0	CHR_BW_1	COMP_YUV	$COMP\_GAIN_1$	$COMP\_GAIN_0$

Reg	Bit#	Bit Name	Description
46	0	CVBS_EN	**CVBS Enable.** Enables composite and luma outputs.
46	3-1	YC_DELAY_{2-0}	**YC Delay.** Relative pipeline delay between luma and chroma outputs (4=0 clock; 0=luma lags chroma by 4 clocks; 7=chroma lags luma by 3 clocks).
46	6-4	RGB_SYNC_{2-0}	**RGB Sync.** Provide sync to RGB components: [2]=1, sync on red; [1]=1, sync on green; [0]=1, sync on blue.
46	7	RGB_SETUP	**RGB Setup.** Provide black level (0) or blank level (1) setup for RGB outputs..
47	1-0	$COMP\_GAIN_{1-0}$	**Composite Chroma Gain.** Percentage of chroma used in composite output: 00=100%, 01=25%, 10=50%, 11=75%.
47	2	COMP_YUV	**Component YUV.** Enables bypass on the RGB inputs sending component data YUV through.
47	3	CHR_BW_1	**Chroma Filter Bandwidth Control.** 00=narrow, 01=wide, 10=extra wide, 11=ultra wide (see Miscellaneous Bit Register 74 for bit 0).

6.2.21 HSync Width (48), Burst Width (49)

HSync Width (48)

7	6	5	4	3	2	1	0
$HSYNC\_WID_7$	$HSYNC\_WID_6$	$HSYNC\_WID_5$	$HSYNC\_WID_4$	$HSYNC\_WID_3$	$HSYNC\_WID_2$	$HSYNC\_WID_1$	$HSYNC\_WID_0$

Burst Width (49)

7	6	5	4	3	2	1	0
-	$BURST\_WID_6$	$BURST\_WID_5$	$BURST\_WID_4$	$BURST\_WID_3$	$BURST\_WID_2$	$BURST\_WID_1$	$BURST\_WID_0$

Reg	Bit#	Bit Name	Description
48	7-0	$HSYNC\_WID_{7-0}$	**HSync Width.** Width of HSync in 27MHz clocks (LSB bit 0 is tied to zero).
49	6-0	$BURST\_WID_{6-0}$	**Burst Width.** Width of the burst in 27MHz clocks.

6.2.22 Back Porch Width (4A), Cb Burst Amplitude (4B)

Back Porch Width (4A)

7	6	5	4	3	2	1	0
$BPORCH_7$	$BPORCH_6$	$BPORCH_5$	$BPORCH_4$	$BPORCH_3$	$BPORCH_2$	$BPORCH_1$	$BPORCH_0$

Cb Burst Amplitude (4B)

7	6	5	4	3	2	1	0
CB_BURST_7	CB_BURST_6	CB_BURST_5	CB_BURST_4	CB_BURST_3	CB_BURST_2	CB_BURST_1	CB_BURST_0

Reg	Bit#	Bit Name	Description
4A	7-0	$BPORCH_{7-0}$	**Back Porch Width.** Width of the back porch in 27MHz clocks (LSB bit 0 is tied to zero).
4B	7-0	CB_BURST_{7-0}	**Cb Burst Amplitude Setting.** Range {-127:127}

6.2.23 Cr Burst Amplitude (4C), Miscellaneous Bits Register 4D

Cr Burst Amplitude (4C)

7	6	5	4	3	2	1	0
CR_BURST_7	CR_BURST_6	CR_BURST_5	CR_BURST_4	CR_BURST_3	CR_BURST_2	CR_BURST_1	CR_BURST_0

Miscellaneous Bits Register 4D

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SLV_THRS	SLV_MOD

Reg	Bit#	Bit Name	Description
4C	7-0	CR_BURST_{7-0}	**Cr Burst Amplitude Setting.** Range {-127:127}
4D	0	SLV_MOD	**Slave Mode.** Enable bit for Full Slave Mode timing. This does not enable Partial Save Mode and should be cleared unless Full Slave Mode operation is required.
4D	1	SLV_THRS	**Slave Mode Threshold.** Controls the threshold at which the encoder begins the horizontal line adjustments (0=0 line, 1=30 line).

6.2.24 Black Level (4E)

Black Level (4E)

7	6	5	4	3	2	1	0
$BLACK\_LVL_9$	$BLACK\_LVL_8$	$BLACK\_LVL_7$	$BLACK\_LVL_6$	$BLACK\_LVL_5$	$BLACK\_LVL_4$	$BLACK\_LVL_3$	$BLACK\_LVL_2$

Black Level (4F)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	$BLACK\_LVL_1$	$BLACK\_LVL_0$

Reg	Bit#	Bit Name	Description
4E, 4F	7-0, 1-0	$BLACK\_LVL_{9-0}$	**Black Level.** Used to create a setup.

6.2.25 Blank Level (50)

Blank Level (50)

7	6	5	4	3	2	1	0
$BLANK\_LVL_9$	$BLANK\_LVL_8$	$BLANK\_LVL_7$	$BLANK\_LVL_6$	$BLANK\_LVL_5$	$BLANK\_LVL_4$	$BLANK\_LVL_3$	$BLANK\_LVL_2$

Blank Level (51)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	$BLANK\_LVL_1$	$BLANK\_LVL_0$

Reg	Bit#	Bit Name	Description
50, 51	7-0, 1-0	$BLANK\_LVL_{9-0}$	**Blanking Level.** Blanking level during non VBI.

6.2.26 Number of Lines (57-58)

Unused (56)

Number of Lines (57)

7	6	5	4	3	2	1	0
NUM_LINES_9	NUM_LINES_8	NUM_LINES_7	NUM_LINES_6	NUM_LINES_5	NUM_LINES_4	NUM_LINES_3	NUM_LINES_2

Number of Lines (58)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	NUM_LINES_1	NUM_LINES_0

Unused (59)

Reg	Bit#	Bit Name	Description
57, 58	7-0, 1-0	NUM_LINES_{9-0}	**Number of Lines.** Number of lines in a frame. Note that an odd number implies an interlaced image and an even number implies a progressive image.

6.2.27 White Level (5E)

White Level (5E)

7	6	5	4	3	2	1	0
$WHITE\_LVL_9$	$WHITE\_LVL_8$	$WHITE\_LVL_7$	$WHITE\_LVL_6$	$WHITE\_LVL_5$	$WHITE\_LVL_4$	$WHITE\_LVL_3$	$WHITE\_LVL_2$

White Level (5F)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	$WHITE\_LVL_1$	$WHITE\_LVL_0$

Reg	Bit#	Bit Name	Description
5E, 5F	7-0, 1-0	$WHITE\_LVL_{9-0}$	**White Level.**

6.2.28 Cb Color Saturation (60)

Cb Color Saturation (60)

7	6	5	4	3	2	1	0
CB_GAIN_7	CB_GAIN_6	CB_GAIN_5	CB_GAIN_4	CB_GAIN_3	CB_GAIN_2	CB_GAIN_1	CB_GAIN_0

Unused (61)

Reg	Bit#	Bit Name	Description
60	7-0	CB_GAIN_{7-0}	**Cb Color Saturation Control.** (1 LSB = 1/128).

6.2.29 Cr Color Saturation (62)

Cb Color Saturation (60)

7	6	5	4	3	2	1	0
CR_GAIN_7	CR_GAIN_6	CR_GAIN_5	CR_GAIN_4	CR_GAIN_3	CR_GAIN_2	CR_GAIN_1	CR_GAIN_0

Unused (63)

Reg	Bit#	Bit Name	Description
62	7-0	CR_GAIN_{7-0}	**Cr Color Saturation Control.** (1 LSB = 1/128).

6.2.30 Tint (65)

Unused (64)

Tint (65)

7	6	5	4	3	2	1	0
$TINT_7$	$TINT_6$	$TINT_5$	$TINT_4$	$TINT_3$	$TINT_2$	$TINT_1$	$TINT_0$

Reg	Bit#	Bit Name	Description
65	7-0	$TINT_{7-0}$	**Tint Adjustment on Chroma.**

6.2.31 Width of Breezeway (69)

Unused (68)

Width of Breezeway (69)

7	6	5	4	3	2	1	0
0	0	0	BR_WAY_4	BR_WAY_3	BR_WAY_2	BR_WAY_1	BR_WAY_0

Reg	Bit#	Bit Name	Description
69	4-0	BR_WAY_{4-0}	**Width of Breezeway.** In 27MHz clocks.

6.2.32 Front Porch (6C)

Front Porch (6C)

7	6	5	4	3	2	1	0
0	0	FR_PORCH_5	FR_PORCH_4	FR_PORCH_3	FR_PORCH_2	FR_PORCH_1	FR_PORCH_0

Unused (6D)

Reg	Bit#	Bit Name	Description
6C	5-0	FR_PORCH_{5-0}	**Front Porch.** Width of front porch in 27MHz clocks (LSB bit 0 tied to zero).

6.2.33 Active Video Line (71-72), First Video Line (73)

Unused (70)

Active Video Line (71)

7	6	5	4	3	2	1	0
ACT_LINE_{10}	ACT_LINE_{9}	ACT_LINE_{8}	ACT_LINE_{7}	ACT_LINE_{6}	ACT_LINE_{5}	ACT_LINE_{4}	ACT_LINE_{3}

Active Video Line (72)

7	6	5	4	3	2	1	0
0	0	0	0	0	ACT_LINE_{2}	ACT_LINE_{1}	ACT_LINE_{0}

First Video Line (73)

7	6	5	4	3	2	1	0
$1ST\_LINE_{7}$	$1ST\_LINE_{6}$	$1ST\_LINE_{5}$	$1ST\_LINE_{4}$	$1ST\_LINE_{3}$	$1ST\_LINE_{2}$	$1ST\_LINE_{1}$	$1ST\_LINE_{0}$

Reg	Bit#	Bit Name	Description
71, 72	7-0, 2-0	ACT_LINE_{10-0}	**Active Video Line.** Number of 27MHz clocks in active video line (1440 setting refers to 720 of luma pixels and 720 chroma (Cb and Cr) pixels; the LSB bits [1:0] are tied to zero).
73	7-0	$1ST\_LINE_{7-0}$	**First Line of Video.** Line number for the first line of video in a field.

6.2.34 Miscellaneous Bits 74, Sync Level (75)

Miscellaneous Bit Register 74

7	6	5	4	3	2	1	0
UV_ORDER	PAL_MODE	CHR_BW_0	INVERT_TOP	SYS625_50	$CPHASE_1$	$CPHASE_0$	VSYNC5

Sync Level (75)

7	6	5	4	3	2	1	0
$SYNC\_LVL_7$	$SYNC\_LVL_6$	$SYNC\_LVL_5$	$SYNC\_LVL_4$	$SYNC\_LVL_3$	$SYNC\_LVL_2$	$SYNC\_LVL_1$	$SYNC\_LVL_0$

Reg	Bit#	Bit Name	Description
74	0	VSYNC5	**VSync Equalization Pulses.** 0=6 and 1=5 VSync equalization and broad pulses.
74	2-1	$CPHASE_{1-0}$	**Resetting Period of Carrier Clock.** 0=every 8 fields, 1=every 4 fields, 2=every other line, 3=once before any chroma burst and then never reset again.
74	3	SYS625_50	**System Field Format.** 0=525 lines and 59.94 fields/sec system; 1=625 lines and 50 fields/sec system..
74	4	INVERT_TOP	**Invert Field ID Polarity.** Inverts the polarity of the encoder's field identification signal.
74	5	CHR_BW_0	**Chroma Filter Bandwidth Control.** 00=narrow, 01=wide, 10=extra wide, 11=ultra wide (see Miscellaneous Bit Register 47 for bit 1).
74	6	PAL_MODE	**PAL or NTSC Mode.** 0=NTSC, 1=PAL.
74	7	UV_ORDER	**UV Order.** Switches ordering of Cb and Cr inputs.
75	7-0	$SYNC\_LVL_{7-0}$	**Sync Level.** Sync level during non-VBI lines.

6.2.35 VBI Blank Level (7C)

VBI Blank Level (7C)

7	6	5	4	3	2	1	0
$VBIBL\_LVL_9$	$VBIBL\_LVL_8$	$VBIBL\_LVL_7$	$VBIBL\_LVL_6$	$VBIBL\_LVL_5$	$VBIBL\_LVL_4$	$VBIBL\_LVL_3$	$VBIBL\_LVL_2$

VBI Blank Level (7D)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	$VBIBL\_LVL_1$	$VBIBL\_LVL_0$

Reg	Bit#	Bit Name	Description
7C, 7D	7-0, 1-0	$VBIBL\_LVL_{9-0}$	**VBI Blanking Level.** Blanking level during VBI lines.

6.2.36 SOFT_RST, ENC_VER - Encoder Soft Reset, Encoder Version

Encoder Soft Reset (7E)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SOFT_RST

Encoder Version Number (7F)

7	6	5	4	3	2	1	0
ENC_VER_7	ENC_VER_6	ENC_VER_5	ENC_VER_4	ENC_VER_3	ENC_VER_2	ENC_VER_1	ENC_VER_0

Reg	Bit#	Bit Name	Description
7E	0	SOFT_RST	**Encoder Soft Reset.** Writing to this bit resets the video encoder.
7F	7-0	ENC_VER_{7-0}	**Encoder Version Number.** Contains the version of the encoder. This is a read-only register.

6.2.37 Misc. Bit Reg. 80, WSS Clock (81-82), WSS Data F1(83-85)

Miscellaneous Bit Register 80

7	6	5	4	3	2	1	0
0	WSS_F1EN	WSSF0_EN	WSS_TYPE	WSS_CLKBY	WSS_EDGE_1	WSS_EDGE_0	0

WSS Clock (81)

7	6	5	4	3	2	1	0
WSS_CLK_{11}	WSS_CLK_{10}	WSS_CLK_9	WSS_CLK_8	WSS_CLK_7	WSS_CLK_6	WSS_CLK_5	WSS_CLK_4

WSS Clock (82)

7	6	5	4	3	2	1	0
0	0	0	0	WSS_CLK_3	WSS_CLK_2	WSS_CLK_1	WSS_CLK_0

WSS Data Field 1 (83)

7	6	5	4	3	2	1	0
WSS_DATF0_{19}	WSS_DATF0_{18}	WSS_DATF0_{17}	WSS_DATF0_{16}	WSS_DATF0_{15}	WSS_DATF0_{14}	WSS_DATF0_{13}	WSS_DATF0_{12}

WSS Data Field 1 (84)

7	6	5	4	3	2	1	0
WSS_DATF0_{11}	WSS_DATF0_{10}	WSS_DATF0_9	WSS_DATF0_8	WSS_DATF0_7	WSS_DATF0_6	WSS_DATF0_5	WSS_DATF0_4

WSS Data Field 1 (85)

7	6	5	4	3	2	1	0
0	0	0	0	WSS_DATF0_3	WSS_DATF0_2	WSS_DATF0_1	WSS_DATF0_0

Reg	Bit#	Bit Name	Description
80	2-1	WSS_EDGE_{1-0}	**WSS Edge Rate Control.** Edge rates are proportional to the frequency of the WSS clock, but can also be scaled by the WSS_EDGE parameter. Higher numbers indicate faster rise and fall times on the WSS pulses.
80	3	WSS_CLKBY	**WSS Clock Bypass.** Typically this is set=1 in NTSC and 0 in PAL. =1 Causes the chroma clock to be used as the WSS clock, =0 forces the local 12-bit WSS clock to be used.
80	4	WSS_TYPE	**WSS Type.** 1=PAL, ITU-R BT.1119-2, 0=NTSC, EIAJ CPR-1204
80	5	WSSF0_EN	**WSS Field 0 Enable.** Enables WSS signal in Field 0.
80	6	WSSF1_EN	**WSS Field 1 Enable.** Enables WSS signal in Field 1.
81, 82	7-0, 3-0	WSS_CLK_{11-0}	**WSS Clock Frequency.** Calculated from: WSS Clock Frequency / Encoder Clock Frequency.
83,84,85	7-0,7-0,3-0	WSS_DATAF1_{19-0}	**WSS Data for Field 1.** A waveform only appears when WSSF1_EN=1.

6.2.38 WSS Data Field 0(86-88), WSS Line Number Field 1 (89)

WSS Data Field 0 (86)

7	6	5	4	3	2	1	0
WSS_DATF0_{19}	WSS_DATF0_{18}	WSS_DATF0_{17}	WSS_DATF0_{16}	WSS_DATF0_{15}	WSS_DATF0_{14}	WSS_DATF0_{13}	WSS_DATF0_{12}

WSS Data Field 0 (87)

7	6	5	4	3	2	1	0
WSS_DATF0_{11}	WSS_DATF0_{10}	WSS_DATF0_{9}	WSS_DATF0_{8}	WSS_DATF0_{7}	WSS_DATF0_{6}	WSS_DATF0_{5}	WSS_DATF0_{4}

WSS Data Field 0 (88)

7	6	5	4	3	2	1	0
0	0	0	0	WSS_DATF0_{3}	WSS_DATF0_{2}	WSS_DATF0_{1}	WSS_DATF0_{0}

WSS Line Number Field 1 (89)

7	6	5	4	3	2	1	0
WSS_LNF1_{7}	WSS_LNF1_{6}	WSS_LNF1_{5}	WSS_LNF1_{4}	WSS_LNF1_{3}	WSS_LNF1_{2}	WSS_LNF1_{1}	WSS_LNF1_{0}

Reg	Bit#	Bit Name	Description
86,87,88	7-0,7-0,3-0	WSS_DATAF0_{19-0}	**WSS Data for Field 0.** A waveform only appears when WSSF0_EN=1.
89	7-0	WSS_LINEF1_{7-0}	**Field 1 WSS Line.** Line number (relative to the previous VSync) at which the WSS data will appear in Field 1.

6.2.39 WSS Field 0 Line Number, WSS Level, Misc. Bits Reg. 8D (8A-8D)

WSS Field 0 Line Number (8A)

7	6	5	4	3	2	1	0
WSS_LNF0_7	WSS_LNF0_6	WSS_LNF0_5	WSS_LNF0_4	WSS_LNF0_3	WSS_LNF0_2	WSS_LNF0_1	WSS_LNF0_0

WSS Level (8B)

7	6	5	4	3	2	1	0
WSS_LVL_9	WSS_LVL_8	WSS_LVL_7	WSS_LVL_6	WSS_LVL_5	WSS_LVL_4	WSS_LVL_3	WSS_LVL_2

WSS Level (8C)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	WSS_LVL_1	WSS_LVL_0

Miscellaneous Bits Register 8D

7	6	5	4	3	2	1	0
0	0	0	NOTCH_EN	NOTCH_WD	$NOTCH\_FRQ_2$	$NOTCH\_FRQ_1$	$NOTCH\_FRQ_0$

Reg	Bit#	Bit Name	Description
8A	7-0	WSS_LNF0_{7-0}	**Field 0 WSS Line.** Line number (relative to the previous VSync) at which the WSS data will appear in Field 0.
8B, 8A	7-0, 1-0	WSS_LVL_{9-0}	**WSS High Level.** WSS waveform will rise from VBIBL_LVL to WSS_LVL in a 0 to 1 transition.
8D	2-0	$NOTCH\_FRQ_{2-0}$	**Notch Frequency.** Selects from 8 possible frequencies around which the notch will be centered (see table below).
8D	3	NOTCH_WD	**Notch Filter Wide Bandwidth.** 1=wide, 0=narrow.
8D	4	NOTCH_EN	**Notch Filter Enable.** 1=On, 0=Off.

NOTCH_FRQ	Description	Notch Y Value	Notch Y Value
0		1 + 1/8 + 1/16	1.1875
1		1 + 1/8 + 1/64	1.1406
2	CCIR 601 NTSC	1 + 1/8 + 1/16 (wide) 1 (narrow)	1.0938 1.0000
3	SQ Pixel NTSC	1 - 1/128	0.9922
4	SQ Pixel PAL	1 - 1/32 - 1/64	0.9531
5	CCIR 601 PAL	1 - 1/8 - 1/32 -1/128 (wide) 1 - 1/4 + 1/32 -1/128 (narrow)	0.8359 0.7734
6		1 - 1/8 - 1/16 - 1/32	0.7813
7		1 - 1/4 - 1/32	0.7188

Table 6: NOTCH_FRQ Values

Hex Indx	Register	NTSC	PAL	PAL-M	PAL-N	Combination PAL-N
40	CHR_FREQ	0x21f07c1f	0x2a098acb	0x21e6efe3	0x2a098acb	0x21f69446
44	CHR_PHASE	0	0	0	0	0
74	CPHASE	2	0	0	0	0
60	CR_GAIN	137	145	137	137	145
62	CB_GAIN	137	145	137	137	145
4C	CR_BURST	0	31	29	29	31
4B	CB_BURST	59	44	41	41	44
74	SYS625_50	0	1	0	1	1
74	VSYNC5	0	1	0	0	1
74	PAL_MODE	0	1	1	1	1
48	HSYNC_WID	126	126	126	126	126
49	BURST_WID	68	64	68	64	68
4A	BPORCH	118	138	118	138	138
6C	FRNT_PORCH	32	24	32	24	24
69	BREEZE_WAY	22	26	18	26	26
71	ACTIVELINE	1440	1440	1440	1440	1440
50	BLANK_LVL	240	251	240	240	251
7C	WSS_LVL	240	251	240	240	251
4E	BLACK_LVL	282	251	282	282	251
5E	WHITE_LVL	800	800	800	800	800
75	SYNC_LVL	16	16	16	16	16
57	LINE_FRAME	525	625	525	625	625

Table 7: Typical Register Values for Various Standards

7. Design and Layout Considerations

Careful circuit design and layout are key factors that insure a successful implementation of the FS450 in a product. The following guidelines will help insure that your design yields the best possible results.

7.1 Pixel Phase Lock Loop

- The analog supply for the Pixel PLL should always be clean and noise free to insure minimum jitter in the PLL. Do not power other circuitry from the PLL supply.
- The supply line V_{DDPA} should be decoupled with a series resistor of 150W and a 4.7µF tantalum capacitor. If 50/60Hz ripple is an issue, consider using 47 or 100µF. Always have a 1000pF to 0.1µF capacitor to remove high frequency noise.
- Use a solid ground plane under the FS450.

7.2 Video Output Filters

- To reduce step noise on the D/A converter outputs, and to lower EMI, consider placing the 75W termination resistors and the first capacitor of the output filter close to the video output pins of the FS450.

7.3 Analog Power Supply Bypassing, Filtering, and Isolation

- When possible, it is recommended that the analog supply voltages be fed from a linear voltage regulator. Switching power supply noise, and noise from the digital plane can induce visible artifacts into the displayed video. Always provide sufficient filtering and high frequency bypassing to insure that power supply noise is minimized for visual as well as EMI reasons.
- It is recommended that each power supply section be isolated with a ferrite bead and a 4.7µF capacitor. Where the power pins are so close together that the 0.1µF bypass capacitors are adjacent, consider changing one of the adjacent capacitors to 100 to 1000pF to reduce higher frequency noise on the power supply.

7.4 Power and Ground

- Within the FS450, separate power is routed to functional sections: phase locked loop, D/A converters, digital processors and digital drivers. All ground pins should be connected to a common ground plane. Power pins should be segregated into analog and digital sections.
- Clean analog power should be applied to the V_{DDPA}, V_{DDOSC}, and V_{DDDA} pins. A 0.1 µF capacitor should be placed adjacent to each group of pins. The capacitor connected to C_{BYPASS} is critical, and it must be connected to V_{DDDA} to minimize noise at the D/A converter outputs. Chip capacitors are recommended.
- Digital power may be derived from system digital +3.3 volts. If necessary insert a ferrite bead in series with the supply trace. A 47 µF capacitor should be placed across the common +3.3 VDC for V_{DD} and V_{DDDA} to act as a reservoir for heavy currents drawn by D/A converters and internal memories. At least one 0.1 µF capacitor should be located adjacent to V_{DD} pins along each side of the FS450 to supply transient currents.

7.5 Interfacing to the FS450 in a Mixed Voltage Environment

As many devices designed today, the FS450 is powered by +3.3 Volts. However, 5 Volt devices are still very common today and will continue to be used for some time in the future. To meet this interface requirement the FS450 has 5 Volt tolerant inputs.

7.5.1 Interfacing to the SIO bus.

The SIO bus was developed previous to 3.3V logic processes. The SIO bus input voltage specification is 1.5 Volts for V_{IL} and 3.0 Volts for V_{IH}. The FS450 is built on a 3.3 Volt process and has 5 Volt tolerant inputs with a V_{IL} of 0.8 Volts and a V_{IH} of 2.0 Volts.

For most applications this voltage difference is not an issue as the output drive low specification (V_{OL}) of the SIO bus and the FS450 are both 0.4 Volts. However, in heavily loaded SIO busses the output V_{OL} is not always preserved.

An easy way to regain the 0.7 Volt difference in the V_{IL} specification of the FS450 and the SIO bus is to bias the FS450's input negative by a diode drop (D1). The diode can be biased by a long-tail resistor pair or a current source pair. Shown below is the long-tail pair:

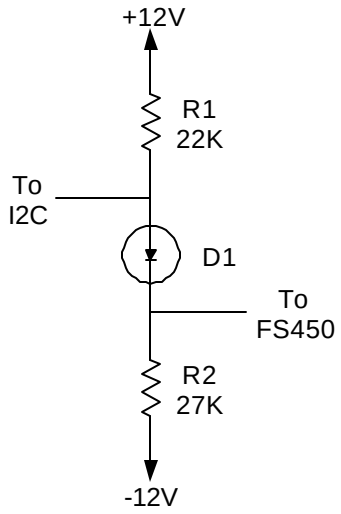


Figure 11. SIO Translation Using Long-tail Resistors
D1 = 1N4148

The long-tail pair is a simple circuit but has the disadvantage of requiring higher voltage power supplies. Also, these supplies may have to powered up in a specific sequence so the surround circuits are not over-voltage.

The translation circuit below requires only one 5 Volt power supply and has no special sequence requirements. In addition, the circuit offers a high impedance load (Q1 become reverse biased) to the SIO bus when its power supply is removed. Unfortunately, it requires more parts. In applications where transistors are more readily available, R2 and R3 can be replaced with diode connected transistors.

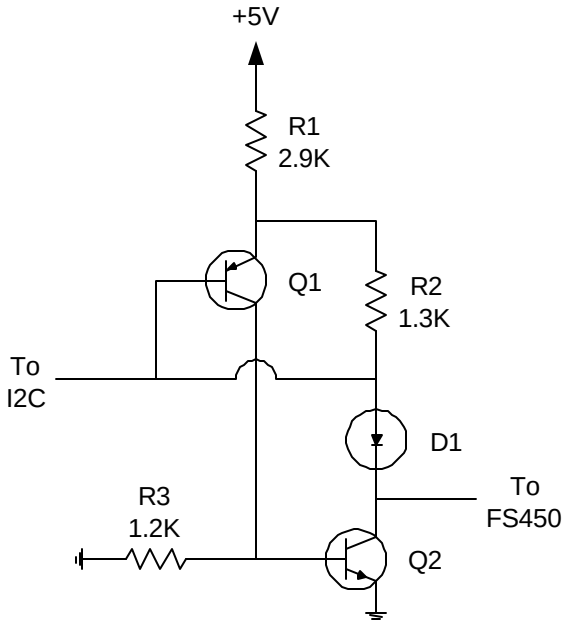


Figure 12. SIO Translation Using Current Mirrors
D1 = 1N4148, Q1 = 2N3906, Q2 = 2N3904

For applications with more than one supply, combinations of the above two circuits can be used. However, the simplest approach to this problem is to limit the loading on the SIO bus when possible. When this is not possible, some of the SIO passive loads can be replaced with active ones. This will increase the SIO access speed without increasing the SIO output low drive current.

8. Specifications

8.1 Absolute Maximum and Recommended Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Rec.	Max	Unit
Power Supply Voltages				
V_{DD} (Measured to V_{SS})	-0.3	3.0-3.6	3.8	V
V_{DDAD} (Measured to V_{SSAD})	-0.3	3.0-3.6	3.8	V
V_{DDPA} and V_{DDPF} (Measured to V_{SSPA} and V_{SSPF})	-0.3	3.0-3.6	3.8	V
V_{DDDA} (Measured to V_{SSDA})	-0.3	3.0-3.6	3.8	V
V_{SSAD}, V_{SSPA}, V_{SS}, V_{SSPA}, V_{SSDA} (delta)	-0.3		0.3	V
Digital Inputs				
3.3 V logic applied voltage (Measured to V_{SS})[2]	-0.3	0-V_{DD}	V_{DD} + 0.3	V
Forced current [3, 4]	-10.0		10.0	mA
Analog Inputs				
Applied Voltage (Measured to V_{SSAD})[2]	-0.3	0-V_{DD}	V_{DDDA} + 0.3	V
Forced current [3, 4]	-10.0		10.0	mA
Digital Outputs				
3.3 V logic applied voltage (Measured to V_{SS})[2]	-0.3	0-V_{DD}	V_{DD} + 0.3	V
Forced current [3, 4]	-6.0		6.0	mA
Short circuit duration (single output in HIGH state to ground)			1	second
Temperature				
Operating, Ambient (R_L=37.5Ω)	0		65	°C
Operating, Ambient (R_L=75Ω)	0		70	°C
Junction			125	°C
Thermal Resistance Junction to Ambient (typical), $Ø_{JA}$			56	°C/W
Thermal Resistance Junction to Case (typical), $Ø_{JC}$			5	°C/W
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)[1]			220	°C
Storage[1]	-40		125	°C
Electrostatic				
Electrostatic Discharge[5]			±150	V

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

8.2 Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply Currents						
I_{DD3}	3.3 volt Digital current	VGA Core Clock=50MHz		165		mA
I_{DDDA}	3.3 volt Analog current	R_L=37.5Ω		85	105	mA
I_{DDDA}	3.3 volt Analog DAC current	R_L=75Ω		45		mA
I_{DDOSC}	3.3 volt Crystal Oscillator current			15		
I_{DDDPA}	3.3 volt VGA PLL current			5		
I_{DDT}	3.3 volt Total Current			270		mA
LVTTL Inputs and Outputs						
C_I	Input Capacitance			5	10	pF
C_O	Output Capacitance			5	10	pF
I_{IH}	Input Current, HIGH	V_{DD3} = 3.3 ± 0.3V, V_{IN} = max.			±10	µA
I_{IL}	Input Current, LOW	V_{DD3} = 3.3 ± 0.3V, V_{IN} = 0 V			±10	µA
I_{ILP}	Input Current, LOW with pull-up	V_{DD3} = 3.3 ± 0.3V, V_{IN} = 0 V	-60		-10	µA
V_{IH}	Input Voltage, Logic HIGH		2.0			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-4.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = -4mA	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = 4mA			0.4	V
GTL Inputs and Outputs						
C_I	Input Capacitance			4	8	pF
C_O	Output Capacitance			4	8	pF
I_{IH}	Input Current, HIGH	V_{DD3} = 3.3 ± 0.3V, V_{IN} = max.			±10	µA
I_{IL}	Input Current, LOW	V_{DD3} = 3.3 ± 0.3V, V_{IN} = 0 V			±10	µA
V_{IH}	Input Voltage, Logic HIGH		V_{REF}+.2			V
V_{IL}	Input Voltage, Logic LOW				V_{REF}-.2	V
V_{REF}	Voltage Reference Range		TBD	0.9	TBD	V
I_{OH}	Output Current, Logic HIGH[1]				-10	µA
I_{OL}	Output Current, Logic LOW[1]				45.0	mA
V_{OL}	Output Voltage, LOW	I_{OL} = 45mA	0.12	0.20	0.34	V
Analog						
V_{IREF}	DAC Current Reference Voltage		1.15	1.276	1.40	V
V_{OC}	Video Output Compliance		-0.4		2	V
R_{OUT}	Video Output Resistance			15		KΩ
C_{OUT}	Video Output Capacitance	C_{OUT} = 0 mA, Freq. = 1 MHz		20		pF

8.3 Switching Characteristics

Parameter		Conditions	Min	Typ[2]	Max	Unit
Clocks						
f_{CKIN}	TV Encoder Reference Clock Frequency			27.0		MHz
f_{XTOL}	TV Reference Clock Frequency Tolerance			30	50[3]	ppm
t_{PWHT}	TV Reference Clock Pulse Width, HIGH		15.0			ns
t_{PWLT}	TV Reference Clock Pulse Width, LOW		15.0			ns
f_{PCKIN}	VGA Clock Positive Edge Frequency	40/60 duty cycle	27.0		85.0	MHz
f_{NCKIN}	VGA Clock Negative Edge Frequency	40/60 duty cycle	27.0		85.0	MHz
f_{CORE}	VGA Core Frequency[4]				50.0	MHz
f_{VCKO}	VGA Clock Output		27.0		85.0	MHz
$t_{JIT-VCK}$	VGA Clock Output Jitter (peak-to-peak)	over a cycle			200	ps
f_{PLLREF}	PLL Reference Clock Frequency		24		100	kHz
M	PLL Numerator		500		1200	
t_{PWHV}	VGA Clock Positive Edge Pulse Width, HIGH		5.0			
t_{PWLV}	VGA Clock Negative Edge Pulse Width, LOW		5.0			
Reset	Assert f_{CKIN} cycles on RESET\ to reset the part		16			Clocks
Digital RGB Input Port						
t_{PDH}	VGA_PCKIN to Data Hold Time		0			ns
t_{NDH}	VGA_NCKIN to Data Hold Time		0			ns
t_{PSU}	VGA_PCKIN to Data Setup Time		1.5			ns
t_{NSU}	VGA_NCKIN to Data Setup Time		1.5			ns
CCIR 656 Video Input and Output Port						
t_{TDH}	TV_CKIN to Data Hold Time		0			ns
t_{TSU}	TV_CKIN to Data Setup Time		10.0			ns
t_{TDO}	TV_CKIN to Data Out Delay				24.0	ns
Serial Microprocessor Interface						
t_{DAL}	SCL Pulse Width, LOW			1.3		µs
t_{DAH}	SCL Pulse Width, HIGH			0.6		µs
t_{STAH}	SDA Start Hold Time			0.6		µs
t_{STASU}	SCL to SDA Setup Time (Stop)			0.6		µs
t_{STOSU}	SCL to SDA Setup Time (Start)			0.6		µs
t_{BUFF}	SDA Stop Hold Time Setup			1.3		µs
t_{DSU}	SDA to SCL Data Setup Time			300		ns
t_{DHO}	SDA to SCL Data Hold Time			300		ns

Notes:

1. GTL outputs are open drain, intended to drive 31 ohm termination from 1.8 volts.
2. Values shown in Typ column are typical for VDD = +3.3V and TA = 25°C
3. TV subcarrier acceptance band is ± 300 Hz.
4. VGA Core Frequency = VGA Clock Frequency/(UIM_DEC+1)

9. Mechanical Dimensions

9.1 100-Lead PQFP (KH) Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A				3.00	
A1			0.05	-	
A2			2.55	2.75	
B			0.25	0.40	3,5
C			0.10	0.25	5
D			23.60	24.20	
D_1			19.80	20.20	
E			17.30	18.20	
E1			13.80	14.20	
e			0.65 BSC		
L			0.60	1.00	4
N	100		100		
ND	30		30		
NE	20		20		
α			0	8°	
ccc			-		

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling Dimension is millimeters
3. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the “B” dimension. Dambar cannot be located on the lower radius or the foot.
4. “L” is the length of terminal for soldering to a substrate.
5. “b” & “C” include lead finish thickness.

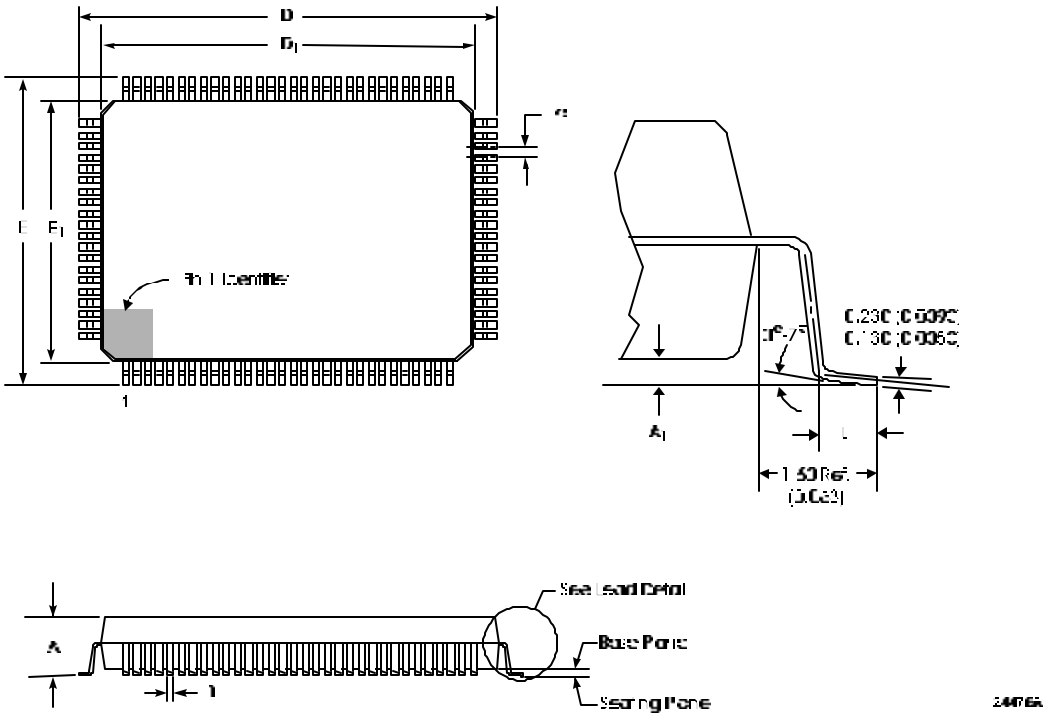


Figure 13: Package Outline & Dimensions

10. Revision History

October 13, 1999: First Release, V1.0.

March 7, 2000: Second Release, V1.1: Throughout: changed encoder registers (40-8D) from little endian to big endian; p. 1, new patent referenced; p.12, corrected table by adding VGA_CKOUTTL, specifying proper clock for non-Intel designs, and proper Syncs for nVidia; p. 13, HSYNC_OUT & VSYNC_OUT are for Slave Mode; p. 14, CSYNC is active high and reverence output voltage is 1.276 V; p. 18 & 39, corrected width of Burst Width register; p. 29, added HSOUTWID, HSOUTST, HSOUTEND registers description; p. 36, added VSOUTWID, VSOUTST, VSOUTEND registers description; p. 52, changes to 7.3 layout considerations; p. 53-4, corrected 5V tolerant issues; p. 56, added V_{IREF}.

June 24, 2000: Third Release, V1.2: minor updates for clarity & formatting, p. 52, updated analog bypass recommendations; p. 58, added pin picture; p. 59, fixed part mark.

11. Order Information

Order Number	Temperature Range	Screening	Package	Package Marking
444-2131	0°C to 65°C	Commercial	100 Lead PQFP	FS450AC
444-2132	0°C to 65°C	Commercial	100 Lead PQFP	FS451AC

Package Markings:

FOCUS
Enhancements
iNet TV FS45x
<YYWWR>
<fab lot id>

where x = 0, or 1; YY=year; WW=work week; R=Revision.

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FOCUS Enhancements, Inc.

600 Research Drive
Wilmington, MA 01887
www.FOCUSinfo.com

Phone: (978) 988-5888
Fax: (978) 988-7555
Email: info@FOCUSinfo.com

