MAS9179

AM Receiver IC

- **Tri Band Receiver IC**
- **High Sensitivity**
- **Very Low Power Consumption**
- **Wide Supply Voltage Range**
- **Power Down Control**
- **Control for AGC On**
- **High Selectivity by Crystal Filter**
- **Fast Startup Feature**

DESCRIPTION

The MAS9179 AM-Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. Only a few external components are required for time signal receiving. The circuit has preamplifier, wide range automatic gain control, demodulator and output comparator built in. The output signal can be processed directly by an additional digital circuitry to extract the data from the received signal. The control for AGC (automatic gain control) can be used to switch AGC on or off if necessary. MAS9179 supports tri band operation by switching between three crystal filters and two additional antenna tuning capacitors.

MAS9179 has differential input and different internal compensation capacitor options for compensating shunt capacitances of different crystals (See ordering information on page 9).

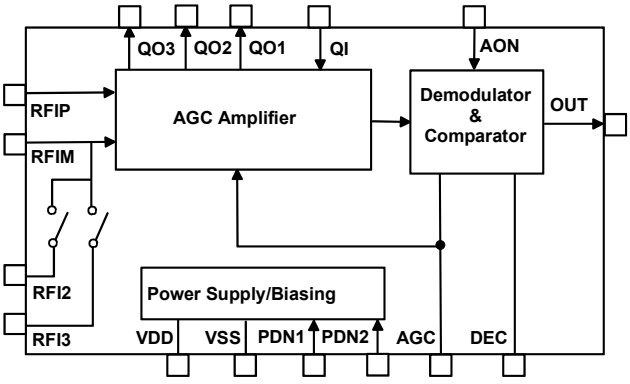
FEATURES

- Tri Band Receiver IC
- Highly Sensitive AM Receiver, 0.4 μV_{RMS} typ.
- Wide Supply Voltage Range from 1.1 V to 5 V
- Very Low Power Consumption
- Power Down Control
- Fast Startup
- Only a Few External Components Necessary
- Control for AGC On
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter

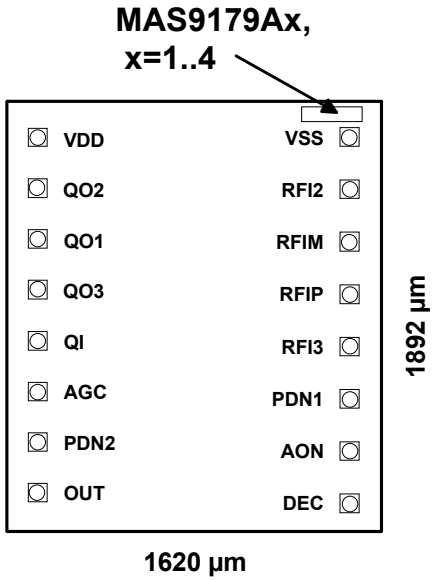
APPLICATIONS

- Multi Band Time Signal Receiver WWVB (USA), JJY (Japan), DCF77 (Germany), MSF (UK), HGB (Switzerland) and BPC (China)

BLOCK DIAGRAM



PAD LAYOUT



DIE size = 1.62 x 1.89 mm; round PAD ∅ 80 µm

Note: Because the substrate of the die is internally connected to VDD, the die has to be connected to VDD or left floating. Please make sure that VDD is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

Note: Coordinates are pad center points where origin has been located in bottom-left corner of the silicon die.

Pad Identification	Name	X-coordinate	Y-coordinate	Note
Power Supply Voltage	VDD	174 µm	1657 µm	
Quartz Filter Output for Crystal 2	QO2	174 µm	1452 µm	
Quartz Filter Output for Crystal 1	QO1	174 µm	1248 µm	
Quartz Filter Output for Crystal 3	QO3	174 µm	1043 µm	
Quartz Filter Input for Crystals	QI	174 µm	839 µm	
AGC Capacitor	AGC	174 µm	634 µm	
Power Down/Frequency Selection Input 2	PDN2	174 µm	429 µm	3
Receiver Output	OUT	175 µm	225 µm	1
Demodulator Capacitor	DEC	1442 µm	240 µm	
AGC On Control	AON	1442 µm	444 µm	2
Power Down/Frequency Selection Input 1	PDN1	1442 µm	649 µm	3
Receiver Input 3 (for Antenna Capacitor 3)	RFI3	1442 µm	853 µm	
Positive Receiver Input	RFIP	1442 µm	1058 µm	4
Negative Receiver Input	RFIM	1442 µm	1262 µm	4
Receiver Input 2 (for Antenna Capacitor 2)	RFI2	1442 µm	1467 µm	
Power Supply Ground	VSS	1442 µm	1671 µm	

Notes:
1) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5$ µA
   - at power down the output is pulled to VSS (pull down switch)
2) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
3) PDN1 = VDD and PDN2 = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down controlled to power up
4) Receiver inputs RFIP and RFIM have both 600 kΩ biasing MOSFET-transistors towards ground

FREQUENCY SELECTION

The frequency selection and power down control is accomplished via two digital control pins PDN1 and PDN2. The control logic is presented in table 1.

Table 1 Frequency selection and power down control

PDN1	PDN2	RFI2 Switch	RFI3 Switch	Selected Crystal Output	Description
High	High	Open	Open	-	Power down
High	Low	Open	Open	QO1	Frequency 1
Low	High	Closed	Open	QO2	Frequency 2, RFI2 capacitor connected in parallel with antenna
Low	Low	Closed	Closed	QO3	Frequency 3, RFI2 and RFI3 capacitors connected in parallel with antenna

The internal antenna tuning capacitor switches (RFI2, RFI3) and crystal filter output switches (QO1, QO2, QO3) are controlled according table 1. See switches in block diagram on page 1.

If frequency 1 is selected the RFI2 and RFI3 switches are open and only crystal output QO1 is active. Antenna frequency is determined by antenna inductor L_{ANT} (see Typical Application on page 5), antenna capacitor C_{ANT1} and parasitic capacitances related to antenna inputs RFIP, RFIM, RFI2 and RFI3 (see Antenna Tuning Considerations below). Frequency 1 is the highest frequency of the three selected frequencies.

If frequency 2 is selected then RFI2 switch is closed to connect C_{ANT2} to pin RFIM in parallel with ferrite antenna and tune it to frequency 2. Then only crystal output QO2 is active. Frequency 2 is the medium frequency of the three selected frequencies.

If frequency 3 is selected both RFI2 and RFI3 switches are closed to connect both C_{ANT2} and C_{ANT3} capacitors to RFIM pin in parallel with ferrite antenna and tune it to frequency 3. Then only crystal QO3 is active. Frequency 3 is the lowest frequency of the three selected frequencies.

It is recommended to switch the device to power down for 50ms before switching to another frequency. This guarantees fast startup in switching to another frequency. The 50ms power down period is used to discharge AGC capacitor and to initialize fast startup conditions.

ANTENNA TUNING CONSIDERATIONS

The ferrite bar antenna having inductance L_{ANT} and parasitic coil capacitance C_{COIL} is tuned to three reception frequencies f_1, f_2 and f_3 by parallel capacitors C_{ANT1}, C_{ANT2} and C_{ANT3}. The receiver input stage and internal antenna capacitor switches have capacitances C_{RFIP}, C_{OFF2}, C_{OFF3} which affect the resonance frequencies. C_{OFF2} and C_{OFF3} are switch capacitances when switches are open. When switches are closed these capacitances are shorted by on resistance of the switches and they are effectively eliminated. Following relationships can be written into three tuning frequencies.

Frequency f_1 (highest frequency):

$C_{TOT1}=C_{COIL}+C_{ANT1}+C_{RFIP}+C_{OFF2}+C_{OFF3}=C_{COIL}+C_{ANT1}+6pF+37pF+119pF=C_{COIL}+C_{ANT1}+162pF$,

$$f_1 = \frac{1}{2\pi\sqrt{L_{ANT} \cdot C_{TOT1}}}$$

Frequency f_2 (middle frequency):

$C_{TOT2}=C_{COIL}+C_{ANT1}+C_{ANT2}+C_{RFIP}+C_{OFF3}=C_{COIL}+C_{ANT1}+C_{ANT2}+ 6pF+119pF=C_{COIL}+C_{ANT1}+C_{ANT2}+ 125pF$,

$$f_2 = \frac{1}{2\pi\sqrt{L_{ANT} \cdot C_{TOT2}}}$$

Frequency f_3 (lowest frequency):

$C_{TOT3}=C_{COIL}+C_{ANT1}+ C_{ANT2}+ C_{ANT3}+C_{RFIP}=C_{COIL}+C_{ANT1}+ C_{ANT2}+ C_{ANT3}+6pF$,

$$f_3 = \frac{1}{2\pi\sqrt{L_{ANT} \cdot C_{TOT3}}}$$

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}-V_{SS}		-0.3	6	V
Input Voltage	V_{IN}		V_{SS}-0.3	V_{DD}+0.3	V
Power Dissipation	P_{MAX}			100	mW
Operating Temperature	T_{OP}		-40	+85	°C
Storage Temperature	T_{ST}		-55	+150	°C

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 1.4V, Temperature = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		1.10		5	V
Current Consumption	I_{DD}	VDD=1.4 V, Vin=0 µVrms VDD=1.4 V, Vin=20 mVrms VDD=3.6 V, Vin=0 µVrms VDD=3.6 V, Vin=20 mVrms	 31 27	64 37 67 40	 91 65	µA
Stand-By Current	I_{DDoff}				0.1	µA
Input Frequency Range	f_{IN}		40		100	kHz
Minimum Input Voltage	$V_{IN\ min}$			0.4	1	µVrms
Maximum Input Voltage	$V_{IN\ max}$		20			mVrms
Receiver Input Resistance Receiver Input Capacitance	R_{RFI} C_{RFI}	f=40kHz..77.5 kHz		230 6		kΩ pF
RFI2 Switch On Resistance RFI2 Switch Off Capacitance	R_{ON2} C_{OFF2}	VDD=1.4 V		3.8 37		Ω pF
RFI3 Switch On Resistance RFI3 Switch Off Capacitance	R_{ON3} C_{OFF3}	VDD=1.4 V		2.4 119		Ω pF
Input Levels $\|I_{IN}\|$<0.5 µA	V_{IL} V_{IH}		 0.8 V_{DD}		0.2 V_{DD}	V
Output Current V_{OL}<0.2 V_{DD};V_{OH}>0.8 V_{DD}	$\|I_{OUT}\|$		5			µA
Output Pulse	T_{100ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	50		140	ms
	T_{200ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	150		230	ms
	T_{500ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	400	500	600	ms
	T_{800ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	700	800	900	ms
Startup Time	T_{Start}	Fast Start-up, Vin=0.4 µVrms Fast Start-up, Vin=20 mVrms		1.3 3.5		s
Output Delay Time	T_{Delay}			50	100	ms

TYPICAL APPLICATION

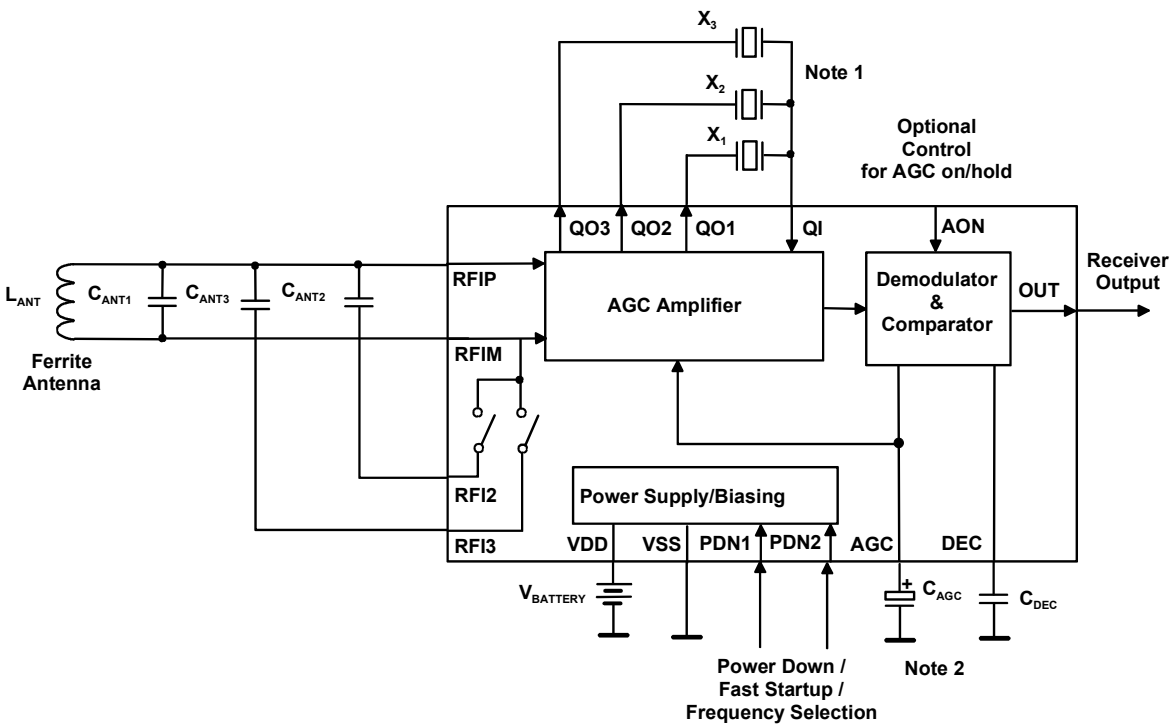


Figure 1 Application circuit of tri band receiver MAS9179

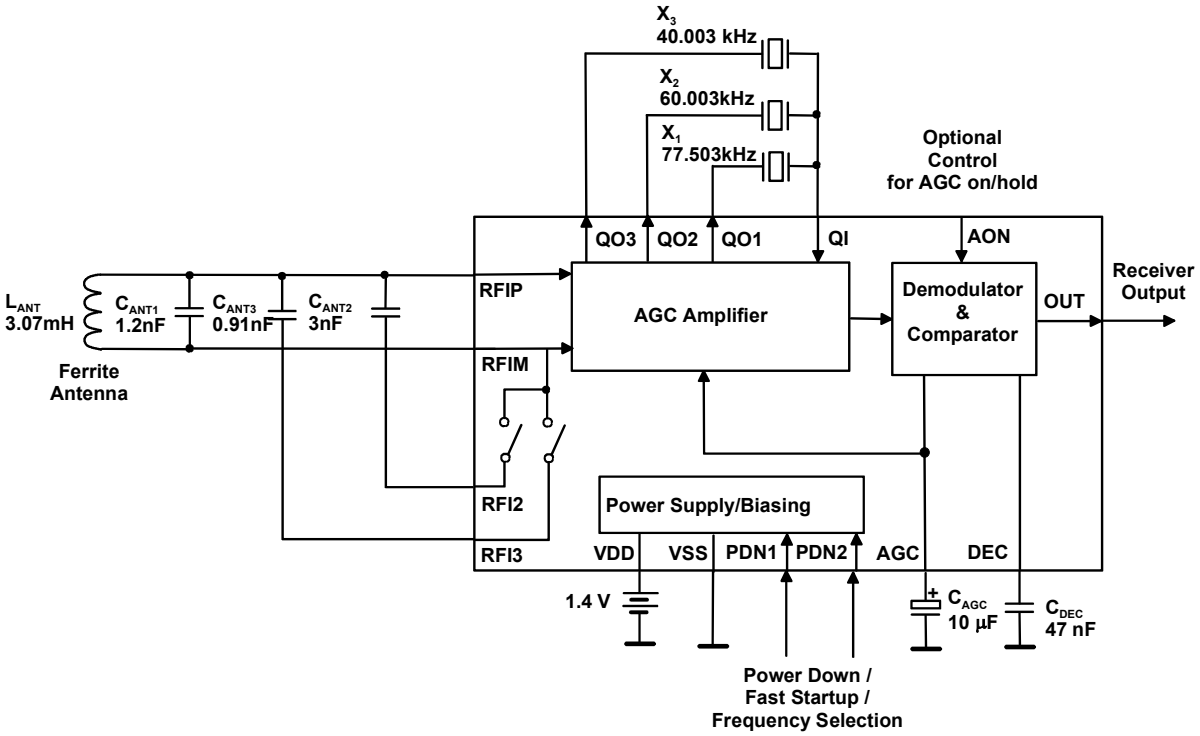


Figure 2 Example circuit of tri band receiver MAS9179 for DCF77/MSF/WWVB/JJY frequencies

TYPICAL APPLICATION (Continued)

Note 1: Crystals
The crystals as well as ferrite antenna frequencies are chosen according to the time-signal system (Table 2). The crystal shunt capacitance C_0 should be matched as well as possible with the internal shunt capacitance compensation capacitor C_C of MAS9179. See Compensation Capacitance Options on table 3.

Table 2 Time-Signal System Frequencies

Time-Signal System	Location	Antenna Frequency	Recommended Crystal Frequency
DCF77	Germany	77.5 kHz	77.503 kHz
HGB	Switzerland	75 kHz	75.003 kHz
MSF	United Kingdom	60 kHz	60.003 kHz
WWVB	USA	60 kHz	60.003 kHz
JJY	Japan	40 kHz and 60 kHz	40.003 kHz and 60.003 kHz
BPC	China	68.5 kHz	68.505 kHz

Table 3 Compensation Capacitance Options

Device	C_C	Crystal Description
MAS9179A1	0.75 pF	For low C_0 crystal
MAS9179A2	0.875 pF	For low C_0 crystal
MAS9179A3	1.25 pF	For high C_0 crystal
MAS9179A4	1.5 pF	For high C_0 crystal

It should be noted that grounded crystal package has reduced shunt capacitance. This value is about 85% of floating crystal shunt capacitance. For example crystal with 1pF floating package shunt capacitance can have 0.85pF grounded package shunt capacitance. PCB traces of crystal and external compensation capacitance should be kept at minimum to minimize additional parasitic capacitance which can cause capacitance mismatching.

Highest frequency crystal is connected to crystal output pin 1 (QO1). Medium frequency crystal is connected to crystal output pin 2 (QO2). Lowest frequency crystal is connected to crystal output pin 3 (QO3). The other pin of each crystal is connected to common crystal input pin QI.

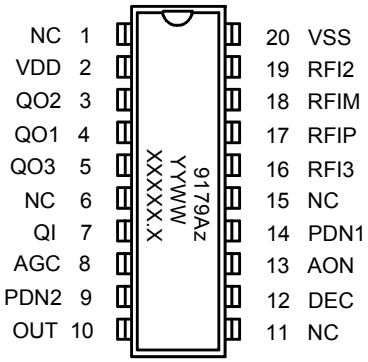
Table 4 below presents some crystal manufacturers having suitable crystals for timesignal receiver application.

Table 4. Crystal Manufacturers and Crystal Types in Alphaphetical Order for Timesignal Receiver Application

Manufacturer	Crystal Type	Dimensions	Web Link
Citizen	CFV-206	ø 2.0 x 6.0	http://www.citizen.co.jp/tokuhan/quartz/
Epson	C-2-Type C-4-Type	ø 1.5 x 5.0 ø 2.0 x 6.0	http://www.epsondevice.com/e/
KDS Daishinku	DT-261	ø 2.0 x 6.0	http://www.kdsj.co.jp/english.html
Microcrystal	MX1V-L2N MX1V-T1K	ø 2.0 x 6.0 ø 2.0 x 8.1	http://www.microcrystal.com/
Seiko Instruments	VTC-120	ø 1.2 x 4.7	http://speed.sii.co.jp/pub/compo/quartz/topE.jsp

Note 2: AGC Capacitor
The AGC and DEC capacitors must have low leakage currents due to very small signal currents through the capacitors. The insulation resistance of these capacitors should be at minimum 100 MΩ. Also probes with at least 100 MΩ impedance should be used for voltage probing of AGC and DEC pins. DEC capacitor can be low leakage chip capacitor.

MAS9179 SAMPLES IN SBDIL 20 PACKAGE



Top Marking Definitions:
YYWW = Year Week
XXXXX.X = Lot Number
z = Sample Version Number

PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
NC	1			
VDD	2	P	Positive Power Supply	
QO2	3	AO	Quartz Filter Output for Crystal 2	
QO1	4	AO	Quartz Filter Output for Crystal 1	
QO3	5	AO	Quartz Filter Output for Crystal 3	
NC	6			1
QI	7	AI	Quartz Filter Input for Crystal	
AGC	8	AO	AGC Capacitor	
PDN2	9	DI	Power Down/Frequency Selection Input 2	3
OUT	10	DO	Receiver Output	2
NC	11			
DEC	12	AO	Demodulator Capacitor	
AON	13	DI	AGC On Control	4
PDN1	14	DI	Power Down/Frequency Selection Input 1	3
NC	15			
RFI3	16	AI	Receiver Input 3 (for Antenna Capacitor 3)	
RFIP	17	AI	Positive Receiver Input	5
RFIM	18	AI	Negative Receiver Input	5
RFI2	19	AI	Receiver Input 2 (for Antenna Capacitor 2)	
VSS	20	G	Power Supply Ground	

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

Notes:

1) Pin 6 between QO3 and QI must be connected to VSS to eliminate DIL package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
2) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5\ \mu A$
   - at power down the output is pulled to VSS (pull down switch)
3) PDN1 = VDD and PDN2 = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down controlled to power up
4) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
5) Receiver inputs RFIP and RFIM have both 600 kΩ biasing MOSFET-transistors towards ground

ORDERING INFORMATION

Product Code	Product	Description	Capacitance Option
MAS9179A1TC00	Tri Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 µm.	C_C = 0.75 pF
MAS9179A2TC00	Tri Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 µm.	C_C = 0.875 pF
MAS9179A3TC00	Tri Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 µm.	C_C = 1.25 pF
MAS9179A4TC00	Tri Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 µm.	C_C = 1.5 pF

Contact Micro Analog Systems Oy for other wafer thickness options.

LOCAL DISTRIBUTOR

MICRO ANALOG SYSTEMS OY CONTACTS

Micro Analog Systems Oy
Kamreerintie 2, P.O. Box 51
FIN-02771 Espoo, FINLAND

Tel. +358 9 80 521
Fax +358 9 805 3213
http://www.mas-oy.com